RS-485 Receivers

Detecting Bus Signals Correctly with Failsafe Biased RS-485 Receivers

Abstract

All RS-485 receivers require a minimum differential input voltage to operate correctly, otherwise they can provide the wrong output signal or even start oscillating. To prevent such malfunctions, resistive voltage dividers (also known as fail-safe biasing networks), are connected to the bus to maintain the input voltage above the minimum level.

Unfortunately, one of the most common mistakes in RS-485 bus node design is the missing or insufficient fail-safe biasing of receiver inputs, leading to the weird receiver behavior mentioned above.

To help engineers gain a deeper understanding of receiver operation and the need for fail-safe biasing, this tech brief explains the functional principle of a receiver and its switching behavior for various input conditions. This tech brief also provides fail-safe biasing examples for a variety of bus configurations and introduces so called full fail-safe receivers that tolerate 0V inputs.

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1. Operating Principles of a Standard Receiver

RS-485 receivers must detect small differential bus signals of as little as ±200mV over the wide common-mode voltage range of -7V to +12V. To accomplish this task, a receiver consists of a differential input voltage divider with biasing stage, followed by a differential comparator (see Figure 1).

The voltage divider action between the input resistors, R_{IN}, and the biasing resistors, R_B, attenuates the line voltage (V_{AB}) by a factor of about 10 to 15. The attenuated input signal (V_{ab}) then is level-shifted (biased) to approximately $V_{CC}/2$. This is necessary to enable the single-supply comparator to process large negative bus signals.

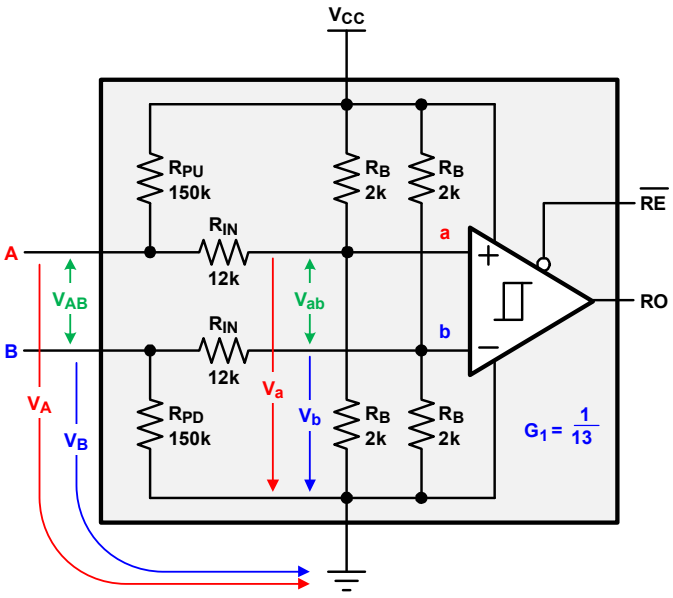

Figure 1. Input Voltage Divider with Comparator

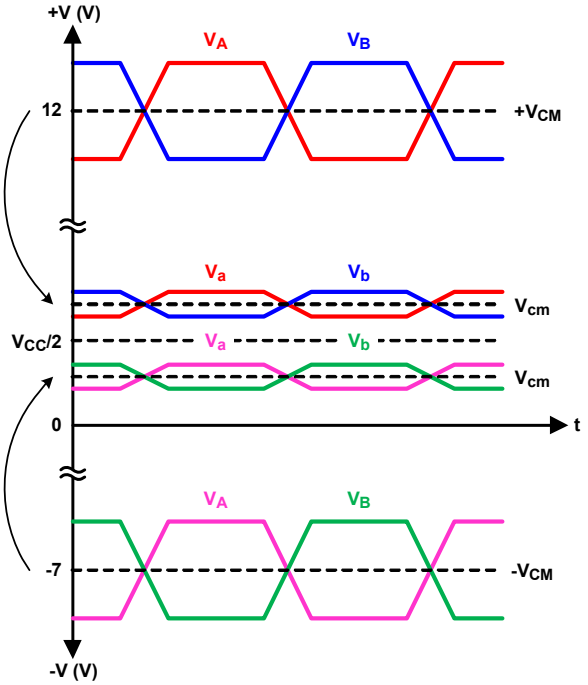

Figure 2. Input Voltage Attenuation and Biasing

Figure 2 shows how large positive and negative line voltages are attenuated and then level-shifted into the positive operating voltage range of the comparator. Expressing the line voltages V_A and V_B through their common-mode and differential components: $V_A = V_{CM} + V_D/2$ and $V_B = V_{CM} – V_D/2$ respectively, the internal comparator input voltages are:

(EQ. 1) $$V_a = \left(V_{CM} + \frac{V_D}{2}\right) \cdot G_1 + V_{CC} \cdot G_2 \quad \text{and}$$

(EQ. 2) $$V_b = \left(V_{CM} - \frac{V_D}{2}\right) \cdot G_1 + V_{CC} \cdot G_2$$

with G_1 as the gain factor of the voltage divider and G_2 the gain factor of the biasing stage.

By signal convention, $V_a – V_b = V_{ab}$, and $V_D = V_A – V_B = V_{AB}$. Thus, the comparator input voltage is:

(EQ. 3) $$V_{ab} = \left(V_{CM} + \frac{V_{AB}}{2}\right) \cdot G_1 + V_{CC} \cdot G_2 - \left(V_{CM} - \frac{V_{AB}}{2}\right) \cdot G_1 - V_{CC} \cdot G_2$$

Equation 3 shows that the differential input structure of the receiver eliminates all common-mode and DC-biasing components, thus simplifying the expression for the comparator's differential input voltage to:

(EQ. 4) $$V_{ab} = V_{AB} \cdot G_1 \quad \text{with} \quad G_1 = \frac{1}{1 + 2R_{IN}/R_B}$$

For the receiver in Figure 1 with R_{IN} = 12kΩ and R_B = 2kΩ, the signal gain is G_1 = 1/13 or 0.077.

2. Minimum Differential Input Voltage

The RS-485 standard specifies a minimum differential input voltage of ±0.2V. The Renesas receiver (and transceiver) datasheets designate the upper and lower limits as the minimum and maximum input voltage thresholds, V_{TH-MIN} and V_{TH-MAX}. Table 1 gives an example for the 80Mbps high-speed receiver ISL32173.

Table 1. Specifications of Receiver Minimum Input Voltage

Parameter	Symbol	Test Condition	Temp (°C)	Min	Typ	Max	Unit
DC Characteristics							
Receiver Differential Threshold Voltage	V_{TH}	$-7V \le V_{CM} \le 12V$	Full	-200		200	mV
Receiver Input Hysteresis	ΔV_{TH}	$V_{CM} = 0V$	25		30		mV

In addition to the electrical specifications, a truth table describes the device switching characteristic by assigning the logic state of the receiver output to the corresponding differential input voltage range (see Table 2). To visualize the switching characteristics described in Table 2, Figure 3 depicts the receiver input conditions and their corresponding output states.

Table 2. Receiver Truth Table

Inputs (A-B)	Output (RO)
$V_{AB} \ge 0.2V$	High
$0.2V \ge V_{AB} \ge -0.2V$	Undetermined
$V_{AB} \le -0.2V$	Low
Inputs open	High

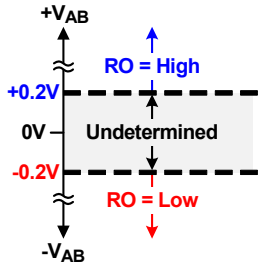

Figure 3. Receiver Input Conditions with Corresponding Output States

3. Bus Conditions

In the case of an actively driven bus, the driver provides sufficient high bus voltage to turn the receiver output high or low, depending on the polarity of the driver output voltage. This is shown in Figure 4.

However, if the driver is disabled (see Figure 5), only the 120Ω termination resistor (R_T) remains connecting Receiver A with the B terminal. In this case, the high input impedance of each terminal (approximately 15kΩ), forms a voltage divider with the low-impedance R_T. This causes the bus voltage to collapse to nearly 0V, which is well below the required 0.2V minimum. Under this condition, the receiver output states are undetermined, meaning the output could be high or low or even oscillating.

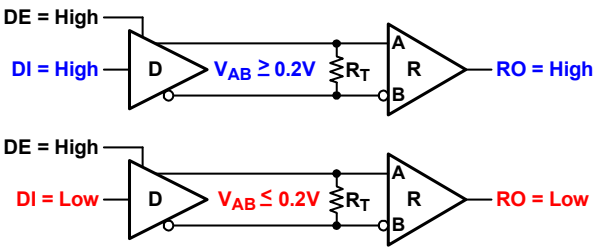

Figure 4. Actively Driven Bus

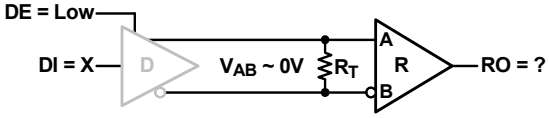

Figure 5. Passive or Undriven Bus

It is important to recognize that input voltages at ±200mV (this is expressed in the truth table as $0.2V \ge V_{AB} \ge -0.2V$), must be avoided under all circumstances.

Another condition is the open-input condition. This can occur when the driver of an unterminated bus is disabled (Figure 6) or there is a cable break or bad connector between the bus and the receiver inputs (Figure 7).

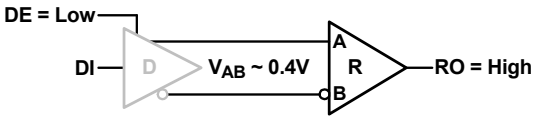

Figure 6. Undriven, Unterminated Bus

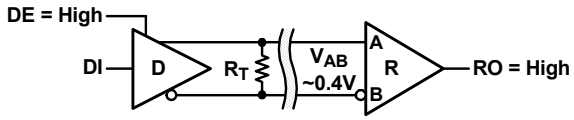

Figure 7. Receiver Disconnected from Terminated Bus

In this case, high-impedance resistors (R_{PU} and R_{PD}) provide a weak bias to the inputs, thus creating a V_{AB} of about 0.4V, which maintains the receiver output high. This function is known as a fail-safe open feature, as it is not essential for the actual receiver operation. **Note**: R_{PU} and R_{PD} have about tenfold the value of R_{IN} to minimize the impact on the voltage divider gain, G_1.

4. Fail-Safe Biasing

Now that we understand how an undriven bus can create 0V bus voltage, we need to passively bias the bus using pull-up and pull-down resistors, commonly referred to as biasing resistors, R_B. These resistors form a voltage divider with R_T, whose output generates a bus voltage larger than 0.2V (Figure 8) to keep the receiver output high. This method is known as fail-safe biasing.

As the resistor network is commonly powered by one of the transceiver/receiver supplies, V_S, we must assume the minimum supply value, V_{CC-MIN}, of that component to ensure a reliable fail-safe biasing operation under worst case conditions.

Also, the bus voltage V_{AB} should include a noise margin, V_N, on top of the input threshold, V_{TH-MAX}, to make allowances for differential noise coming from external sources that might couple into the bus lines: $V_{AB} = V_{TH-MAX} + V_N$. For well-balanced data links, V_N is commonly assumed to be 50mV to 100mV.

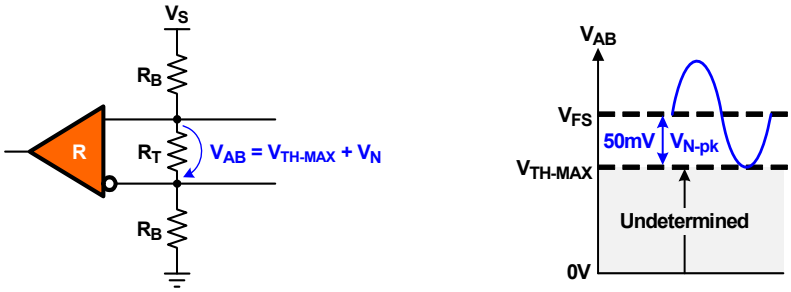

Figure 8. The Fail-Safe Bus Voltage should Include at Least 50mV Noise Margin

Another requirement for the fail-safe biasing network is that AC-wise, the parallel circuit of the termination resistor with the biasing resistors matches the characteristic cable impedance: $Z_0 = R_T \parallel 2R_B$ (Figure 9), which is 120Ω for RS-485 cables.

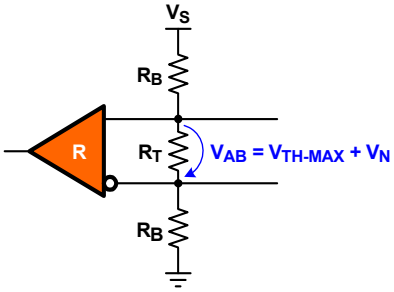

Figure 9. $Z_0 = R_T \parallel 2R_B$

The following sections show fail-safe biasing terminations for various interface configurations.

4.1 Simplex Interfaces: Point-to-Point and Multidrop

Simplex interfaces transmit in one direction only (Figure 10). They consist of a single driver and one or more receivers. Bus termination is applied to the remote cable end, opposite the driver.

If the driver is permanently enabled, a single 120Ω termination resistor is all that is needed. However, if the driver can be disabled by a controller, a fail-safe biasing network must be installed. In this case, the resistor values are calculated using Equations 5 and 6:

(EQ. 5) $$R_B = 60\Omega \cdot \frac{V_S}{V_{AB}}$$

(EQ. 6) $$R_T = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

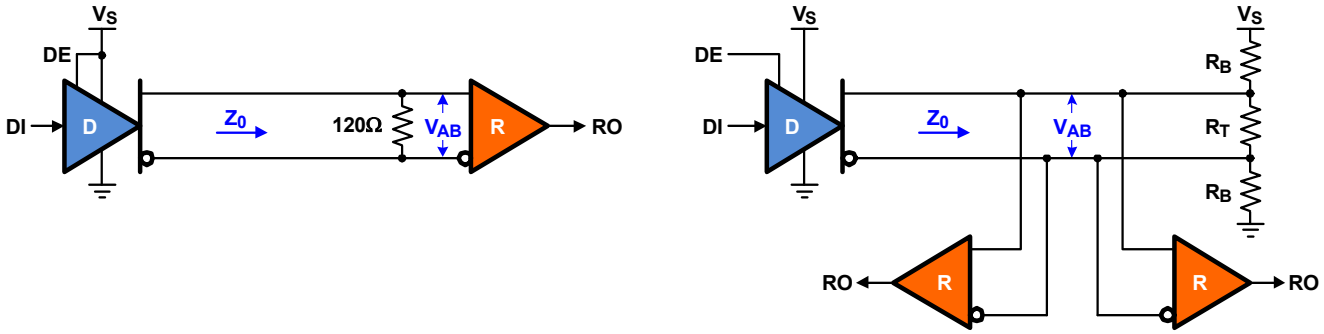

Figure 10. Point-to-Point (left) or Multidrop (right) Data Links in Simplex Mode

4.2 Full-Duplex Interface: Point-to-Point

This interface represents two simplex, point-to-point data links in opposite directions (Figure 11). The designations for the transmit and receive paths correspond with the driver outputs and receiver inputs of the master node. Again, depending on the driver-control method, the bus terminations can be simple 120Ω resistors or fail-safe biasing networks. In this case, the resistor equations remain the same as shown for Figure 10:

(EQ. 7) $$R_B = 60\Omega \cdot \frac{V_S}{V_{AB}}$$

(EQ. 8) $$R_T = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

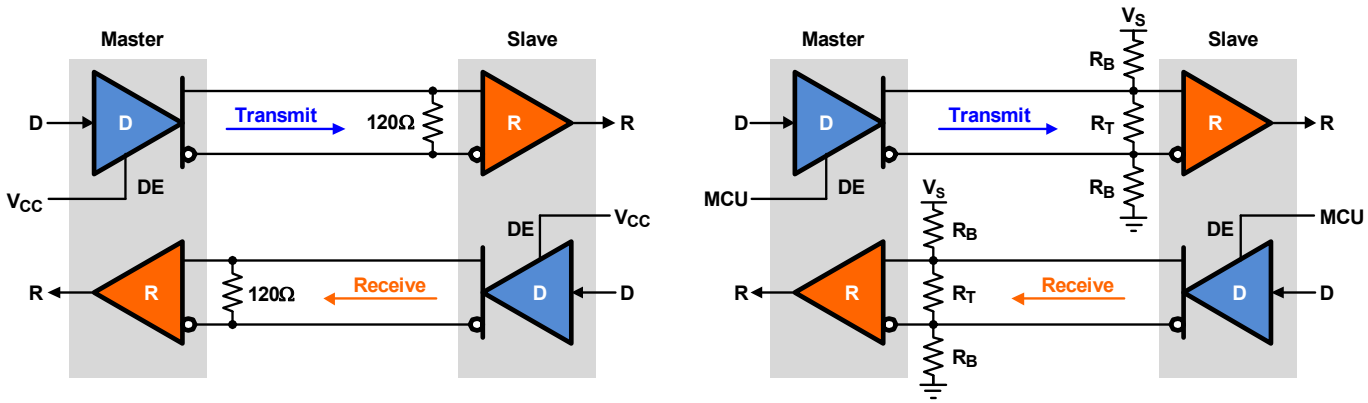

Figure 11. Full-Duplex, Point-to-Point Buses: with Always Enabled Drivers (left) and Controlled Driver Enable Pins (right)

4.3 Full-Duplex Interface: Multipoint

The transmit path of a full-duplex multipoint interface is actually a multidrop bus as only one driver drives multiple receivers (Figure 12). Its driver could therefore be permanently enabled, thus reducing the transmit path termination to a single 120Ω resistor. Figure 12 however, assumes a driver with enable-control, and therefore distinguishes the resistors of its fail-safe biasing network from those in the receive path by adding the suffix “Tx”.

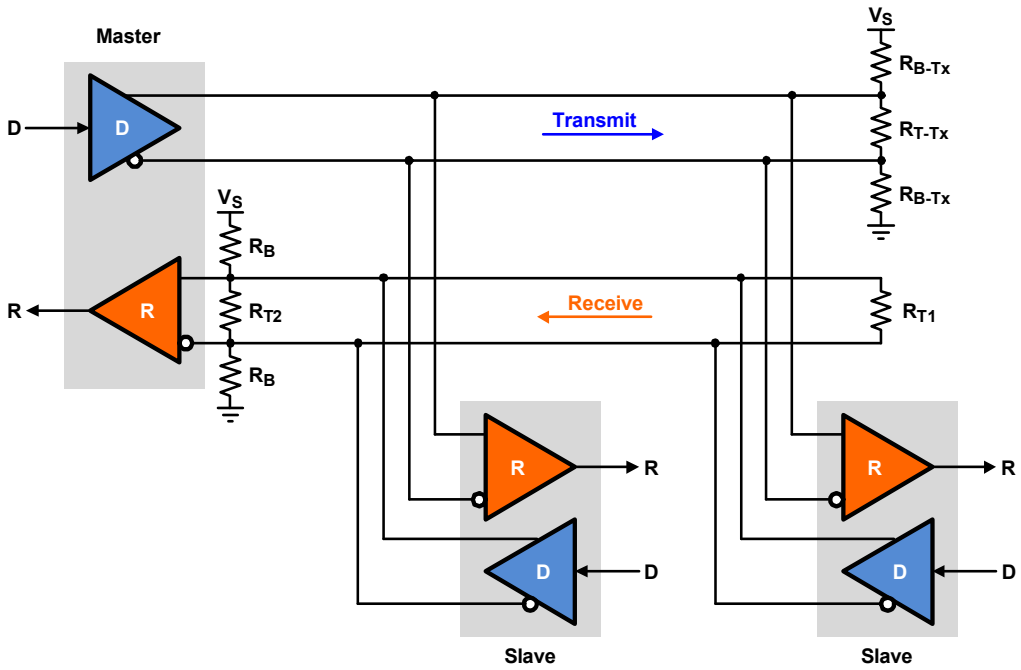

Figure 12. Full-Duplex Multipoint Bus for Higher Data Throughput

The equations for the resistor values of the transmit path are:

(EQ. 9) $$R_{B-Tx} = 60\Omega \cdot \frac{V_S}{V_{AB}}$$

(EQ. 10) $$R_{T-Tx} = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

The receive path is a multipoint bus with multiple drivers, of which the enable functions must be controlled to prevent multiple drivers from accessing the bus at the same time. This is known as bus contention.

As the driver output signal propagates the receive path in both directions, both cable ends must be terminated. This is accomplished by terminating the cable at the opposite end of the master node receiver with a single 120Ω resistor and the cable end near the receiver with a fail-safe biasing network. The equations for the resistor values of the receiver path are then:

(EQ. 11) $$R_B = \frac{V_S / V_{AB} + 1}{0.036}$$

(EQ. 12) $$R_{T2} = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

(EQ. 13) $$R_{T1} = 120\Omega$$

4.4 Half-Duplex Interfaces: Point-to-Point and Multipoint

The most commonly applied RS-485 interface configuration is the half-duplex bus. It is used for multipoint and point-to-point data links. Using the master-slave communication principle, any node can receive data at any time, thus allowing the receiver to be constantly enabled. Transmitting data, however, requires driver enable-control to prevent bus contention.

Because driver output signals propagate the bus in both directions, the bus is terminated at both ends. For bus lengths up to about 100m, it is common to terminate the cable end near the master with a fail-safe biasing network, while the other cable end receives a simple 120Ω resistor. Thus, the resistor equations are the same as for the transmit path of the full-duplex bus.

(EQ. 14) $$R_B = \frac{V_S / V_{AB} + 1}{0.036}$$

(EQ. 15) $$R_{T2} = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

(EQ. 16) $$R_{T1} = 120\Omega$$

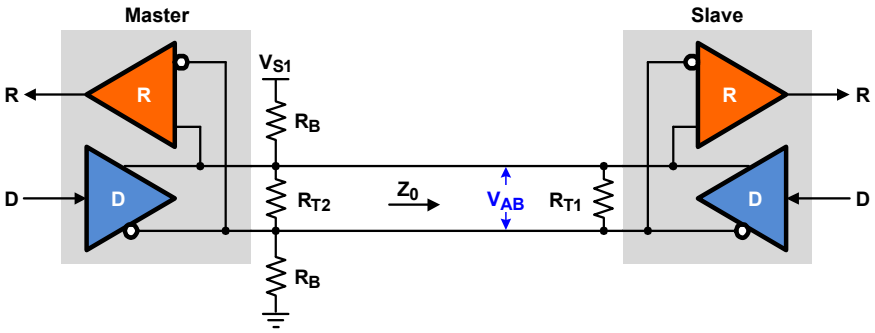

Figure 13. Short Distance Point-to-Point Half-Duplex Interface

For long distance networks, the bus cable's increased DC-resistance can cause significant signal attenuation due to its voltage divider action with the 120Ω resistor. Therefore, it is recommended to apply fail-safe biasing networks at both cable ends. The resistor equations then become:

(EQ. 17) $$R_B = \frac{2V_S / V_{AB} + 1}{0.036}$$

(EQ. 18) $$R_T = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega}$$

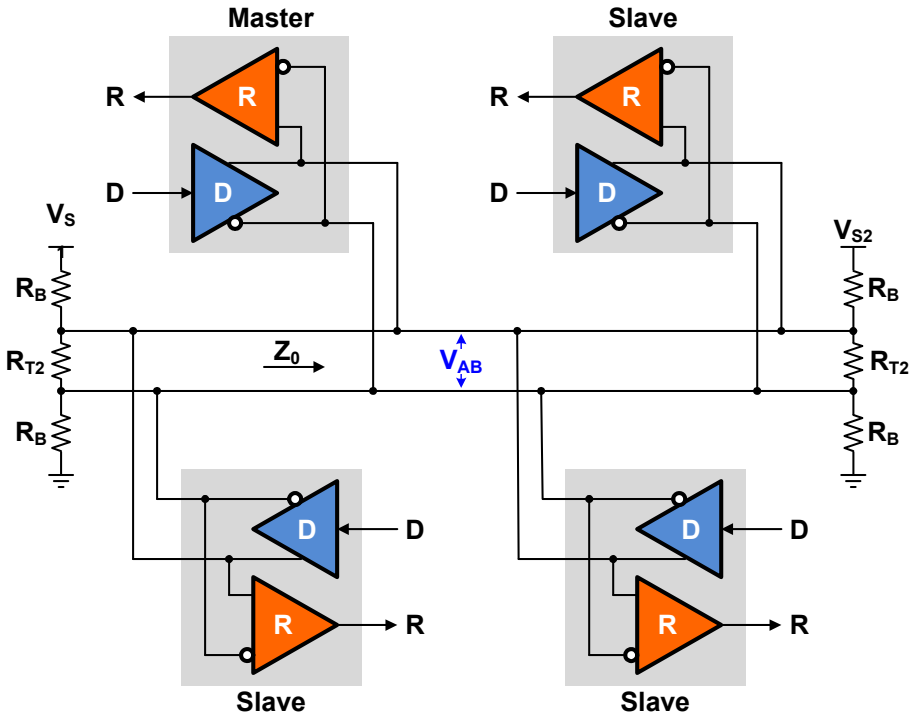

Figure 14. Long Distance Multipoint Half-Duplex Interface

4.5 Full Fail-Safe Receivers and Transceivers

Full Fail-Safe (FFS) transceivers provide internal fail-safe biasing, meaning their outputs turn high under the following conditions:

- Floating inputs, when the device is disconnected from the bus
- Shorted inputs, when a bus fault in the form of a short occurs
- Close to 0V inputs, when a terminated bus is not actively driven

FFS capability is accomplished by offsetting V_{TH-MAX} to slightly negative values of -50mV by means of an internal current source instead of pull-up/down resistors. This causes the receiver output to turn high when the bus voltage is still slightly negative, which enables the detection of 0V bus voltage.

RS-485 applications in less noisy environments can therefore operate without external fail-safe biasing, which contributes to cost and space savings. Electrically noisy environments however, still require external fail-safe networks. Their resistor values can be calculated using the same equations used for standard or fail-safe open transceivers.

The benefits FFS transceivers provide over standard transceiver are:

- For a given level of fail-safe bus voltage, the noise margin is higher due to the lower V_{TH-MAX}.
- For a given noise margin, V_N, the minimum required bus input voltage is smaller, thus allowing for the use of higher resistor values, reducing current consumption.

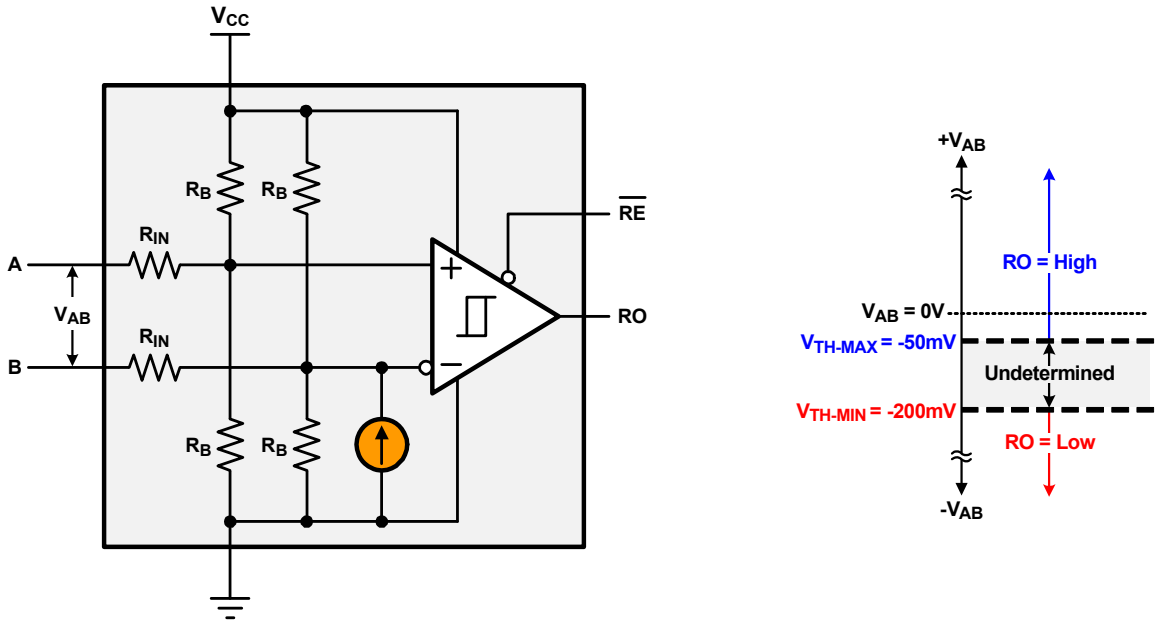

Figure 15. Full Fail-Safe Transceiver with Input Voltage Ranges

5. Conclusion

External fail-safe biasing in RS-485 networks is advised for data links that are not actively driven at certain times, such as during the handover of bus access between drivers, and when bus communication halts.

Networks using standard or fail-safe open transceivers should always apply fail-safe biasing, while FFS transceivers might require external fail-safe biasing only in electrically noisy environments.

The Renesas vast RS-485 portfolio offers transceivers of both fail-safe categories, for wider ranges of data rates, packages, operating temperatures, and overvoltage protection.

6. References

1. ANSI TIA-485-A, “Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems”.
2. AN1986, “External Fail-Safe Biasing of RS-485 Networks”.

7. Revision History

Rev.	Date	Description
1.00	May.9.19	Applied new formatting. Updated Figure 14.
0.00	Aug.6.17	Initial release

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