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## **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU		Document No.	TN-V85-A0039A/E	Rev.	1.00
Title	Cautions on using On-Chip Debugging		Information Category	Technical Notification		
Applicable Product	V850E2/Fx4 V850E2/Fx4-H V850E2/Fx4-G V850E2/Fx4-L	Lot No.	Reference Document	User's Manual: Hardware R01UH0076ED0200 R01UH0002ED0200 R01UH0366EJ0100 R01UH0114ED0200		

The following notes will be added in the "Cautions on using On-Chip Debugging" described in the user's manual of the applicable product.

- 35.5 Cautions on using On-Chip Debugging (Fx4)
- 36.5 Cautions on using On-Chip Debugging (Fx4-H)
- 23.5 Cautions on using On-Chip Debugging (Fx4-G, Fx4-L)

In the case of using "User's Manual: Hardware" regarding the products above, please use this document together.

## [Additional Contents]

## Before:

(1) Handling of device that was used for debugging

Do not mount a device that was used for debugging on a mass-produced product,

because the flash memory was rewritten during debugging

and thus the number of flash memory rewrites cannot be guaranteed.



## After:

- (1) Handling of device that was used for debugging Do not mount a device that was used for debugging on a mass-produced product, because the flash memory was rewritten during debugging and thus the number of flash memory rewrites cannot be guaranteed.
- (2) If a pin reset is input while self-programming is in progress (the FLMD0 signal is at the high level) in debugging mode (the DCUTRST pin is at the high level), debugging will be suspended.
  In that case, input the pin reset again while FLMD0 is at the low level.
- (3) After power is supplied to the microcomputer, place the high level on the RESET pin while the DCUTRST pin is low. If the internal NEXUS function has not been initialized yet so that the signal on the RESET pin changes from the low to the high level while the signal on the DCUTRST pin is still high, release from the reset state will not proceed because internal signals are undefined, and the CPU will not operate.
- (4) After the chip is released from the RESET state and the transition of the level on the  $\overline{DCUTRDY}$  pin from the high to the low level, wait until at least 10 cycles of the clock signal on the DCUTCK pin are input while the DCUTMS pin is at the high level and the  $\overline{DCUTRST}$  pin is at the low level before setting the  $\overline{DCUTRST}$  pin to the high level.
- (5) Once the DCUTRST pin is at the high level, keep it at the high level (i.e. do not change the level back from high to low once the DCUTRST pin is set to the high level).
- (6) Terminating operation in on-chip debugging mode under any of the following conditions causes operation to become undefined. After terminating operations in the on-chip debugging mode, set the RESET pin and the DCUTRST pin to the low level so that the start-up sequence for Nexus is executed.
- Power supply off
- Low level on the DCUTRST pin
- ID codes do not match
- FLMD0 pin and