RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A018A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G1A Descriptions in the Hardware Use Rev. 1.10 Changed	Information Category	Technical Notification			
		Lot No.				
Applicable Product	RL78/G1A R5F10E	All lots	Reference Document	RL78/G1A User's Manual: Hardware Rev.1.10 R01UH0305EJ0110 (Mar. 2013)		

This document describes misstatements found in the RL78/G1A User's Manual: Hardware Rev.1.10 (R01UH0305EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
11.2 Configuration of A/D Converter	Pages 363	Incorrect descriptions revised
11.3.2 A/D converter mode register 0 (ADM0)	Pages 371 to 375	Incorrect descriptions revised
12.6 Operation of UART (UART0 to UART2) Communication	Pages 528	Incorrect descriptions revised
12.6.1 UART transmission	Pages 539	Incorrect descriptions revised
13.5.16 Communication operations	Page 637	Incorrect descriptions revised
17.3.4 Port mode registers 0 to 2, 7, 12, 15 (PM0 to PM2, PM7, PM12, PM15)	Pages 746	Incorrect descriptions revised
18.3.3 SNOOZE mode	Page 767	Incorrect descriptions revised
22.3.1.1 Flash memory CRC control register (CRC0CTL)	Pages 808	Incorrect descriptions revised
25.4.3 Procedure for accessing data flash memory	Page 842	Changed specification
29.3.1 Pin characteristics	Page 889 , 890	Incorrect descriptions revised
29.4 AC Characteristics	Page 900	Incorrect descriptions revised
29.5.1 Serial array unit	Page 905 to 917	Incorrect descriptions revised
29.6.1 A/D converter characteristics	Page 929	Extended specification
30.3.1 Pin characteristics	Page 944 , 945	Incorrect descriptions revised
30.4 AC Characteristics	Page 954	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.



Corrections in the User's Manual: Hardware

No.	Corrections and Applica	ble Item	S	Pages in this document	
	Document No. Engl	ish	R01UH0305EJ0110	for corrections	
1	11.2 Configuration of A/D Converter		Page 363	Page 3	
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7	18.3.3 SNOOZE mode		Page 767	Page 14	
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13	29.6.1 A/D converter characteristics		Page 929	Page 25	
14	30.3.1 Pin characteristics		Page 944, 945	Page 26	
15	30.4 AC Characteristics		Page 954	Page 27	

Incorrect: Bold with underline: Correct: Gray hatched

Revision History

RL78/G1A User's Manual: Hardware Rev.1.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A018A/E	Sep. 9, 2013	First edition issued No.1 to 15 in corrections (This notice)



Incorrect:

1. 11.2 Configuration of A/D Converter

(9) AVREFP pin

This pin inputs an external reference voltage (AVREFP).

If using AVREFP as the + side reference voltage of the A/D converter, set the ADREFP1 and ADREFP0 bits of A/D converter mode register 2 (ADM2) to 1.

The analog signals input to ANI2 to ANI12 and ANI16 to ANI30 are converted to digital signals based on the voltage applied between AVREFP and the -side reference voltage (AVREFM/AVSS).

In addition to AVREFP, it is possible to select AVDD, or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

Correct:

(9) AVREFP pin

This pin inputs an external reference voltage (AVREFP). If using AVREFP as the + side reference voltage of the A/D converter, set the A/D converter mode register 2 (ADM2), ADREFP1 bits to 1 and ADREFP0 bits to 0. The analog signals input to ANI2 to ANI12 and ANI16 to ANI30 are converted to digital signals based on the voltage applied between AVREFP and the -side reference voltage (AVREFM/AVSS).

In addition to AVREFP, it is possible to select AVDD, or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.



Incorrect:

2. 11.3.2 A/D converter mode register 0 (ADM0)

 Table 11-3.
 A/D Conversion Time Selection (2/4)

 (2) 12 bit A/D Converter
 When there is stabilization wait time (hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode ^{Note 1}))

A/D	Convert	ter Mod	e Regis	ter 0	Mode	Conversion	Number of	Number of	Stabilization	Stab	vilization Wait T	ime + Convers	ion Time Selec	ction
		(ADM0)				Clock (fad)	Stabilization	Conversion	Wait Time	AVDD = 1.6 to 3.6 V	AVDD = 1.6 to 3.6 V	AVDD = 1.8 to 3.6 V	AVDD = 2.4 to 3.6 V	AVDD = 2.7 to 3.6 V
FR2	FR1	FR0	LV1	LV0			Wait Clock	Clock	+Conversion	$f_{CLK} = 1 \text{ MHz}$	$f_{CLK} = 4 \text{ MHz}$	$f_{CLK} = 8 \text{ MHz}$	$f_{CLK} = 16 \text{ MHz}$	$f_{CLK} = 32 \text{ MHz}$
									Time					
0	0	0	1	Q	Normal 1	fclк/32	4 fc∟ĸ	54 fad	1732/fclк	Setting	Setting	Setting	Setting	54.125 <i>μ</i> s
								of		prohibited	prohibited	prohibited	prohibited	
0	0	1				fclk/16		sampling	868/fclk				54.25 μs	27.125 μs
0	1	0				fclk/8		clock:	436 /fclк			54.5 <i>μ</i> s	27.25 μs	13.625 <i>μ</i> s
0	1	1				fclk/6		11 fad)	328/fclк			41 <i>μ</i> s	20.5 <i>µ</i> s	10.25 <i>μ</i> s
1	0	0				fc∟ĸ/5			274/fclк			34.25 <i>μ</i> s	17.125 <i>μ</i> s	8.5625 μs
1	0	1				fclк/4			220/fclк		55 <i>µ</i> s	27.5 μs	13.75 <i>μ</i> s	6.875 <i>μ</i> s
1	1	0				fclк/2			112/fclк		28 <i>µ</i> s	14 <i>μ</i> s	7 μs	3.5 <i>μ</i> s
1	1	1				fc∟к/1	2 fclк		56/f ськ	56 <i>μ</i> s	14 <i>µ</i> s	7 <i>μ</i> s	3.5 <i>μ</i> s	Setting
					Normal 2	((0.0	EQ four	66 fue	0.170%	0	0	0	0	prohibited
0	0	0	1	1	Nomai 2	fclk/32	30 ICLK	(number	2170/fcLk	Setting	Setting	Setting	Setting	67.8125 <i>μ</i> s
	0	4				four/16		of	1111/fork	profibiled	promibilied	promibilied		3/ 8125 10
0	0	1				four/9		sampling	596/four			72.25 / Note2	26.625 μs	19 2125 vc
0	1	0				four/G		CIOCK:				FG 75 το Note 2	29.275μ	14 1975 vo
0	1	1						20 IAD)	434/ICLK			0.70 μs	20.375 μs	14.1075 μs
1	0	0				TCLK/5			388/ICLK		Note 2	48.5 µs	24.25 μs	12.125 μs
1	0	1				fclk/4			322/fclk		80.5 µS	40.25 µS	20.125 μs	10.0625 μs
1	1	0				fclk/2	20.6		190/fclк	- Note 2	47.5 μS ¹⁰⁰²	23.75 µS	11.875 μs	5.9375 μs
1	1	1				fc∟ĸ/1	29 ICLK		95/fc∟ĸ	95 μ s hole 2	23.75 µs ¹⁰⁰²	11.875 µs ¹⁰⁰²	5.9375 <i>μ</i> s	Setting
	0	0	4	0		for 1/22	15 four	76 fan	2447/faux	Sotting	Sotting	Sotting	Sotting	prohibited
0	0	0	1	0	ge 1	ICLK/ 32	TO TOLK	(number	Z447/ICLK	prohibited	prohibited	prohibited	prohibited	70.40075 µS
0	0	1			-	fciк/16		of	1231/fci.к	promoted	promoted	promoted	76.9375 / 6 Note 2	38,46875 / 6 Note 2
0	1	0				fcik/8		sampling	623/fci.k			77.875 <i>u</i> s	38.9375 / 6 Note 2	19.46875 /6 ^{Note2}
0	1	1				fcik/6		CIOCK: 33 fad)	471/fci.к			58.875 //s	29,4375 / 6 Note 2	14,71875 / 6 ^{Note 2}
1	0	0				fcik/5		,	395/fci.к			49.375 <i>u</i> s	24.6875 / 6 ^{Note 2}	12.34375 / 6 Note 2
1	0	1				fci k/4			319/fci.к		79.75 //s Note 2	39.875 //s	19.9375 / 6 Note 2	9.96875 /6 Note 2
1	1	0				fcik/2			167/fci.к		41.75 //s Note 2	20.875 //s	10,4375 / 6 Note 2	5 21875 / 6 Note 2
1	1	1				fclк/1			91/fciк	91 µs Note 2	22.75 / 6 Note 2	11.375 //s	5.6875 / 6 Note	Setting
		'							U I/IULI	0. 10		·	0.0010 μ0	prohibited
0	0	0	1	1	Low-volta	fclk/32	8 fclk	230 fad	7368/fclk	Setting	Setting	Setting	Setting	230.25 د Note 2
					ge 2			(number		prohibited	prohibited	prohibited	prohibited	
0	0	1				fclк/16		Of	3688/fclk				230.5 µs ^{Note 2}	115.25 µs Note 2
0	1	0				fclk/8		clock:	1848/fclк			231 µs ^{Note 2}	115.5 <i>µ</i> s ^{Note 2}	57.75 μs ^{Note 2}
0	1	1				fськ/6		187 fad)	1388/fclк			173.5 µs ^{Note 2}	86.75 <i>µ</i> s ^{Note 2}	43.375 //s Note 2
1	0	0				fськ/5			1158/fclк			144.75 µs Note 2	72.375 µs Note 2	36.1875 µs ^{Note 2}
1	0	1				fськ/4			928/fclк		232 <i>µ</i> s	116 <i>µ</i> s ^{Note 2}	Note 2 58 بھ	29 µs ^{Note 2}
1	1	0				fclk/2			468/f ськ		117 <i>μ</i> s	58.5 μs ^{Note 2}	29.25 µs ^{Note 2}	Note 2 مر 14.625 A
1	1	1				fclk/1			238/fclк	238 <i>µ</i> s	59.5 μs	29.75 µs ^{Note 2}	14.875 µs Note 2	Setting
										-				prohibited



Correct:

 Table 11-3.
 A/D Conversion Time Selection (2/4)

 (2) 12 bit A/D Converter When there is stabilization wait time (hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode ^{Note 1}))

A/D	Convert	er Mode	e Regis	ter 0	Mode	Conversion	Number of	Number of	Stabilization	Stab	ilization Wait T	ime + Convers	ion Time Selec	tion
		(ADM0)				Clock (fad)	Stabilization	Conversion	Wait Time	AVDD = 1.6 to 3.6 V	AVDD = 1.6 to 3.6 V	AVDD = 1.8 to 3.6 V	AVDD = 2.4 to 3.6 V	AVDD = 2.7 to 3.6 V
FR2	FR1	FR0	LV1	LV0			Wait Clock	Clock	+Conversion	fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
									Time					
0	0	0	0	0	Normal 1	fclк/32	4 fclк	54 fad	1732/f ськ	Setting	Setting	Setting	Setting	54.125 <i>μ</i> s
								(number of		prohibited	prohibited	prohibited	prohibited	
0	0	1				fc∟к/16		sampling	868/fclк				54.25 <i>μ</i> s	27.125 <i>μ</i> s
0	1	0				fclк/8		clock:	436/f ськ			54.5 <i>μ</i> s	27.25 μs	13.625 <i>μ</i> s
0	1	1				fclк/6		11 fad)	328/fclк			41 <i>μ</i> s	20.5 <i>µ</i> s	10.25 <i>μ</i> s
1	0	0				fclк/5			274/fclк			34.25 <i>μ</i> s	17.125 <i>μ</i> s	8.5625 <i>μ</i> s
1	0	1				fclк/4			220/fclк		55 <i>µ</i> s	27.5 <i>µ</i> s	13.75 <i>μ</i> s	6.875 <i>μ</i> s
1	1	0				fclк/2			112/fclк		28 <i>µ</i> s	14 <i>μ</i> s	7 μs	3.5 <i>μ</i> s
1	1	1				fс∟к/1	2 fclk		56/f с∟к	56 <i>μ</i> s	14 <i>µ</i> s	7 <i>μ</i> s	3.5 <i>μ</i> s	Setting
			-		Normal 2	(/00	58 four	66 fap	0470%	O a tilla ar	O a til a m	O a til a a	O a til a a	prohibited
0	0	0	0	1	Normai 2	TCLK/32	30 ICLK	(number	2170/fclk	Setting	Setting	Setting	Setting	67.8125 μs
0	0	1				fcrk/16		of	1114/fcir	profibiled	promibilied	promibilied		34 8125 15
0	1	0				four/8		sampling	586/fcur			73.25 / s ^{Note 2}	36 625 vs	18 3125 vs
0	1	1				four/6		CIOCK: 23 fad)				56.75 μs ^{Note 2}	28.375μ	14 1875 vs
0	1	1				four/5		2010)	299/four			19.5 (c Note 2	$20.373 \ \mu s$	14.1075 μ 5
1	0	0				ICLK/S			300/ICLK		PO E Lo Note 2	40.3 μs	24.20 μ S	12.123 μs
1	0	1				ICLK/4			322/ICLK		00.3 μs	40.25 /15	20.125 μs	10.0625 μs
1	1	0				TCLK/Z	20 four		190/ICLK	ог – Note 2	47.5 μs	23.75 /ls	11.875 μs	5.9375 µs
1	1	1				TCLK/1	29 ICLK		95/ICLK	95 μs	23.75 µs	11.8/5 <i>µ</i> S	5.9375 μs	Setting
0	0	0	1	0	Low-volta	fc1x/32	15 fcьк	76 fap	2447/fcik	Setting	Setting	Setting	Setting	76 46875 //s Note 2
0	0	0	1	0	ge 1	ICEN CL		(number	2111/101	prohibited	prohibited	prohibited	prohibited	10.10010 #0
0	0	1				fclк/16		of	1231/fclк	•			76.9375 //s Note 2	38.46875 µs ^{Note 2}
0	1	0				fськ/8		sampling	623/fclк			77.875 μs	38.9375 //s Note 2	19.46875 µs ^{Note 2}
0	1	1				fclk/6		33 fad)	471/fclк			58.875 μs	29.4375 //s Note 2	14.71875 µs ^{Note 2}
1	0	0				fclк/5			395/f ськ			49.375 μs	24.6875 //s Note 2	12.34375 µs Note 2
1	0	1				fclк/4			319/fclк		79.75 µs ^{Note 2}	39.875 μs	19.9375 µs Note 2	9.96875 µs Note 2
1	1	0				fськ/2			167/f ськ		41.75 μs ^{Note 2}	20.875 μs	10.4375 //s Note 2	5.21875 µs Note 2
1	1	1				fclк/1			91/f ськ	91 <i>μ</i> s ^{Note 2}	22.75 µs Note 2	11.375 μs	5.6875 μs	Setting
													,	prohibited
0	0	0	1	1	Low-volta	fclк/32	8 fclк	230 fad	7368/fclk	Setting	Setting	Setting	Setting	<mark>Note 2</mark> 230.25 بر 230.25
					ge 2			(number		prohibited	prohibited	prohibited	prohibited	
0	0	1				fclк/16		sampling	3688/f ськ				230.5 µs ^{Note 2}	Note 2 115.25 µs
0	1	0				fськ/8		clock:	1848/fclк			231 µs ^{Note 2}	115.5 <i>µ</i> s ^{Note 2}	57.75 μs ^{Note 2}
0	1	1				fськ/6		187 fad)	1388/fclк			173.5 <i>µ</i> S ^{Note 2}	86.75 <i>µ</i> s ^{Note 2}	43.375 <i>µ</i> S
1	0	0				fс∟к/5			1158/fclк			144.75 μs Note 2	72.375 μs Note 2	36.1875 µs ^{Note 2}
1	0	1				fс∟к/4			928/fclк		232 µs	116 µs ^{Note 2}	58 μs Note 2	29 µs ^{Note 2}
1	1	0				fclк/2			468/f ськ		117 <i>μ</i> s	58.5 μs ^{Note 2}	29.25 µs ^{Note 2}	14.625 µs Note 2
1	1	1				fclk/1			238/fclк	238 <i>µ</i> s	59.5 <i>μ</i> s	29.75 <i>µ</i> s ^{Note 2}	14.875 <i>µ</i> s ^{Note 2}	Setting
														prohibited



Incorrect:

Table 11-3. A/D Conversion Time Selection (4/4)

(4) 8 bit A/D Converter When there is stabilization wait time(hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode ^{Note 1}))

A/D 0	Conver	ter Mo	de Reg	gister	Mode	Conversion	Number of	Number of	Stabilization	Stabiliz	ation Wait Ti	me + Conver	sion Time Se	election
	0	(ADM())			Clock (fad)	Stabilization	Conversion	Wait Time	AVpp = 1.6 to 3.6 V	AV _{DD} = 1.6 to 3.6 V	AV_{DD} = 1.8 to 3.6 V	AV_{DD} = 2.4 to 3.6 V	AVpp = 2.7 to 3.6 V
FR2	FR1	FR0	LV1	LV0			Wait Clock	Clock	+Conversion	fclk = 1 MHz	fclk = 4 MHz	fclk = 8 MHz	fclk = 16 MHz	fclk = 32 MHz
									Time					
0	0	0	1	Q	Normal 1	fclк/32	4 fclк	41 fad	1316/f ськ	Setting	Setting	Setting	Setting	41.125 <i>µ</i> s
								(number of		prohibited	prohibited	prohibited	prohibited	
0	0	1				fclк/16		sampling	660/fclk				41.25 <i>μ</i> s	20.625 µs
0	1	0				fс∟к/8		clock:	332/f ськ			41.5 <i>μ</i> s	20.75 μs	10.375 <i>µ</i> s
0	1	1				fclк/6		11 fad)	250/f ськ			31.25 <i>μ</i> s	15.625 <i>μ</i> s	7.8125 <i>μ</i> s
1	0	0				fclк/5			209/fclk			25.125 μs	13.0625 <i>μ</i> s	6.53125 <i>μ</i> s
1	0	1				fс∟к/4			168/f ськ		42 <i>µ</i> s	21 <i>µ</i> s	10.5 <i>μ</i> s	5.25 μs
1	1	0				fclк/2			86/f ськ		21.5 <i>µ</i> s	10.75 <i>μ</i> s	5.375 <i>μ</i> s	2.6875 <i>µ</i> s
1	1	1				fс∟к/1	2 fclк		43/f cLK	43 <i>µ</i> s	10.75 <i>μ</i> s	5.375 <i>μ</i> s	2.6875 <i>μ</i> s	Setting
					No marcal O		50.6	50.6						prohibited
0	0	0	1	1	Normai 2	fclk/32	30 ICLK	(number	1754/ і ськ	Setting	Setting	Setting	Setting	54.8125 <i>μ</i> s
		4				four/16		of	006/faux	pronibiled	pronibiled	pronibited		29 2125 10
0	0	1				four/9		sampling	490/ICLK			CO 25 , Note 2	$20.125 \mu s$	20.3123 μs
0	1	0				ICLK/O		clock:	402/ICLK			00.23 μs	$30.125 \mu s$	10.0020 μs
0	1	1						2 3 IAD)	370/ICLK			47 µS	23.3 μs	11.75 μs
1	0	0				ICLK/5			323/ICLK		OT C Note 2	40.375 µS	20.1875 μs	10.09375 μs
1	0	1				TCLK/4			270/fclk		67.5 μS	33./5 μS	16.875 μs	8.4375 μs
1	1	0				fclk/2	20 faur		164/fclk	a a Note 2	41 μS	20.5 µS	10.25 μs	5.125 μs
1	1	1				tc∟ĸ/1	29 ICLK		82/fclk	82 μs	20.5 µs ¹⁰⁰²	10.25 µs ^{1.002}	5.125 <i>μ</i> s	Setting
0	0	0	4	0		four/32	15 fcтк	63 fad	2031/four	Setting	Setting	Setting	Setting	63 /6875 (c Note2
0	0	0	1	0	ge 1			(number	200 Micek	prohibited	prohibited	prohibited	prohibited	00.+0070 μ5
0	0	1				fclк/16		of	1023/f ськ				63.9375 L/S Note 2	31.96875 <i>µ</i> s ^{Note 2}
0	1	0				fclk/8		sampling	519/f ськ			64.875 μs	32.4375 µs Note 2	16.21875 µs Note 2
0	1	1				fclк/6		33 fad)	393/f ськ			49.125 μs	24.5625 //s Note 2	12.28125 µs Note 2
1	0	0				fс∟к/5			330/fclk			41.25 μs	20.625 µs Note 2	10.3125 µs Note 2
1	0	1				fclк/4			267/f ськ		66.75 µs Note 2	33.375 μs	16.6875 µs Note 2	8.34375 µs Note 2
1	1	0				fclk/2			141/f ськ		35.25 µs Note 2	17.625 <i>μ</i> s	8.8125 µs Note 2	4.40625 µs Note 2
1	1	1				fськ/1			78/f clk	78 μs ^{Note 2}	19.5 μs Note 2	9.75 <i>μ</i> s	4.875 µs ^{Note 2}	Setting
											,			prohibited
0	0	0	1	1	Low-volta	fclк/32	8 fclk	217 fad	6952/fclk	Setting	Setting	Setting	Setting	217.25 µs Note 2
					ge 2			(number		prohibited	prohibited	prohibited	prohibited	
0	0	1				fclк/16		sampling	3480/f с∟к				217.5 μs ^{Note 2}	108.75 µs
0	1	0				fськ/8		clock:	1744/fclk			218 <i>µ</i> s	109 <i>µ</i> s ^{Note 2}	54.5 <i>µ</i> s ^{Note 2}
0	1	1				fс∟к/6		187 fad)	1310/fcцк			163.75 μs Note 2	81.875 μs Note 2	40.9375 µs ^{Note 2}
1	0	0				fclк/5			1093/fclk			136.625 µs Note 2	68.3125 µs Note 2	34.15625 <i>µ</i> S ^{Note 2}
1	0	1				fськ/4			876/fclk		219 <i>µ</i> s	109.5 µs ^{Note 2}	54.75 µs ^{Note 2}	27.375 µs Note 2
1	1	0				fclk/2			442/fclk		110.5 <i>μ</i> s	55.25 μs ^{Note 2}	27.625 μs Note 2	$13.8125 \mu s^{\text{Note 2}}$
1	1	1				fськ/1			225/fclk	225 <i>µ</i> s	56.25 μs	28.125 μs ^{Note 2}	14.0625 <i>µ</i> s ^{Note 2}	Setting
														prohibited



Correct:

Table 11-3. A/D Conversion Time Selection (4/4)

(4) 8 bit A/D Converter When there is stabilization wait time(hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode ^{Note 1}))

A/D 0	Conver	ter Mo	de Reg	gister	Mode	Conversion	Number of	Number of	Stabilization	Stabiliz	ation Wait Ti	me + Conver	sion Time Se	election
	0	(ADM())			Clock (fad)	Stabilization	Conversion	Wait Time	AV _{DD} = 1.6 to 3.6 V	AV_{DD} = 1.6 to 3.6 V	AV _{DD} = 1.8 to 3.6 V	AV_{DD} = 2.4 to 3.6 V	$AV_{DD} = 2.7$ to 3.6 V
FR2	FR1	FR0	LV1	LV0			Wait Clock	Clock	+Conversion	fclk = 1 MHz	fclk = 4 MHz	fclk = 8 MHz	fclk = 16 MHz	fclk = 32 MHz
									Time					
0	0	0	0	0	Normal 1	fclк/32	4 fclк	41 fad	1316/f ськ	Setting	Setting	Setting	Setting	41.125 <i>µ</i> s
								(number of		prohibited	prohibited	prohibited	prohibited	
0	0	1				fс∟к/16		sampling	660/fclk				41.25 <i>μ</i> s	20.625 µs
0	1	0				fс∟к/8		clock:	332/fclk			41.5 <i>μ</i> s	20.75 <i>µ</i> s	10.375 <i>μ</i> s
0	1	1				fс∟к/6		11 fad)	250/fclk			31.25 <i>μ</i> s	15.625 <i>μ</i> s	7.8125 <i>μ</i> s
1	0	0				fс∟к/5			209/fclk			25.125 <i>μ</i> s	13.0625 <i>μ</i> s	6.53125 <i>μ</i> s
1	0	1				fс∟к/4			168/fclк		42 <i>µ</i> s	21 <i>µ</i> s	10.5 <i>μ</i> s	5.25 <i>μ</i> s
1	1	0				fclк/2			86/f ськ		21.5 <i>µ</i> s	10.75 <i>μ</i> s	5.375 <i>μ</i> s	2.6875 <i>µ</i> s
1	1	1				fclк/1	2 fclk		43/f cLK	43 <i>μ</i> s	10.75 <i>μ</i> s	5.375 <i>μ</i> s	2.6875 <i>μ</i> s	Setting
					Normal 2		50 faun	526-		0	0	0	0	prohibited
0	0	0	0	1	Normai 2	fclk/32	30 ICLK	(number	1754/ î с⊥к	Setting	Setting	Setting	Setting	54.8125 <i>μ</i> s
	0	4				four/16		of		profibiled	promibilied	promibilied		28 3125 ve
0	0	1				four/9		sampling	192/four			60.25 /c Note 2	$30.025 \ \mu s$	20.0120 μs
0	1	0				four/6		clock: 23 fap)	402/ICLK			00.23 μS	$30.125 \ \mu s$	11.75 vo
0	1	1				four/E		20140)	370/ICLK			47 µ5	23.3 μs	11.75 μs
1	0	0							323/ICLK		OT C Note 2	40.373 µS	20.1675 μs	10.09375 μs
1	0	1				TCLK/4			270/ICLK		67.5 μs	33.75 //S	16.875 μs	8.4375 μs
1	1	0				TCLK/2	20 faur		164/fclk	Note 2	41 μS	20.5 µS	10.25 μs	5.125 μs
1	1	1				fclk/1	29 ICLK		82/fclk	82 μs	20.5 µs	10.25 µs	5.125 <i>μ</i> s	Setting
	0	0	4			four/32	15 fcтк	63 fad	2031/four	Setting	Setting	Setting	Setting	63 /6875 /c ^{Note2}
0	0	0	I	0	ge 1			(number	200 MICLK	prohibited	prohibited	prohibited	prohibited	00.40075 μ5
0	0	1				fc_к/16		of	1023/fclk	promoted	promotion	promotod	63.9375 //s ^{Note 2}	31.96875 LS Note 2
0	1	0				fclk/8		sampling	519/fclk			64.875 μs	, 32.4375 L/S Note 2	, 16.21875 <i>μ</i> s ^{Note 2}
0	1	1				fclk/6		33 fad)	393/fclk			, 49.125 μs	24.5625 L/S Note 2	, 12.28125 <i>Lis</i> ^{Note 2}
1	0	0				fclk/5			330/fclk			41.25 μs	20.625 LS Note 2	10.3125 µs Note 2
1	0	1				fclк/4			267/f ськ		66.75 µs Note 2	, 33.375 μs	, 16.6875 µs Note 2	, 8.34375 μs ^{Note 2}
1	1	0				fclk/2			141/fclк		35.25 µs Note 2	17.625 μs	8.8125 µs Note 2	4.40625 µs Note 2
1	1	1				fclk/1			78/f clk	78 μs ^{Note 2}	19.5 <i>μ</i> s Note 2	9.75 μs	4.875 <i>µ</i> s ^{Note 2}	Setting
	-	-								,	/	,	,	prohibited
0	0	0	1	1	Low-volta	fclк/32	8 fclk	217 fad	6952/fclk	Setting	Setting	Setting	Setting	217.25 µs Note 2
					ge 2			(number		prohibited	prohibited	prohibited	prohibited	
0	0	1				fclк/16		ot sampling	3480/f ськ				217.5 <i>µ</i> s ^{Note 2}	108.75 <i>µ</i> s Note 2
0	1	0				fclk/8		clock:	1744/fclк			218 µs	109 µs ^{Note 2}	54.5 <i>µ</i> s Note 2
0	1	1				fclk/6		187 fad)	1310/fcцк			163.75 μs Note 2	81.875 µs Note 2	$40.9375\mu s^{\rm Note2}$
1	0	0				fclk/5			1093/f ськ			136.625 µs	68.3125 ,/.s ^{Note 2}	$34.15625~\mu\mathrm{s}^{\mathrm{Note2}}$
1	0	1				fськ/4			876/f ськ		219 <i>µ</i> s	109.5 <i>µ</i> s ^{Note 2}	54.75 <i>µ</i> s ^{Note 2}	27.375 <i>µ</i> s ^{Note 2}
1	1	0				fclk/2			442/fclk		110.5 <i>μ</i> s	55.25 <i>µ</i> s ^{Note 2}	27.625 µs Note 2	$13.8125\mu s^{\rm Note2}$
1	1	1				fclk/1			225/f ськ	225 µs	56.25 μs	28.125 µs Note 2	14.0625 //s ^{Note 2}	Setting
														prohibited



Incorrect:

3. 12.6 Operation of UART (UART0 to UART2) Communication

• 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	-		_
	2	-	UART1	-
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting	IIC20
	1	CSI21	LIN-bus)	IIC21

Date: Sep. 24, 2013

Correct:

• 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C		
0	0	CSI00	UART0	IIC00		
	1	-		_		
	2	-	UART1	-		
	3	CSI11		IIC11		
1	0	CSI20	UART2 (supporting	IIC20		
	1	-	LIN-bus)	-		

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Incorrect:







Correct:





Incorrect: 5. 13.5.16 Communication operations

Note The wait time is calculated as follows. (IICWL0 setting value + IICWH0 setting value + 4) \times f_{CLK} + t_F \times 2 [clocks] Date: Sep. 24, 2013

Correct:

Note The wait time is calculated as follows. (IICWL0 setting value + IICWH0 setting value + 4[clocks]) / f_{CLK} + t_F × 2



Incorrect:

6. 17.3.4 Port mode registers 0 to 2, 7, 12, 15 (PM0 to PM2, PM7, PM12, PM15)

Figure 17-5. Format of Port Mode Register (PM0 to PM2, PM7, PM12, PM15)

Address: FFF20H After reset: 00H R/W											
Symbol	7	6	5	4	3	2	1	0			
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00			
Address: FF	F21H After	reset: 00H	R/W								
Symbol	7	6	5	4	3	2	1	0			
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10			
Address: FFF22H After reset: 00H R/W											
Symbol	7	6	5	4	3	2	1	0			
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20			
Address: FF	Address: FFF27H After reset: 00H R/W										
Symbol	7	6	5	4	3	2	1	0			
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70			
Address: FF	F2CH After	reset: 00H	R/W								
Symbol	7	6	5	4	3	2	1	0			
PM12	1	1	1	1	1	1	1	PM120			
Address: FF	F2FH After	reset: 00H	R/W								
Symbol	7	6	5	4	3	2	1	0			
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150			
	PM0n	I/C) mode selec	tion for Pmn/	KRm pin (n =	= 0 to 9, m = 1	0 to 2, 7, 12, 1	5)			
	0	Output mode	e (output buffe	er on)							
	1	Input mode	(output buffer	off)							



Correct:

Figure 17-5. Format of Port Mode Register (PM0 to PM2, PM7, PM12, PM15)

Address: FFF20H After reset: FFH R/W											
Symbol	7	6	5	4	3	2	1	0			
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00			
Address: FF	F21H After	reset: FFH	R/W								
Symbol	7	6	5	4	3	2	1	0			
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10			
Address: FFF22H After reset: FFH R/W											
Symbol	7	6	5	4	3	2	1	0			
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20			
Address: FF	F27H After	reset: FFH	R/W								
Symbol	7	6	5	4	3	2	1	0			
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70			
Address: FF	F2CH After	reset: FFH	R/W								
Symbol	7	6	5	4	3	2	1	0			
PM12	1	1	1	1	1	1	1	PM120			
Address: FF	F2FH After	reset: FFH	R/W								
Symbol	7	6	5	4	3	2	1	0			
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150			
	PMmn	I/O m	ode selection	for Pmn/KRk	pin $(n = 0 \text{ to } 7)$	m = 0 to 2, 7	7, 12, 15 , k= () to 9)			
	0	Output mode	e (output buffe	er on)							
	1	Input mode	Input mode (output buffer off)								



Incorrect:

7. 18.3.3 SNOOZE mode

Transition time from SNOOZE mode to normal operation: • When vectored interrupt servicing is carried out: HS (High-speed main) mode : **4.99 to 9.44 \mus + 7 clocks** LS (Low-speed main) mode : **110 to 5.08 \mus + 7 clocks** LV (Low-voltage main) mode : **16.58 to 25.40 \mus + 7 clocks** • When vectored interrupt servicing is not carried out: HS (High-speed main) mode : **4.99 to 9.44 \mus + 7 clocks** LS (Low-speed main) mode : **1.10 to 5.08 \mus + 7 clocks**

LV (Low-voltage main) mode : 16.58 to 25.40µs + 7 clocks

8. 22.3.1.1 Flash memory CRC control register (CRC0CTL)

Symbol	<7>	6	5	4	3	2	1	0
CRC0CTL	CRC0EN	0	FEA5	FEA4	FEA3	FEA2	FEA1	FEA0

CRC0EN	Control of CRC ALU operation
0	Stop the operation.
1	Start the operation according to HALT instruction execution.

FEA5	FEA4	FEA3	FEA2	FEA1	FEA0	High-speed CRC operation range
0	0	0	0	0	0	0 to 3EEBH (16 K to 4 bytes)
0	0	0	0	0	1	0 to 7FFBH (32 K to 4 bytes)
0	0	0	0	1	0	0 to BFFBH (48 K to 4 bytes)
0	0	0	0	1	1	0 to FFFBH (64 K to 4 bytes)
		Other that	Setting prohibited			

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Correct:

Transition time from SNOOZE mode to normal operation: • • When vectored interrupt servicing is carried out: HS (High-speed main) mode : 4.99 to 9.44 μ s + 1 clocks LS (Low-speed main) mode : 1.10 to 5.08 μ s + 1 clocks LV (Low-voltage main) mode : 16.58 to 25.40 μ s + 1 clocks • When vectored interrupt servicing is not carried out: HS (High-speed main) mode : 4.99 to 9.44 μ s + 1 clocks LS (Low-speed main) mode : 1.10 to 5.08 μ s + 1 clocks LS (Low-voltage main) mode : 16.58 to 25.40 μ s + 1 clocks LV (Low-voltage main) mode : 16.58 to 25.40 μ s + 1 clocks

Symbol	<7>	6	5	4	3	2	1	0
CRC0CTL	CRC0EN	0	FEA5	FEA4	FEA3	FEA2	FEA1	FEA0

CRC0EN	Control of CRC ALU operation
0	Stop the operation.
1	Start the operation according to HALT instruction execution.

FEA5	FEA4	FEA3	FEA2	FEA1	FEA0	High-speed CRC operation range
0	0	0	0	0	0	0 to 3FFBH (16 K - 4 bytes)
0	0	0	0	0	1	0 to 7FFBH (32 K - 4 bytes)
0	0	0	0	1	0	0 to BFFBH (48 K - 4 bytes)
0	0	0	0	1	1	0 to FFFBH (64 K - 4 bytes)
Other than above						Setting prohibited



Incorrect:

9. 25.4.3 Procedure for accessing data flash memory The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).<2> Wait for the setup to finish for software timer.etc.

The time setup takes differs for each main clock mode.

<Setup time for each main clock mode>

- HS (High-speed main): 5 µs
- LS (Low-speed main): 720 ns
- LV (Low-voltage main): 10 µs
- <3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.

2. Before executing a STOP instruction during the setup time, temporarily clear DFLEN to 0.

Correct:

The data flash memory is stopped after a reset ends. To access the data flash, make initial settings according to the following procedure.

<1> Set bit 0 (DFLEN) of the data flash control register (DFLCTL) to 1.

<2> Wait for the setup to finish for software timer, etc.

The time setup takes differs for each flash operation mode for the main clock.

- <Setup time for each flash operation mode> • HS (High speed main): 5 µs
- LS (Low speed main): 720 ns
- LV (Low voltage main): 10 µs
- <3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.

- 2. Transition to the STOP mode is not possible during the setup time. To enter the STOP mode during the setup time, clear DFLEN to 0 and then execute the STOP instruction.
- 3. The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, operate the high-speed on-chip oscillator clock (HIOSTOP = 0) and execute the data flash library after 30 μ s have elapsed.

After initialized, the data flash memory can be read by using a CPU instruction or can be read/written by using a data

flash library.

If the DMA controller operates when the data flash memory is accessed, however, follow one of these procedures:

(A) Suspending/forcibly terminating DMA transfer

Before reading the data flash memory, suspend DMA transfer of all the channels used. After setting the DWAITn bit to 1, however, wait at least for the duration of three clocks (f_{CLK}) before reading the

data flash memory. After reading the data flash memory, lift the suspension of transfer by clearing the DWAITn bit to 0.

Or, forcibly terminate DMA transfer in accordance with the procedure in 15.5.5 Forced termination by software before reading the data flash memory. Resume DMA transfer after the data flash memory has been read.

(B) Access the data flash memory by using the newest data flash library.

(C) Insertion of NOP Insert an NOP instruction immediately before the instruction that reads the data flash memory.

<Example>

MOVW HL, addr16 ; Reads RAM.

NOP : Insert NOP instruction before reading data flash memory.

MOV A,[DE] ; Read data flash memory.



If a high-level language such as C is used, however, the compiler may generate two instructions for one code. In this case, the NOP instruction is not inserted immediately before the data flash memory read instruction. Therefore, read the data flash memory by (A) or (B) above.

Remarks 1. n: DMA channel number (n = 0, 1) 2. f_{CLK}: CPU/peripheral hardware clock frequency



Incorrect:

10. 29.3 DC Characteristics

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.6 \text{ V} \le \text{AV}_{\text{DD}} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}, 1.6 \text{ V} \le \text{EV}_{\text{DD0}} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0 \text{ V}) (1/5)$

Note 3. Specification under output current where the duty \leq 70%.

The output current value that has changed the duty ratio lower than 70% can be calculated with the following expression (when changing the duty ratio to n%).

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (2/5)

Note 3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio lower than 70% can can be calculated with the following expression (when changing the duty ratio to n%).

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Correct:

Note 3. Specification under conditions where the duty factor \leq 70%. The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

Note 3. Specification under conditions where the duty factor \leq 70%. The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).



Incorrect:

11. 29.4 AC Characteristics

$(TA = -40 \text{ to } +85^{\circ}\text{C}, 1.6 \text{ V} \le \text{AVDD} \le 3.6 \text{ V}, 1.6 \text{ V} \le \text{EVDD0} \le \text{VDD} \le 3.6 \text{ V}, \text{Vss} = \text{EVss0} = 0 \text{ V})$

	Items	Symbol		Con	ditions		MIN.	TYP.	MAX.	Unit	
	Instruction cycle (minimum	Тсү	Main system HS (high		-speed	$2.7~V\!\le\!V_{DD}\!\le\!3.6~V$	0.03125		1	μS	
	instruction execution time)		clock (f _{main})	main) mo	ode	$2.4~V\!\le\!V_{DD}\!<\!2.7~V$	0.0625		1	μS	
			mode	LV (Low- main) mo	voltage ode	$1.6 V \le V_{DD} \le 3.6 V$	0.25		1	μS	
				LS (low-s main) mo	speed ode	$1.8V \leq V_{DD} \leq 3.6V$	0.125		1	μs	
			Subsystem c operation	lock (fsue	3)	$1.8V\!\leq\!V_{DD}\!\leq\!3.6V$	28.5	30.5	31.3	μS	
			In the self	HS (high	-speed	$2.7~V\!\leq\!V_{DD}\!\leq\!3.6~V$	0.03125		1	μS	
			programming mode	main) mo	ode	$2.4~V\!\le\!V_{DD}\!<\!2.7~V$	0.0625		1	μs	
				LV (Low- main) mo	voltage ode	$1.8V\!\leq\!V_{DD}\!\leq\!3.6V$	0.25		1	μS	
				LS (low-s main) mo	speed ode	$1.8V\!\leq\!V_{DD}\!\leq\!3.6V$	0.125		1	μs	
	External main system clock	fex	$2.7~V \leq V_{\text{DD}} \leq$	≤ 3.6 V			1.0		20.0	MHz	
<r></r>	frequency		$2.4 \text{ V} \leq V_{\text{DD}}$ <	< 2.7 V			1.0		1.0	MHz	
			$1.8 \text{ V} \le \text{Vdd}$	< 2.4 V			1.0		8.0	MHz	
			$1.6 \text{ V} \le \text{V}_{\text{DD}}$ <	< 1.8 V			1.0		4.0	MHz	
		fexs					32		35	kHz	
	External main system clock input	texh, texl	$2.7~V \leq V_{\text{DD}} \leq$	≤ 3.6 V			24			ns	
<r></r>	nigh-level width, low-level width		$2.4 \text{ V} \leq V_{\text{DD}}$ <	< 2.7 V			30			ns	
			$1.8 \text{ V} \le \text{Vdd}$	< 2.4 V			60			ns	
			$1.6 \text{ V} \leq \text{V}_{\text{DD}}$ <	< 1.8 V			120			ns	
		texhs, texls					13.7	, ,			
	TI00, TI01, TI03 to TI07 input high-level width, low-level width	t⊤⊪, t⊤⊫					1/fмск+10			ns ^{Note}	
	T000, T001, T003 to T007	fто	$ \begin{array}{l} \text{HS (high-speed} \\ \text{main) mode} \end{array} \qquad \begin{array}{l} 2.7 \ \text{V} \leq \text{EV}_{\text{DDO}} \\ \hline 1.8 \ \text{V} \leq \text{EV}_{\text{DDO}} \\ \hline 1.6 \ \text{V} \leq \text{EV}_{\text{DDO}} \end{array} $		$\leq EV_{DD0} \leq 3.6 V$			8	MHz		
	output frequency				1.8 V ⊴	$\leq EV_{DD0} < 2.7 V$			4	MHz	
					$1.6~V \leq EV_{\text{DD0}} < 1.8~V$				2	MHz	
			LV (Low-voltage 1 main) mode		$1.6~V \leq EV_{\text{DD0}} \leq 3.6~V$				2	MHz	
			LS (low-spee	ed main)	$1.8~V \leq EV_{\text{DD0}} \leq 3.6~V$				4	MHz	
			mode		1.6 V ⊴	≤ EV _{DD0} < 1.8 V			2	MHz	
	PCLBUZ0, PCLBUZ1 output	f PCL	HS (high-spe	ed	2.7 V ≤	$\leq EV_{DD0} \leq 3.6 V$			8	MHz	
	frequency		main) mode		1.8 V ≤	\leq EV _{DD0} < 2.7 V			4	MHz	
					1.6 V ≤	≤ EV _{DD0} < 1.8 V			2	MHz	
			LV (Low-volta	age	1.8 V ≤	$\leq EV_{DD0} \leq 3.6 V$			4	MHz	
			main) mode		1.6 V ⊴	≤ EV _{DD0} < 1.8 V			2	MHz	
			LS (low-spee	ed main)	1.8 V ≤	$\leq EV_{DD0} \leq 3.6 V$			4	MHz	
			mode		1.6 V ⊴	≤ EV _{DD0} < 1.8 V			2	MHz	
	Interrupt input high-level width,	tinth,	INTP0		1.6 V ≤	$\leq V_{DD} \leq 3.6 \text{ V}$	1			μS	
	IOW-IEVEI WIDTN	L INTL	INTP1 to INT	P11	1.6 V ≤	$\leq EV_{DD0} \leq 3.6 V$	1			μS	
	Key interrupt input high-level width, low-level width	t kr	KR0 to KR9		1.8 V ≤ 1.8 V ≤	$\leq EV_{DD0} \leq 3.6 \text{ V},$ $\leq AV_{DD} \leq 3.6 \text{ V}$	250			ns	
					1.6 V	≤ EV _{DD0} < 1.8 V, ≤ AV _{DD} < 1.8 V	1			μS	
	RESET low-level width	trsl				-	10			μs	



Correct:

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, AV_{DD} \le V_{DD} \le 3.6 \text{ V}, 1.6 \text{ V} \le \text{EVDD0} \le \text{VDD} \le 3.6 \text{ V}, \text{Vss} = \text{EVss0} = 0 \text{ V})$

	Items	Symbol		Con	ditions		MIN.	TYP.	MAX.	Unit	
	Instruction cycle (minimum	Тсү	Main system HS (hig		-speed	$2.7~V\!\leq\!V_{DD}\!\leq\!3.6~V$	0.03125		1	μS	
	instruction execution time)		clock (fmain)	main) mo	ode	$2.4~V\!\le\!V_{DD}\!<\!2.7~V$	0.0625		1	μS	
			mode	LV (Low- main) mo	voltage ode	$1.6V \leq V_{DD} \leq 3.6V$	0.25		1	μS	
				LS (low-s main) mo	speed ode	$1.8V\!\leq\!V_{DD}\!\leq\!3.6V$	0.125		1	μs	
			Subsystem clock (fsub) operation		3)	$1.8V\!\leq\!V_{DD}\!\leq\!3.6V$	28.5	30.5	31.3	μs	
			In the self	HS (high	-speed	$2.7V\!\leq\!V_{DD}\!\leq\!3.6V$	0.03125		1	μS	
			mode	main) mo	ode	$2.4~V\!\le\!V_{DD}\!<\!2.7~V$	0.0625		1	μS	
				LV (Low- main) mo	voltage ode	$1.8V\!\leq\!V_{DD}\!\leq\!3.6V$	0.25		1	μS	
				LS (low-s main) mo	speed ode	$1.8V\!\leq\!V_{DD}\!\leq\!3.6V$	0.125		1	μs	
	External main system clock	fex	$2.7 \text{ V} \leq \text{V}_{\text{DD}} \leq$	≤ 3.6 V			1.0		20.0	MHz	
<k></k>	nequency		$2.4 \text{ V} \leq \text{V}_{\text{DD}}$	< 2.7 V			1.0		16.0	MHz	
			$1.8 V \le V_{DD} <$	< 2.4 V			1.0		8.0	MHz	
			1.6 V ≤ Vdd <	< 1.8 V			1.0		4.0	MHz	
	Extornal main system clock input	fexs	071/21/	() () (32		35	kHz	
<r></r>	high-level width, low-level width	texh, texl	$2.7 V \leq VDD \leq$	≤ 3.6 V			24			ns	
-1.6			$2.4 V \leq VDD <$	< 2.7 V						ns	
			1.0 V ≤ VDD <	< 1.8 V			120			ns	
		texns,	1.0 1 2 100	. 1.0 1			13.7			μS	
		texls									
	TI00, TI01, TI03 to TI07 input high-level width, low-level width	t⊤ıн, t⊤ı∟					1/fмск+10			ns ^{Note}	
	TO00, TO01, TO03 to TO07	fто	$\begin{array}{ll} \text{HS (high-speed} & 2.7 \text{ V} \leq \\ \text{main) mode} & 1.8 \text{ V} \leq \end{array}$		$\leq EV_{DD0} \leq 3.6 V$			8	MHz		
	output frequency				$1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 2.7 \text{ V}$				4	MHz	
					1.6 V ≤	≤ EV _{DD0} < 1.8 V			2	MHz	
			LV (Low-volta main) mode	age	1.6 V ≤	$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6 \text{ V}$			2	MHz	
			LS (low-spee mode	ed main)	1.8 V ≤	$\leq EV_{DD0} \leq 3.6 V$			4	MHz	
		f	LIC (high one	ad	1.6 V ≤	$\leq EVDD0 < 1.8 V$			2	MHZ	
	frequency	IPCL	main) mode	ea	2.7 V ≤	$\leq EVDD0 \leq 3.6 V$			8		
			,		1.0 V 1	$\leq EVDD0 < 2.7 V$			4	MH7	
			IV (Low-volt	ade	1.0 V -	$\leq EV_{DD0} \leq 3.6 V$			4	MHz	
			main) mode	age	1.6 V <	< EVDD0 < 1.8 V			2	MHz	
			LS (low-spee	ed main)	1.8 V ≤	$\leq EV_{DD0} \leq 3.6 V$			4	MHz	
			mode	,	1.6 V ≤	≤ EV _{DD0} < 1.8 V			2	μs 1 μ s 20.0 MHz 8.0 MHz 9.0 MHz 1 μ s 9.0 MHz 10.0 MHz 10.0 MHz 11.0 μ s 12.0 MHz 2 MHz 2 MHz 2 MHz 2 MHz 2 MHz 2 MHz 2	
	Interrupt input high-level width,	tinтн,	INTP0		1.6 V ≤	$\leq V_{DD} \leq 3.6 \text{ V}$	1			μS	
	low-level width	t intl	INTP1 to INT	P11	1.6 V ≤	$\leq EV_{DD0} \leq 3.6 V$	1			μS	
	Key interrupt input high-level	t kr	KR0 to KR9		1.8 V ≤	$\leq EV_{DD0} \leq 3.6 V,$	250			ns	
	width, low-level width				1.8 V ⊴	$\leq AV_{DD} \leq 3.6 \text{ V}$					
					1.6 V	≦ EV _{DD0} < 1.8 V,	1			μS	
	DECET law lavel with				1.6 V ⊴	≦ AVdd < 1.8 V					
	RESET low-level width	trsl					10			μS	



12. 29.5.1 Serial array unit **Incorrect:**

(2)During communication at same potential (CSI mode) (master mode, SCKp... internal clock output corresponding CSI00 only)

$1 = 1010 + 85^{\circ}$	$1 \vee 1 \leq E \vee DD \leq 1 \vee DD \leq 3 \times 1 \vee C \leq E \vee C \leq 0 \leq 1 \vee 1$

Parameter	Symbol	Condition	IS	HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkcy1	$2.7~V \leq EV_{DD} \leq 3.6~V$	tксv1 ≳.4/fc ∟к	83.3 Note 4		250		500		ns
SCKp high-/low-level width	tкн1, tкL1	$2.7 \text{ V} \leq EV_{DD} \leq 3.6 \text{ V}$	/	tксү1/2 –10		tксү1/2 —50		tксү1/2 -50		ns
SIp setup time (to $\overline{SCKp}^{\uparrow}$) Note 5	tsik1	$2.7 \text{ V} \leq EV_{DD} \leq 3.6 \text{ V}$	/	33		110		110		ns
SIp hold time (from $\overline{SCKp}^{\uparrow}$) Note 6	tksi1	$2.7 \text{ V} \leq EV_{\text{DD}} \leq 3.6 \text{ V}$	/	10		10		10		ns
Delay time from SCKp ↓ to SOp output ^{Note 7}	tkso1	C = 30.pF Note 8			10		10		10	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The value must also be 2/fCLK or more.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

8. C is the load capacitance of the SCKp and SOp output lines.

Correct:

(2)During communication at same potential (CSI mode) (master mode, SCKp... internal clock output corresponding CSI00 only)

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.7 \text{ V} \le EV_{DD0} \le V_{DD} \le 3.6 \text{ V}, \text{Vss} = EV_{SS0} = 0 \text{ V})$

Parameter	Symbol	Conditions	HS	HS Note 1 L		Note 2 LV		Note 3	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t ксү1	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 3.6 \text{ V} \text{tkcy1} \geq 2/\text{fclk}$	83.3 Note 4		250		500		ns
SCKp high-/low-level width	tкн1, tкL1	$2.7~V \leq EV_{\text{DD}} \leq 3.6~V$	tксү1/2 –10		tксү1/2 –50		tксү1/2 -50		ns
SIp setup time (to $\overline{SCKp}^{\uparrow}$) Note 5	tsik1	$2.7~V \leq EV_{\text{DD}} \leq 3.6~V$	33		110		110		ns
SIp hold time (from $\overline{SCKp}\uparrow$) Note 6	tksi1	$2.7 \text{ V} \leq EV_{\text{DD}} \leq 3.6 \text{ V}$	10		10		10		ns
Delay time from $\overline{SCKp}\downarrow$ to SOp output Note 7	tkso1	C = 20 pF Note 8		10		10		10	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The fMCL must also be 24MHz or less.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

8. C is the load capacitance of the SCKp and SOp output lines.

Incorrect:

- Notes 1. HS is condition of HS (high-speed main) mode.
 - 2. LS is condition of LS (low-speed main) mode.
 - 3. LV is condition of LV (low-voltage main) mode.
 - 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Sip setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp\" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 7. C is the load capacitance of the SOp output lines.
 - 8. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Correct:

- Notes 1. HS is condition of HS (high-speed main) mode.
 - 2. LS is condition of LS (low-speed main) mode.
 - **3.** LV is condition of LV (low-voltage main) mode.
 - Transfer rate in the SNOOZE mode : MAX. 1 Mbps
 - 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp[†]" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 8. C is the load capacitance of the SOp output lines.



Incorrect:

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) /)

<r></r>	Parameter	Symbol	Conditions			Note 1	LS'	lote 2	LV '	Note 3	Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	SCKp cycle time	tkcy1	$\label{eq:2.7} \begin{split} & 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \\ & 2.3 \ V \leq V_b \leq 2.7 \ V, \\ & C_b = 20 \ pF, \ R_b = 2.7 \ k\Omega \end{split}$	tĸcy1 ≥ 2/f CLK	300		1150		1150		ns
	SCKp high-level width	tкнı	$2.7 \text{ V} \leq E \text{V}_{\text{DD0}} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_{\text{b}} = 20 \text{ pF}, \text{R}_{\text{b}} = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,	tксү1/2 – 120		tксү1/2 - 120		tксү1/2 - 120		ns
	SCKp low-level width	tĸ∟ı	$2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V$ $C_b = 20 \ pF, \ R_b = 2.7 \ k\Omega$	$V \le V_b \le 2.7 V$,	tксү1/2 – 10		tксү1/2 - 50		tксү1/2 - 50		ns
	SIp setup time (to SCKp↑) ^{Note 4}	tsik1	$2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V$ $C_b = 20 \ pF, \ R_b = 2.7 \ k\Omega$	$V \le V_b \le 2.7 V$,	121		479		479		ns
	SIp hold time (from SCKp↑) ^{Note 4}	tksi1	$\label{eq:2.7} \begin{array}{l} 2.7 \; V \leq E V_{DD0} \leq 3.6 \; V, 2.3 \; V \\ \\ C_b = 20 \; pF, R_b = 2.7 \; k\Omega \end{array}$	$V \le V_b \le 2.7 V$,	10		10		10		ns
	Delay time from $\overline{SCKp}\downarrow$ to SOp output Note 4	tkso1	$2.7 \text{ V} \leq EV_{DD0} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,		130		130		130	ns
	SIp setup time (to SCKp↓) ^{Note 5}	tsik1	$\label{eq:2.7} \begin{array}{l} 2.7 \; V \leq E V_{DD0} \leq 3.6 \; V, 2.3 \; V \\ \\ C_b = 20 \; pF, R_b = 2.7 \; k\Omega \end{array}$	$V \le V_b \le 2.7 V$,	3		110		110		ns
	SIp hold time (from SCKp↓) ^{Note 5}	tksi1	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 3.6 \text{ V}, 2.3 \text{ V}$ $C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$	$V \leq V_b \leq 2.7 V$,	10		10		10		ns
	Delay time from SCKp↑ to SOp output ^{Note 5}	tkso1	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 3.6 \text{ V}, 2.3 \text{ V}$ $C_{\text{b}} = 20 \text{ pF}, R_{\text{b}} = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,		10		10		10	ns

Correct:

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (TA = -40 to $+85^{\circ}$ C, 2.7 V \leq EV_{DD0} \leq V_{DD} \leq 3.6 V, Vss = EV_{SS0} = 0 V)

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Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t ксү1	$\label{eq:VDD} \begin{split} & 2.7 \; V \leq EV_{DD0} \leq 3.6 \; V, \\ & 2.3 \; V \leq V_b \leq 2.7 \; V, \\ & C_b = 20 \; pF, \; R_b = 2.7 \; k\Omega \end{split}$	tĸcyı ≥ 2/fcLĸ	300		1150		1150		ns
SCKp high-level width	tкнı	$\begin{split} 2.7 \; V &\leq E V_{DD0} \leq 3.6 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b &= 20 \; pF, \; R_b = 2.7 \; k\Omega \end{split}$		tксү1/2 – 120		tксү1/2 – 120		tксү1/2 – 120		ns
SCKp low-level width	t ĸ∟1	$\label{eq:V} \begin{split} 2.7 \; V &\leq E V_{DD0} \leq 3.6 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b &= 20 \; pF, \; R_b = 2.7 \; k\Omega \end{split}$		tксү1/2 – 10		tксү1/2 - 50		tксү1/2 - 50		ns
SIp setup time (to SCKp↑) ^{Note 4}	tsik1	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,	121		479		479		ns
SIp hold time (from SCKp↑) ^{Note 4}	tksi1	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,	10		10		10		ns
Delay time from $\overline{SCKp}\downarrow$ to SOp output Note 4	tkso1	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_{\text{b}} = 20 \text{ pF}, \text{R}_{\text{b}} = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,		130		130		130	ns
SIp setup time (to SCKp↓) ^{Note 5}	tsik1	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,	33		110		110		ns
SIp hold time (from SCKp↓) ^{Note 5}	tksi1	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,	10		10		10		ns
Delay time from <u>SCKp</u> ↑ to SOp output ^{Note 5}	tkso1	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6 \text{ V}, 2.3 \text{ V}$ $C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$	$V \le V_b \le 2.7 V$,		10		10		10	ns



Incorrect:

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, $\overline{SCKp...}$ internal clock output) (2/2) (Ta = -40 to +85°C, 1.8 V $\leq EV_{DD0} \leq V_{DD} \leq 3.6$ V, Vss = $EV_{SS0} = 0$ V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time	tsik1	$2.7 \; V \leq EV_{DD0} \leq 3.6 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, eq:delta_del$	81		479		479		ns
(to SCKp↑) Note 4		$C_{\rm b}=30~pF,R_{\rm b}=2.7~k\Omega$							
		$ \begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\mbox{Note } 6}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array} $	177		479		479		ns
SIp hold time (from SCKp↑) ^{Note 4}	tksi1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	19		19		19		ns
		$\begin{array}{l} 1.8 \ V \leq EV_{\text{DD0}} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 6}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$	19		19		19		ns
Delay time from $\overline{SCKp}\downarrow$ to SOp output Note 4	tkso1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		100		100		100	ns
		$ \begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 6}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array} $		195		195		195	ns
SIp setup time (to SCKp↓) ^{Note 5}	tsik1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	44		110		110		ns
		$\begin{array}{l} 1.8 \ V \leq EV_{\text{DD0}} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 6}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$	44		110		110		ns
SIp hold time (from $\overline{SCKp}\downarrow$) Note 5	tksi1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	19		19		19		ns
		$ \begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 6}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array} $	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 5	tkso1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		25		25		25	ns
		$ \begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 6}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array} $		25		25		25	ns



Correct:

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, 5	SCKp internal clock output) (2/2)
$(T_A = -40 \text{ to } +85^{\circ}C, 1.8 \text{ V} \le EV_{DD0} \le V_{DD} \le 3.6 \text{ V}, \text{ Vss} = EV_{SS0} = 0 \text{ V})$	

Parameter	Symbol	Conditions	HS Note 1		LS	Note 2	LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time	tsik1	$2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V,$	177		479		479		ns
(to SCKp ⁺) ¹⁰⁰⁰		C_b = 30 pF, R_b = 2.7 k Ω							
		$ \begin{array}{l} 1.8 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V & \mbox{Note 6}, \\ C_b = 30 \; pF, \; R_b = 5.5 \; k\Omega \end{array} $	479		479		479		ns
SIp hold time (from SCKp↑) ^{Note 4}	tksi1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	19		19		19		ns
		$ \begin{array}{l} 1.8 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V^{\text{Note 6}}, \\ C_b = 30 \; pF, \; R_b = 5.5 \; k\Omega \end{array} $	19		19		19		ns
Delay time from $\overline{SCKp}\downarrow$ to SOp output Note 4	tkso1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		195		195		195	ns
		$\begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\mbox{Note } 6}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$		483		483		483	ns
Slp setup time (to SCKp↓) ^{Note 5}	tsiĸ1	$\begin{array}{l} 2.7 \; V \leq EV_{DD0} \leq 3.6 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 30 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	44		110		110		ns
		$ \begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\mbox{Note } 6}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array} $	110		110		110		ns
SIp hold time (from SCKp↓) ^{Note 5}	tksi1	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \leq 3.6 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	19		19		19		ns
		$ \begin{array}{l} 1.8 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V^{\text{Note 6}}, \\ C_b = 30 \; pF, \; R_b = 5.5 \; k\Omega \end{array} $	19		19		19		ns
Delay time from <u>SCKp</u> ↑ to SOp output ^{Note 5}	tkso1	$\begin{array}{l} 2.7 \; V \leq EV_{DD0} \leq 3.6 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 30 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		25		25		25	ns
		$ \begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 6}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array} $		25		25		25	ns



13. 29.6.1 A/D converter characteristics **Addition**:

When AV_{REF(+)}= AV_{REFP}/ANI0(ADREFP1 = 0, ADREFP0 = 1), AV_{REF(-)}= AV_{REFM}/ANI1(ADREFM = 1), target pin:ANI2-ANI12

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.7 \le \text{AV}_{\text{REFP}} \le \text{AV}_{\text{DD}} \le \text{V}_{\text{DD}} \le 3.6\text{V}, \text{V}_{\text{SS}} = 0\text{V}, \text{AV}_{\text{SS}} = 0\text{V}, \text{Reference voltage}(+) = \text{AV}_{\text{REFP}}, \text{Reference voltage}(-) = \text{AV}_{\text{REFM}} = 0\text{V}, \text{HALT mode})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R _{ES}				12	bit
Overall error Note1,2,3	AINL	12bit resolution		±1.7	±3.3	LSB
Conversion time	T _{CONV}	ADTYP=0, 12bit resolution	3.375			μs
Zero-scale error Note1,2,3	E _{zs}	12bit resolution		±1.3	±3.2	LSB
Full-scale error Note1,2,3	E _{FS}	12bit resolution		±0.7	±2.9	LSB
Integral linearity error Note1,2,3	ILE	12bit resolution		±1.0	±1.4	LSB
Differential linearity error Note1,2,3	DLE	12bit resolution		±0.9	±1.2	LSB
Analog input voltage	V _{AIN}		0		AV_{REFP}	V

Notes 1: TYP. Value is the average value AV_{DD} = AV_{REFP} = 3V, T_A = 25 \ ^{\circ}C.

MAX. Values are mean $\pm 3\sigma$ in normal distribution.

2: This value based on the characterization results, is not subject to production testing.

3: Excludes quantization error ($\pm 1/2$ LSB).

Caution 1. Attention must be paid to noise input to each power supply and ground lines.

The reference voltage line of AV_{REFP} is separated from the other power supply lines for noise countermeasures. Caution 2. Please make sure that pulses whose voltage suddenly change, such as digital pulses, are not input or output to a pin adjacent to the pin whose value is being A/D converted and P20 to P27, P150 to P154.



Date: Sep. 24, 2013

Incorrect:	Correct:
14. 30.3.1 Pin characteristics ($T_A = -40$ to +105°C, 2.4 V ≤ AV _{DD} ≤ V _{DD} ≤ 3.6 V, 2.4 V ≤ EV _{DD0} ≤ V _{DD} ≤ 3.6 V, V _{SS} = EV _{SS0} = 0	
V) Note 3. Specification under output current where the duty ≤ 70%. The output current value that has changed the duty ratio lower than 70% can be calculated with the following expression (when changing the duty ratio to n%).	Note 3. Specification under conditions where the duty factor \leq 70%. The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{AV}_{\text{DD}} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0$	
Note 3. Specification under output current where the duty \leq 70%. The output current value that has changed the duty ratio lower than 70% can can be calculated with the following expression (when changing the duty ratio to n%).	Note 3. Specification under conditions where the duty factor \leq 70%. The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
15. 30.4 AC Characteristics	
$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le AV_{DD} \le 3.6 \text{ V}, 2.4 \text{ V} \le EV_{DD0} \le V_{DD} \le 3.6 \text{ V}, \text{ Vss} = EV_{SS0} = 0 \text{ V})$	(T _A = −40 to +105°C, $AV_{DD} \le V_{DD} \le 3.6$ V, 2.4 V ≤ EV _{DD0} ≤ V _{DD} ≤ 3.6 V, V _{SS} = EV _{SS0} = 0 V)

