Date: Oct. 31, 2023

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0128A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G24 Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G24 Group	Lot No. All lots	Reference Document	RL78/G24 User's Manual: Hardware Rev. 1.00 R01UH0961EJ0100 (Apr 28, 2023)		

This document describes misstatements found in the RL78/G24 User's Manual: Hardware Rev. 1.00 (R01UH0961EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
7.5.4 Examples of register settings for port and alternate functions	Page 317	Incorrect descriptions revised
10.6.3 Cautions on channel output operation	Page 455	Incorrect descriptions revised
12.2 Configuration of Timer RD2	Page 536	Incorrect descriptions revised
12.3.4 Timer RD timer-KB PWM output gating mode control register (TRDBCR)	Page 541	Incorrect descriptions revised
12.6 Timer RD2 Interrupts	Page 679	Incorrect descriptions revised
20.3.4 A/D converter mode register 1 (ADM1)	Page 1095	Incorrect descriptions revised
20.3.10 Analog input channel specification registers n for advanced mode (ADSn) (n = 0 to 3)	Page 1107	Caution added
20.3.15 A/D conversion sampling mode specification register (ADSPMOD)	Page 1112	Caution added
24.5.3 Master transmission/reception	Page 1289	Incorrect descriptions revised
24.5.7 SNOOZE mode function	Page 1321	Incorrect descriptions revised
25.5.16 Communication operations	Page 1442	Incorrect descriptions revised
43.3.2 Supply current characteristics 44.3.2 Supply current characteristics	Page 1861 Page 1940	Incorrect descriptions revised
43.6.1 A/D converter characteristics	Page 1904	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0961EJ0100	
1	7.5.4 Examples of register settings for port and alternate functions		Page 317	Page 3
2	10.6.3 Cautions on channel output operation		Page 455	Page 4
3	12.2 Configuration of Timer RD2		Page 536	Page 5
4	12.3.4 Timer RD timer-KB PWM output gating mode control register (TRDBCR)		Page 541	Page 6
5	12.6 Timer RD2 Interrupts		Page 679	Page 7
6	20.3.4 A/D converter mode register 1 (ADM1)		Page 1095	Page 8
7	20.3.10 Analog input channel specification registers n for advanced mode (ADSn) (n = 0 to 3)		Page 1107	Page 9
8	20.3.15 A/D conversion sampling mode specification register (ADSPMOD)		Page 1112	Page 10
9	24.5.3 Master transmission/reception		Page 1289	Page 11
10	24.5.7 SNOOZE mode function		Page 1321	Page 12
11	25.5.16 Communication operations		Page 1442	Page 13
12	43.3.2 Supply current characteristics 44.3.2 Supply current characteristics		Page 1861 Page 1940	Page 14
13	43.6.1 A/D converter characteristics		Page 1904	Page 15

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G24 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0128A/E	Oct. 31, 2023	First edition issued Corrections No.1 to No.13 revised (this document)

1. **7.5.4 Examples of register settings for port and alternate functions (Page 317)**

Incorrect:

Table 7 - 5 Examples of Register and Output Latch Settings for Alternate Functions (19/22)

Pin Name	Function Used		PIORx	POMxx	PMxx	PMCAxx	Pxx	Alternate Function Output		20-pin	24-pin	25-pin	30-pin	32-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O						SAU and DALI	Other Than SAU and DALI										
P120	P120	Input	—	—	0	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	—	TO02 = 0Note										
	ANI19	Analog input	—	—	1	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IVCMP0	Analog input	—	—	1	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PGAI0	Analog input	—	—	1	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(TI02)	Input	PIOR36 = 1Note	—	0	1	×	—	×	✓	✓	✓	✓	✓	—	—	—	—	—
	(TO02)	Output	PIOR36 = 1Note	—	0	0	0	—	×	✓	✓	✓	✓	✓	—	—	—	—	—
	TRGIDZ	Input	—	—	0	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRGTRG	Input	—	—	0	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note This setting is only applicable in the 20- to 32-pin products.

Correct:

Table 7 - 5 Examples of Register and Output Latch Settings for Alternate Functions (19/22)

Pin Name	Function Used		PIORx	POMxx	PMCAxx	PMxx	Pxx	Alternate Function Output		20-pin	24-pin	25-pin	30-pin	32-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O						SAU and DALI	Other Than SAU and DALI										
P120	P120	Input	—	—	0	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	—	TO02 = 0Note										
	ANI19	Analog input	—	—	1	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IVCMP0	Analog input	—	—	1	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PGAI0	Analog input	—	—	1	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(TI02)	Input	PIOR36 = 1Note	—	0	1	×	—	×	✓	✓	✓	✓	✓	—	—	—	—	—
	(TO02)	Output	PIOR36 = 1Note	—	0	0	0	—	×	✓	✓	✓	✓	✓	—	—	—	—	—
	TRGIDZ	Input	—	—	0	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRGTRG	Input	—	—	0	1	×	—	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

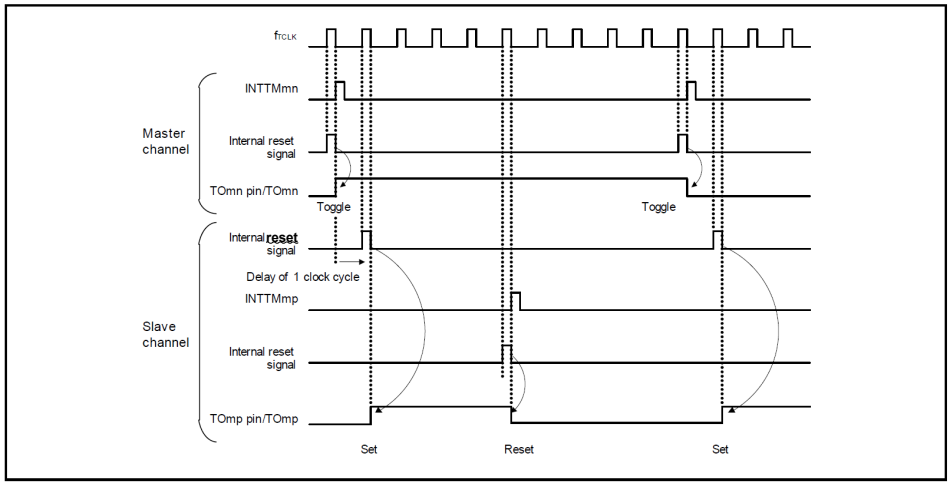
Note This setting is only applicable in the 20- to 32-pin products.

2. 10.6.3 Cautions on channel output operation (Page 455)

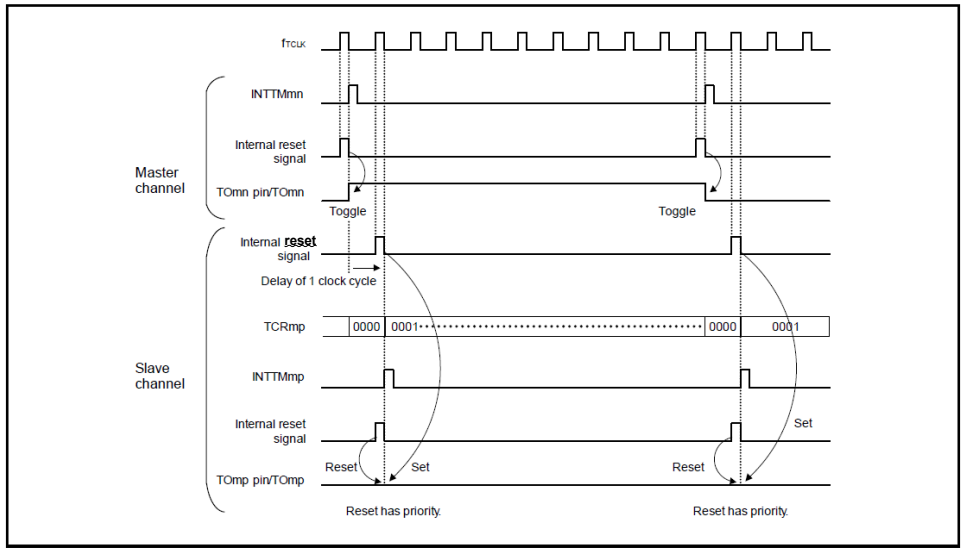
Incorrect:

Figure 10 - 36 States of Operation following Set and Reset Signals

1. Basic timing during operation



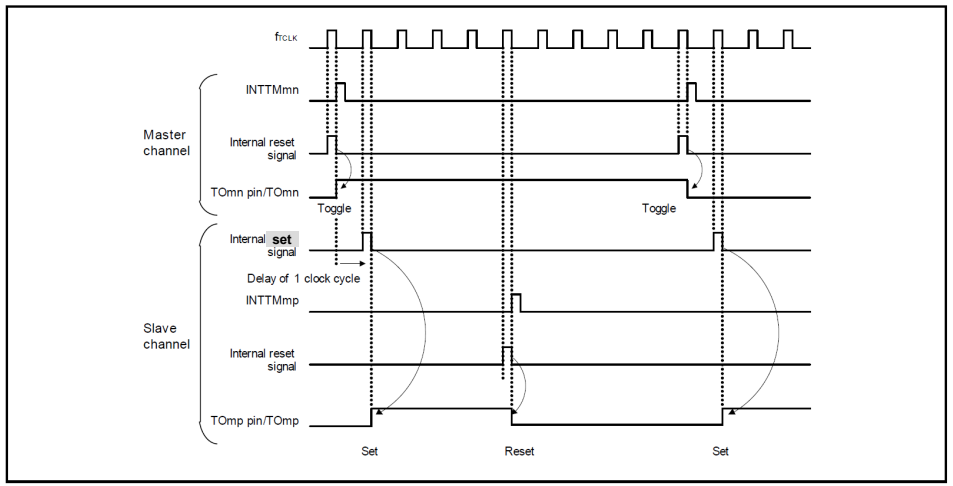
2. Timing during operation with the duty cycle set to 0%



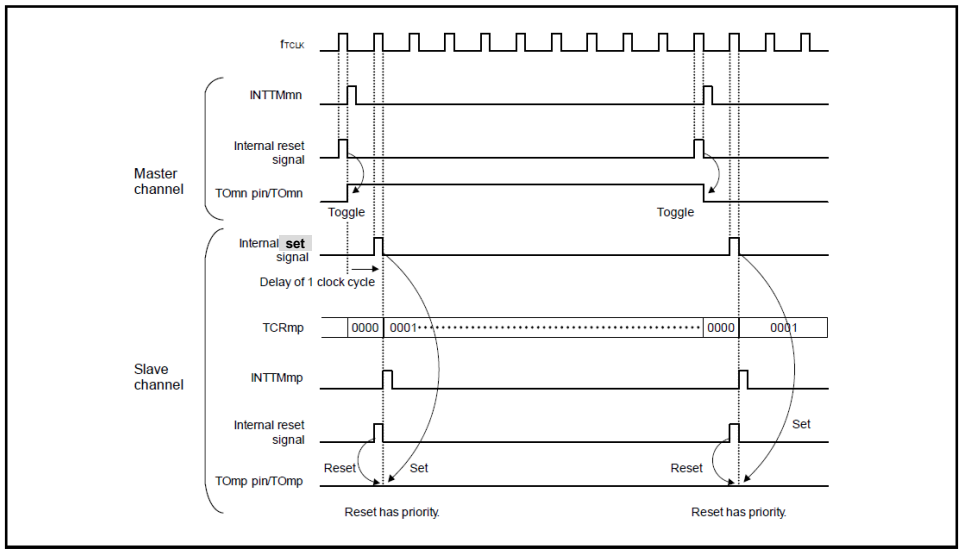
Correct:

Figure 10 - 36 States of Operation following Set and Reset Signals

1. Basic timing during operation



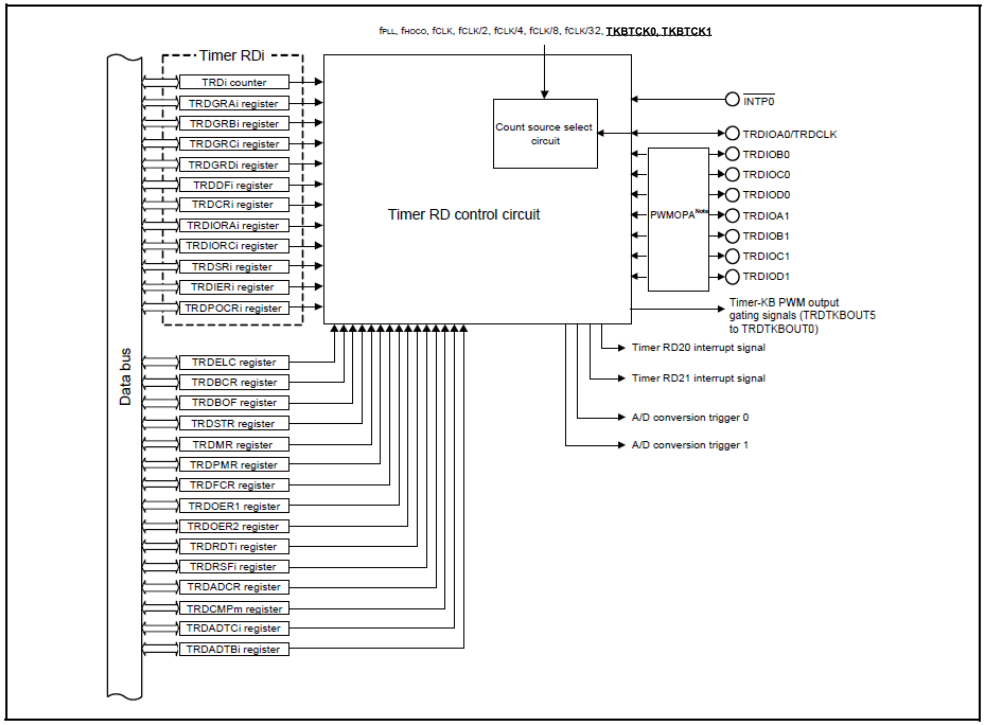
2. Timing during operation with the duty cycle set to 0%



3. 12.2 Configuration of Timer RD2 (Page 536)

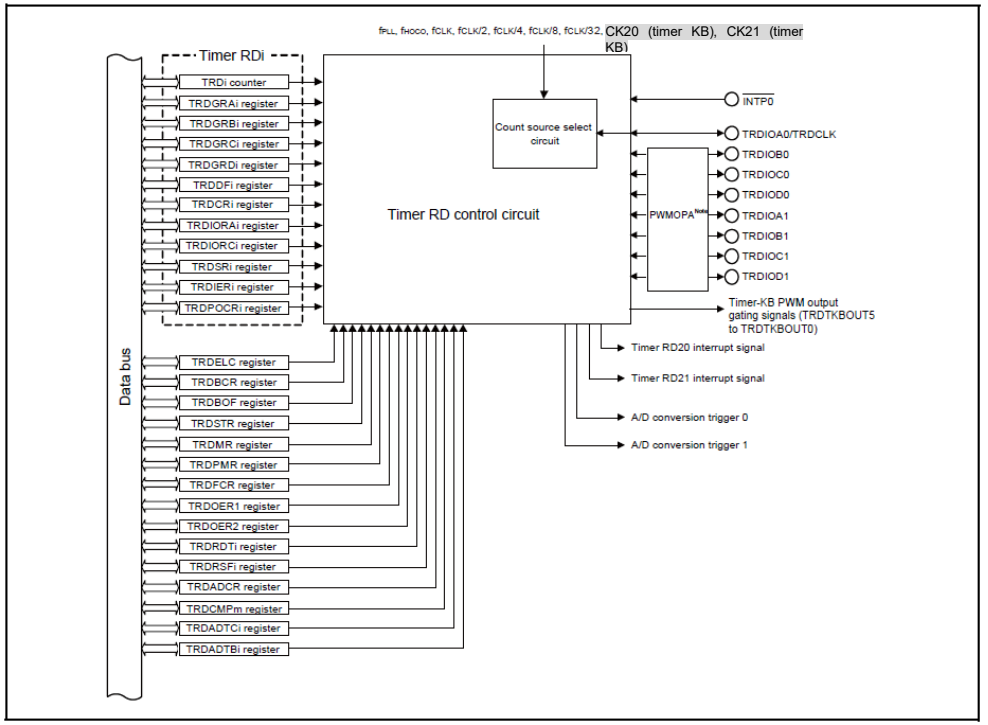
Incorrect:

Figure 12 - 1 Block Diagram of Timer RD2



Correct:

Figure 12 - 1 Block Diagram of Timer RD2



4. 12.3.4 Timer RD timer-KB PWM output gating mode control register (TRDBCR) (Page 541)

Incorrect:

12.3.4 Timer RD timer-KB PWM output gating mode control register (TRDBCR)

Figure 12 - 5 Format of Timer RD Timer-KB PWM Output Gating Mode Control Register (TRDBCR)

Address: F0391H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
TRDBCR	GCE	0	0	GCKS	0	0	0	GMD

GCE	Enabling timer-KB PWM output gating mode
0	Timer-KB PWM output gating mode is disabled.
1	Timer-KB PWM output gating mode is enabled.

GCKS	Selecting the count source for timer-KB PWM output gating mode
0	**TKBTCK0 is selected.**
1	**TKBTCK1 is selected.**

GMD	Selecting the operation in timer-KB PWM output gating mode
0	Standalone mode
1	Timer KB3 interlocked mode

Correct:

12.3.4 Timer RD timer-KB PWM output gating mode control register (TRDBCR)

Figure 12 - 5 Format of Timer RD Timer-KB PWM Output Gating Mode Control Register (TRDBCR)

Address: F0391H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
TRDBCR	GCE	0	0	GCKS	0	0	0	GMD

GCE	Enabling timer-KB PWM output gating mode
0	Timer-KB PWM output gating mode is disabled.
1	Timer-KB PWM output gating mode is enabled.

GCKS	Selecting the count source for timer-KB PWM output gating mode
0	The CK20 operating clock for timer KB3 is selected.
1	The CK21 operating clock for timer KB3 is selected.

GMD	Selecting the operation in timer-KB PWM output gating mode
0	Standalone mode
1	Timer KB3 interlocked mode

5. 12.6 Timer RD2 Interrupts (Page 679)

Incorrect:

12.6 Timer RD2 Interrupts

When timer RD2 is not set to extended complementary PWM mode or timer-KB PWM output gating mode, timer RD2 generates a timer RD2i (i = 0 or 1) interrupt request from six sources each for timer RD20 and timer RD21. **Table 12 - 28** lists the registers associated with timer RD2 interrupts and **Figure 12 - 109** shows a block diagram of the timer RD2 interrupt section.

Table 12 - 28 Registers Associated with Timer RD2 Interrupts

	Timer RD Status Register	Timer RD Interrupt Enable Register	Interrupt Request Flag (Register)	Interrupt Mask Flag (Register)	Priority Specification Flag (Register)
Timer RD20	TRDSR0	TRDIER0	TRDIF0**(IF2H)**	TRDMK0 **(MK2H)**	TRDPR00**(PR02H)** TRDPR10**(PR12H)**
Timer RD21	TRDSR1	TRDIER1	TRDIF1**(IF2H)**	TRDMK1 **(MK2H)**	TRDPR01**(PR02H)** TRDPR11 **(PR12H)**

Correct:

12.6 Timer RD2 Interrupts

When timer RD2 is not set to extended complementary PWM mode or timer-KB PWM output gating mode, timer RD2 generates a timer RD2i (i = 0 or 1) interrupt request from six sources each for timer RD20 and timer RD21. **Table 12 - 28** lists the registers associated with timer RD2 interrupts and **Figure 12 - 109** shows a block diagram of the timer RD2 interrupt section.

Table 12 - 28 Registers Associated with Timer RD2 Interrupts

	Timer RD Status Register	Timer RD Interrupt Enable Register	Interrupt Request Flag (Register)	Interrupt Mask Flag (Register)	Priority Specification Flag (Register)
Timer RD20	TRDSR0	TRDIER0	TRDIF0 (IF1H)	TRDMK0 (MK1H)	TRDPR00 (PR01H) TRDPR10 (PR11H)
Timer RD21	TRDSR1	TRDIER1	TRDIF1 (IF1H)	TRDMK1 (MK1H)	TRDPR01 (PR01H) TRDPR11 (PR11H)

6. 20.3.4 A/D converter mode register 1 (ADM1) (Page 1095)

Incorrect:

Figure 20 - 7 Format of A/D Converter Mode Register 1 (ADM1)

Address: FFF32H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	ADLSP	ADTRS2	ADTRS1	ADTRS0

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger no-wait mode or software trigger wait mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

ADLSP	fCLK input frequency setting
0	4 MHz < fCLK ≤ 48 MHz
1	1 MHz ≤ fCLK ≤ 4 MHz

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS2	ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	0	Channel 01 timer array unit counting or capture end interrupt signal (INTTM01)
0	1	0	Realtime clock interrupt signal (INTRTC)
0	1	1	32-bit interval timer channel 0 interrupt signal (ELCITL0)
1	0	0	Event input from the ELCNote
Setting values other than the above is prohibited.			

Note Event input from the ELC cannot be used in the SNOOZE mode.

Caution 1. **Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).**

Caution 2. **To complete A/D conversion, specify at least the following time as the hardware trigger interval:**
Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time
Hardware trigger wait mode: 2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time

Caution 3. **In modes other than SNOOZE mode, input of the next INTRTC or ELCITL0 will not be recognized as a valid hardware trigger for up to four cycles of the fCLK clock after the first INTRTC or ELCITL0 is input.**

Caution 4. **The settings of the ADTMD[1:0] and ADTRS[2:0] bits are only effective when the advanced mode is disabled. Do not change their values from the initial values when the advanced mode is enabled.**

Caution 5. **When the advanced mode is enabled, selecting the sequential conversion mode is prohibited. Do not change the ADSCM bit from the initial value (one-shot conversion mode).**

Correct:

Figure 20 - 7 Format of A/D Converter Mode Register 1 (ADM1)

Address: FFF32H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	ADLSP	ADTRS2	ADTRS1	ADTRS0

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger no-wait mode or software trigger wait mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

ADLSP	fCLK input frequency setting
0	4 MHz < fCLK ≤ 48 MHz
1	1 MHz ≤ fCLK ≤ 4 MHz

ADSCM	Specification of the A/D conversion modeNote 1
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS2	ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	0	Channel 01 timer array unit counting or capture end interrupt signal (INTTM01)
0	1	0	Realtime clock interrupt signal (INTRTC)
0	1	1	32-bit interval timer channel 0 interrupt signal (ELCITL0)
1	0	0	Event input from the ELCNote 2
Setting values other than the above is prohibited.			

Note 1. When the advanced mode is enabled, selecting the sequential conversion mode is prohibited. Set the ADSCM bit to 1 (one-shot conversion mode).

Note 2. Event input from the ELC cannot be used in the SNOOZE mode.

Caution 1. **Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).**

Caution 2. **To complete A/D conversion, specify at least the following time as the hardware trigger interval:**
Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time
Hardware trigger wait mode: 2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time

Caution 3. **In modes other than SNOOZE mode, input of the next INTRTC or ELCITL0 will not be recognized as a valid hardware trigger for up to four cycles of the fCLK clock after the first INTRTC or ELCITL0 is input.**

Caution 4. **The settings of the ADTMD[1:0] and ADTRS[2:0] bits are only effective when the advanced mode is disabled. Do not change their values from the initial values when the advanced mode is enabled.**

7. 20.3.10 Analog input channel specification registers n for advanced mode (ADSn) (n = 0 to 3) (Page 1107)

Incorrect:

Caution 1. When the setting of the ADSPSCn[1:0] bits is 10B or 11B, do not change the settings of the ADISSn and ADSn[4:0] bits from the initial values.
Caution 2. Do not set the same value to the ADSPSCn[1:0] bits of the ADS0 to ADS3 registers. Note, however, that setting of 00B is always allowed. Set the ADSPSCn[1:0] bits to 00B unless the simultaneous sampling is to be used.
Caution 3. Only rewrite the values of the ADISSn and ADSPSCn[1:0] bits while conversion operation is stopped (ADCS = 0, ADCE = 0).
Caution 4. Do not rewrite the value of the ADSn[4:0] bits during A/D conversion. Only rewrite it while conversion operation is stopped (ADCS = 0, ADCE = 0).
Caution 5. Set the port that is specified as the analog input by the port mode control A register xx (PMCAxx) to the input mode by using the corresponding port mode register xx (PMxx).
Caution 6. When specifying an input channel by the ADSn register, do not select the pin that is specified as digital I/O by the port mode control A register xx (PMCAxx).

Correct:

Caution 1. When the setting of the ADSPSCn[1:0] bits is 10B or 11B, do not change the settings of the ADISSn and ADSn[4:0] bits from the initial values.
Caution 2. Do not set the same value to the ADSPSCn[1:0] bits of the ADS0 to ADS3 registers. Note, however, that setting of 00B is always allowed. Set the ADSPSCn[1:0] bits to 00B unless the simultaneous sampling is to be used.
Caution 3. Before rewriting the value of the ADSn register, take measures such as disabling the corresponding hardware trigger to prevent the triggering of A/D conversion. Alternatively, discard the result of the first conversion after having rewritten the given register and use the second and subsequent results.
Caution 4. Set the port that is specified as the analog input by the port mode control A register xx (PMCAxx) to the input mode by using the corresponding port mode register xx (PMxx).
Caution 5. When specifying an input channel by the ADSn register, do not select the pin that is specified as digital I/O by the port mode control A register xx (PMCAxx).

8. 20.3.15 A/D conversion sampling mode specification register (ADSPMOD) (Page 1112)

Incorrect:

Note • This setting is only allowed in normal mode 1.
• Do not set ADSPMOD[1:0] to 01B when any of the following analog input channel is specified in the ADSn register enabled by the ADSCTL register.
– ANI16 to ANI30
– PGA output
– Temperature sensor output voltage
– Internal reference voltage

Caution **Only rewrite the value of the ADSPMOD register while conversion operation is stopped (ADCS = 0, ADCE = 0).**

Correct:

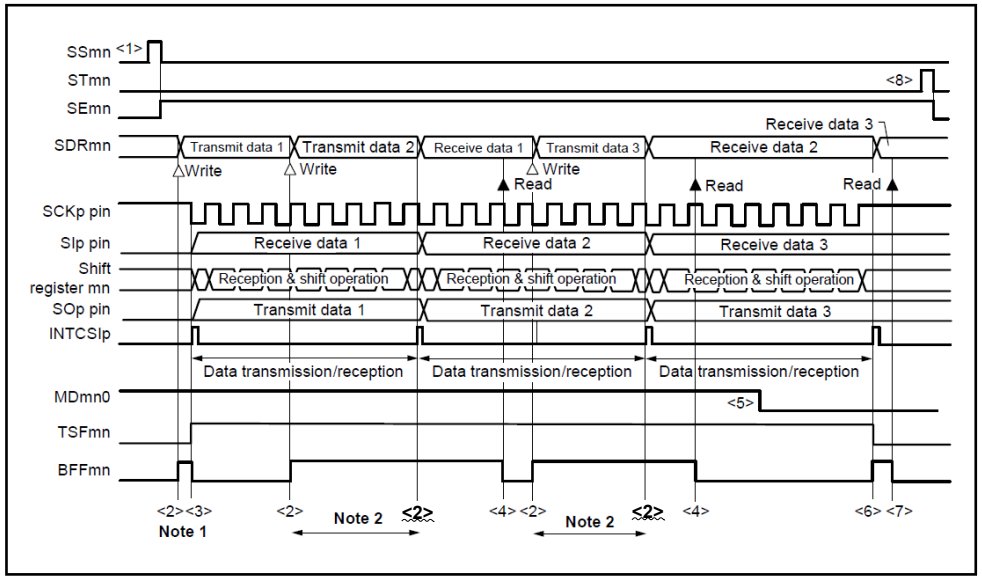
Note • This setting is only allowed in normal mode 1.
• Do not set ADSPMOD[1:0] to 01B when any of the following analog input channel is specified in the ADSn register enabled by the ADSCTL register.
– ANI16 to ANI30
– PGA output
– Temperature sensor output voltage
– Internal reference voltage

Caution **Do not rewrite the value of the ADSPMOD register during A/D conversion. Also, before rewriting the value, take measures such as disabling the corresponding hardware trigger to prevent the triggering of A/D conversion while the A/D converter is in the conversion standby state.**

9. 24.5.3 Master transmission/reception (Page 1289)

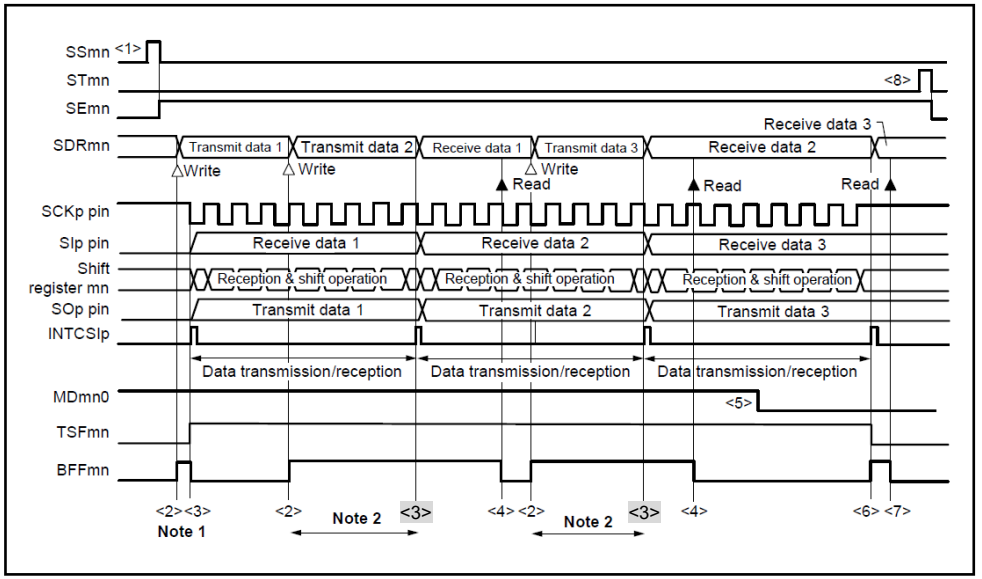
Incorrect:

Figure 24 - 48 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Correct:

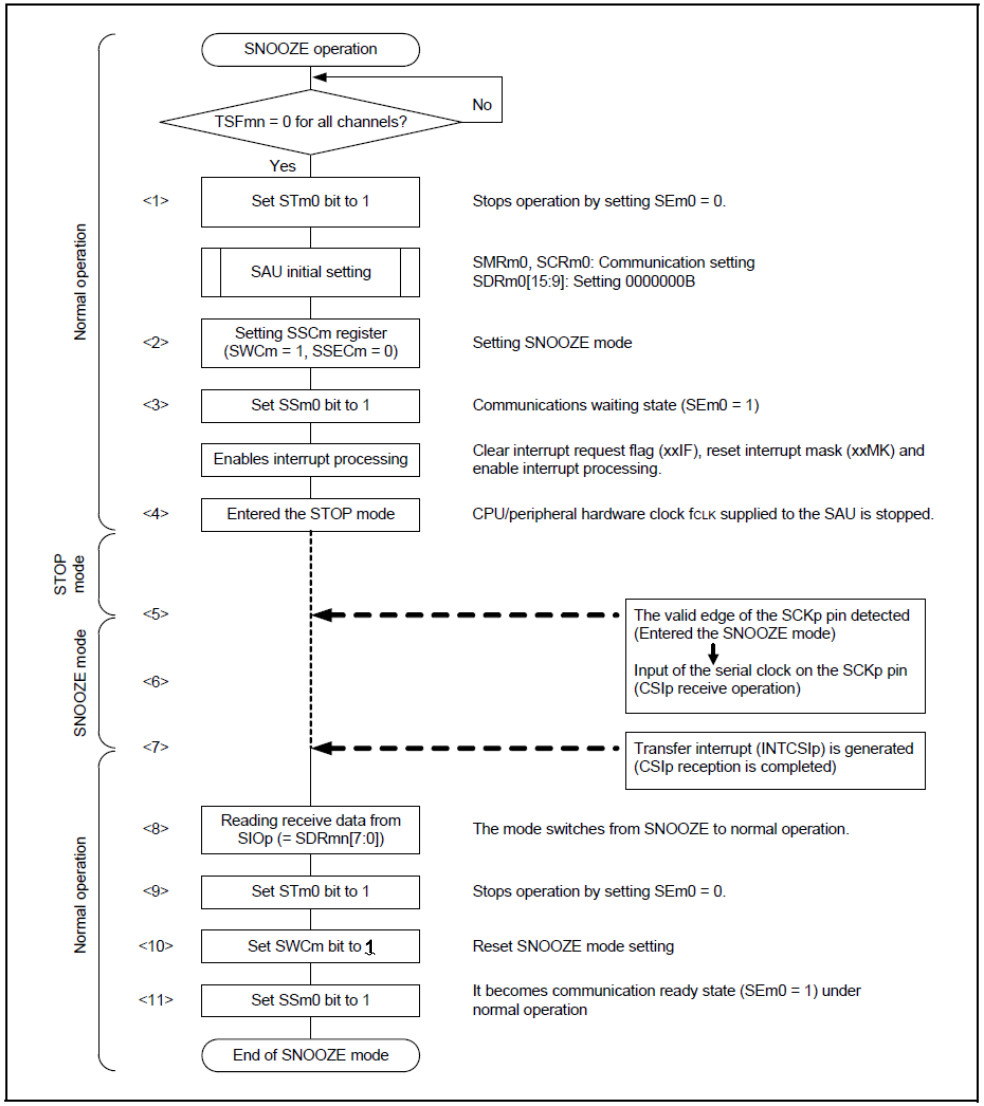
Figure 24 - 48 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



10. 24.5.7 SNOOZE mode function (Page 1321)

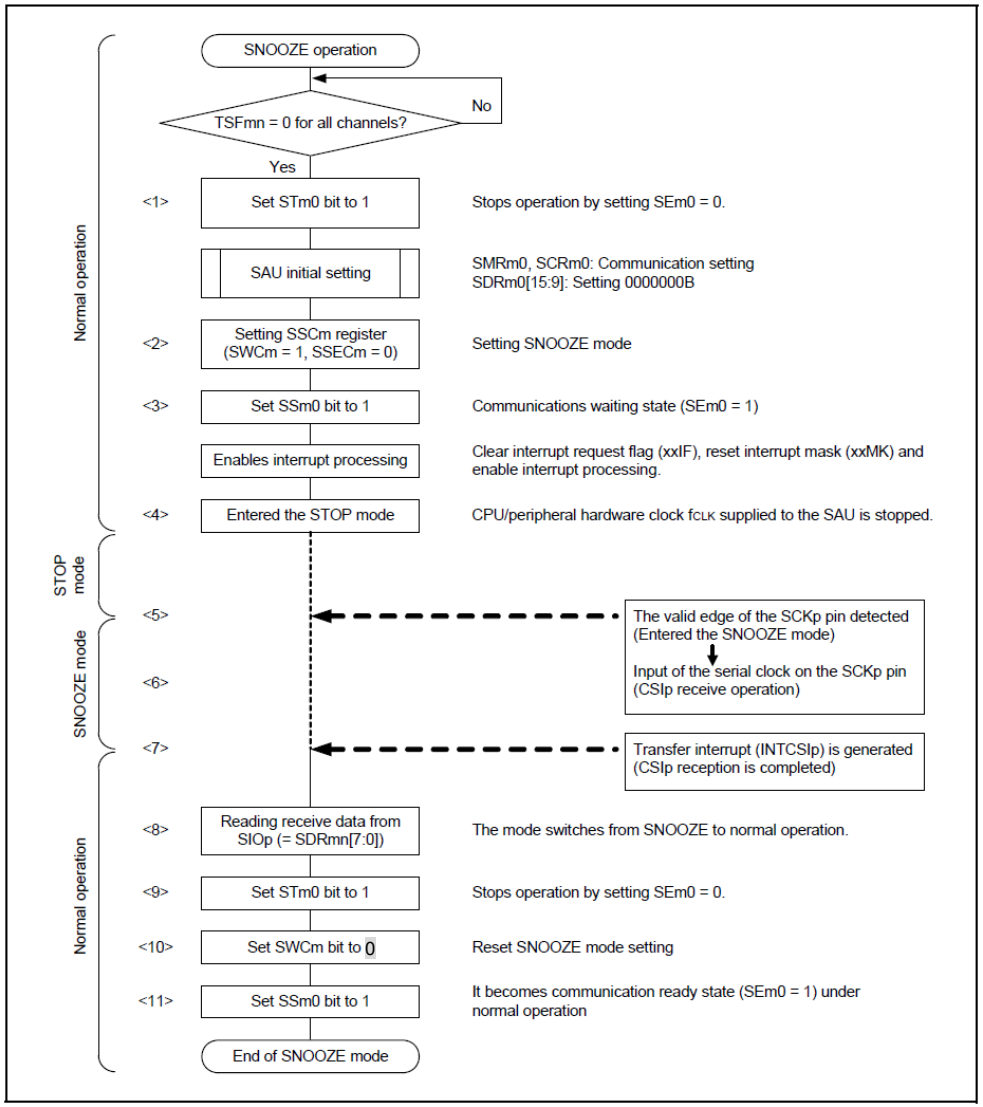
Incorrect:

Figure 24 - 73 Flowchart of SNOOZE Mode Operation (once startup)



Correct:

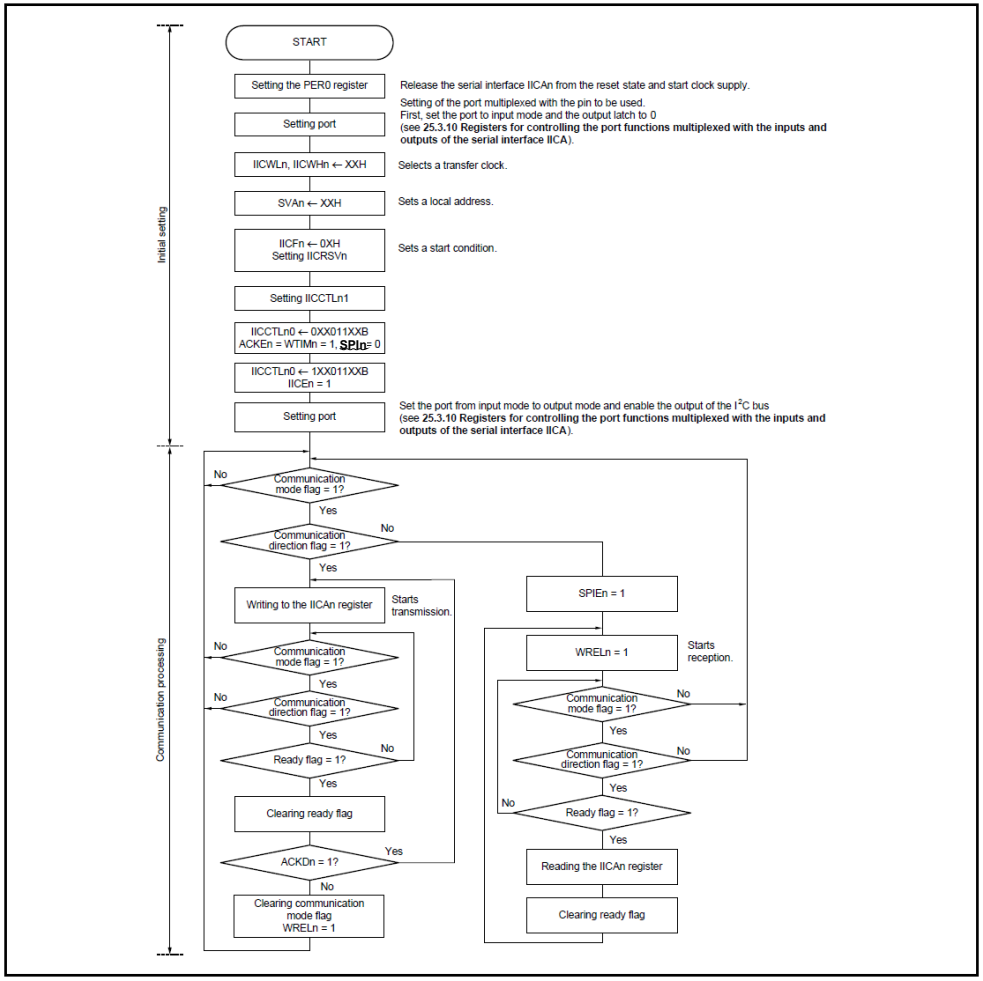
Figure 24 - 73 Flowchart of SNOOZE Mode Operation (once startup)



11. 25.5.16 Communication operations (Page 1442)

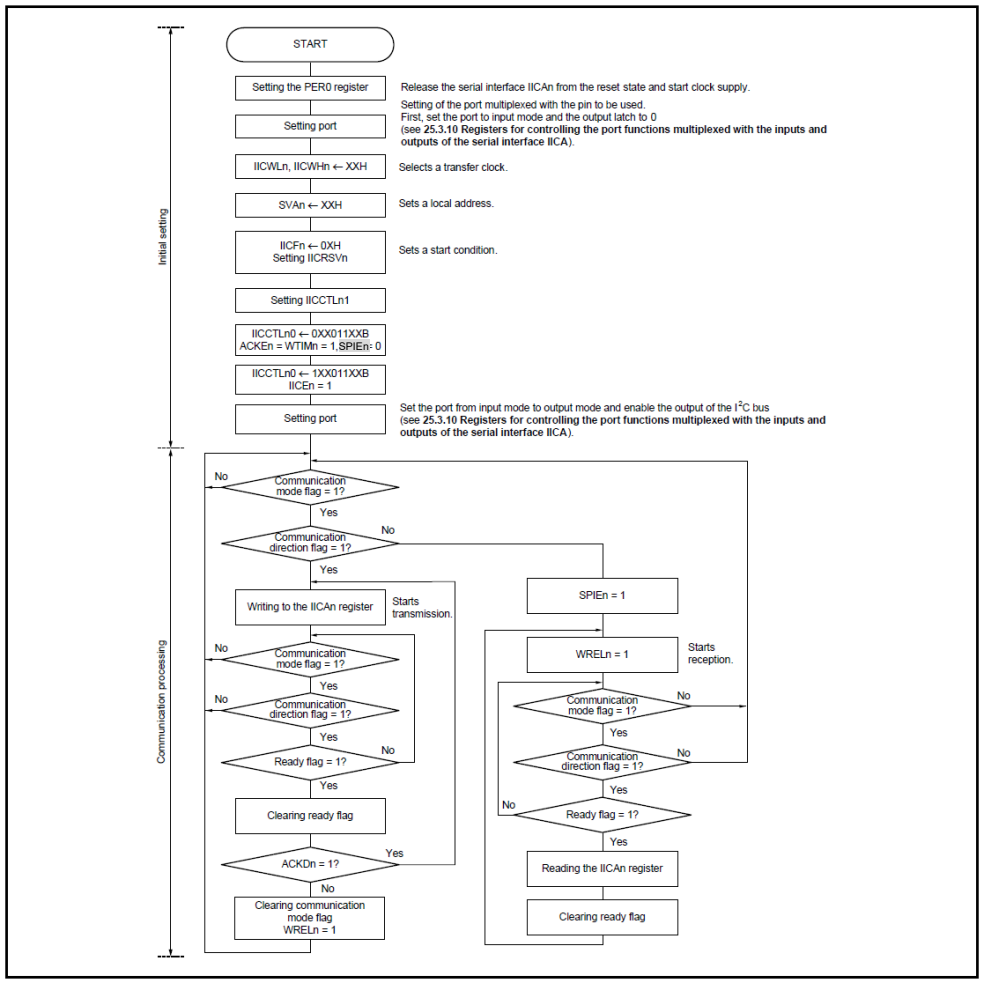
Incorrect:

Figure 25 - 31 Slave Operation Flowchart (1)



Correct:

Figure 25 - 31 Slave Operation Flowchart (1)



12. 43.3.2 Supply current characteristics (Page 1861) 44.3.2 Supply current characteristics (Page 1940)

Incorrect:

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} Note 1	HIPREC = 0			380	—	μA
		HIPREC = 1			240	—	μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1				20	—	μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.3	—	μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz			0.005	—	μA
		f_{RTCCLK} = 128 Hz			0.002	—	μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.04	—	μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 32.768 kHz (typ.)			0.32	—	μA
A/D converter operating current	I_{ADC} Notes 1, 6	Conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		0.95	1.6	mA
			Low-voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.54	0.81	mA
AV_{REFP} current	I_{ADREF} Note 7	AV_{REFP} = 5.0 V			60	—	μA
A/D converter internal reference voltage current	I_{ADREF} Note 1				114	—	μA
Temperature sensor operating current	I_{TMPS} Note 1				110	—	μA
D/A converter operating current	I_{DAC} Notes 1, 8	Per channel	10-bit DAC, V_{DD} = 5.0 V		223	—	μA
			8-bit DAC, V_{DD} = 5.0 V		120	—	μA
Comparator operating current	I_{CMP} Notes 1, 9	Per channel			100	—	μA
PGA operating current	I_{PGA} Notes 1, 10				460	—	mA
Sample & hold circuit operating current	I_{SH} Notes 1, 11	Per channel			800	—	μA
LVD operating current	I_{LVD0} Notes 1, 12				0.03	—	μA
	I_{LVD1} Notes 1, 12				0.03	—	μA
FAA operating current	I_{FAA} Notes 1, 13	f_{CLK} = 48 MHz			11.0	—	mA
		f_{CLK} = 32 MHz			7.3	—	mA

Correct:

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} Note 1	HIPREC = 0			380	—	μA
		HIPREC = 1			240	—	μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1				20	—	μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.3	—	μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz			0.005	—	μA
		f_{RTCCLK} = 128 Hz			0.002	—	μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.04	—	μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 32.768 kHz (typ.)			0.32	—	μA
A/D converter operating current	I_{ADC} Notes 1, 6	Conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		0.95	1.6	mA
			Low-voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.54	0.81	mA
AV_{REFP} current	I_{ADREF} Note 7	AV_{REFP} = 5.0 V			60	—	μA
A/D converter internal reference voltage current	I_{ADREF} Note 1				114	—	μA
Temperature sensor operating current	I_{TMPS} Note 1				110	—	μA
D/A converter operating current	I_{DAC} Notes 1, 8	Per channel	10-bit DAC, V_{DD} = 5.0 V		223	—	μA
			8-bit DAC, V_{DD} = 5.0 V		120	—	μA
Comparator operating current	I_{CMP} Notes 1, 9	Per channel			100	—	μA
PGA operating current	I_{PGA} Notes 1, 10				460	—	μA
Sample & hold circuit operating current	I_{SH} Notes 1, 11	Per channel			800	—	μA
LVD operating current	I_{LVD0} Notes 1, 12				0.03	—	μA
	I_{LVD1} Notes 1, 12				0.03	—	μA
FAA operating current	I_{FAA} Notes 1, 13	f_{CLK} = 48 MHz			11.0	—	mA
		f_{CLK} = 32 MHz			7.3	—	mA

13. 43.6.1 A/D converter characteristics (Page 1904)

Incorrect:

43.6 Analog Characteristics

43.6.1 A/D converter characteristics

1. Normal modes 1 and 2

(T_A = –40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, f_{CLK} ≤ 32 MHz,
reference voltage (+) = AV_{REFP} (ADREFP[1:0] = 01B), reference voltage (–) = AV_{REFM} (ADREFM = 1),
target pins: ANI2 to ANI7, ANI16 to ANI30, internal reference voltage, and temperature sensor output voltage)

Item	Symbol		Conditions	Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		32	MHz
Overall error Notes 1, 3, 4, 5	AINL		4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 6	t_{CONV}	ADM3.ADVMOD=0	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2			µs
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2			µs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2			µs
		ADM3.ADVMOD=1	4.5V ≦ AV_{REFP} = VDD ≦ 5.5V	1			µs
			2.7V ≦ AV_{REFP} = VDD ≦ 5.5V	1			µs
			2.4V ≦ AV_{REFP} = VDD ≦ 5.5V	1			µs
Zero-scale error Notes 1, 2, 3, 4, 5	E_{ZS}		4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 5	E_{FS}		4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error Notes 1, 4, 5	ILE		4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE		4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Correct:

43.6 Analog Characteristics

43.6.1 A/D converter characteristics

1. Normal modes 1 and 2

(T_A = –40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, f_{CLK} ≤ 32 MHz,
reference voltage (+) = AV_{REFP} (ADREFP[1:0] = 01B), reference voltage (–) = AV_{REFM} (ADREFM = 1),
target pins: ANI2 to ANI7, ANI16 to ANI30, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	f_{AD}		1		32	MHz
Overall error Notes 1, 3, 4, 5	AINL	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 6	t_{CONV}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2			µs
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2			µs
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2			µs
Zero-scale error Notes 1, 2, 3, 4, 5	E_{ZS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 5	E_{FS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error Notes 1, 4, 5	ILE	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V