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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0120A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/I1C (512KB) Descriptions in the User's Manual: Hardware Rev. 1.01 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1C Group	Lot No. All lots	Reference Document	RL78/I1C (512KB) User's Manual: Hardware Rev. 1.01 R01UH0889EJ0101 (Nov. 2022)		

This document describes misstatements found in the RL78/I1C (512KB) User's Manual: Hardware Rev. 1.01 (R01UH0889EJ0211).

Corrections

Applicable Item	Applicable Page	Contents
43.3.2 Supply current characteristics	Page 1228 to Page 1233	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0889EJ0101
1	43.3.2 Supply current characteristics			Page 1228 to Page 1233	Page 3 to Page 7

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/I1C Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0120A/E	Jan. 20, 2023	First edition issued Corrections No.1 revised (this document)

1. 43.3.2 Supply current characteristics (Page 1228 to Page 1233)

Incorrect:

43.3.2 Supply current characteristics

(T_A = −40 to +85° C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0V) (1/6)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{IH} = 32 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		2.5		mA
						V_{DD} = 3.0 V		2.5		mA
					Normal operation	V_{DD} = 5.0 V		5.6	9.1	mA
						V_{DD} = 3.0 V		5.6	9.1	mA
				f_{IL} = 15 kHz, T_A = +85°C [Note 7]	Normal operation			5.0	13	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD}, V_{RTC} or V_{SS}, EV_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, 12-bit A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors.**

2. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

3. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). **However, not including the current flowing into independent power supply RTC, 12-bit interval timer.**

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LP (low-power main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

6. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

7. When high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Correct:

43.3.2 Supply current characteristics

(T_A = −40 to +85° C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0V) (1/6)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{IH} = 32 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		2.5		mA
						V_{DD} = 3.0 V		2.5		mA
					Normal operation	V_{DD} = 5.0 V		5.6	9.1	mA
						V_{DD} = 3.0 V		5.6	9.1	mA
				f_{IL} = 15 kHz, T_A = +85°C [Note 7]	Normal operation			5.0	13	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD}, V_{RTC} or V_{SS}, EV_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, 12-bit A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.

2. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

3. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1).

6. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
7. When high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
   2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
   2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
   LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
   LP (low-power main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz
   LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
6. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
7. When high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = −40 to +85° C, 1.6 V ≤ AVDD = EVDD = VDD ≤ 5.5 V, AVSS = VSS = EVSS = 0V) (3/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	IDD2 [Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	fIH = 32 MHz[Note 4]	VDD = 5.0 V		0.69	1.9	mA
					VDD = 3.0 V		0.68	1.9	mA
				fCLK = 32 MHz[Note 4], PLL operation	VDD = 5.0 V		1.2	2.2	mA
					VDD = 3.0 V		1.2	2.2	mA
				fIH = 24 MHz[Note 4]	VDD = 5.0 V		0.56	1.5	mA
					VDD = 3.0 V		0.56	1.5	mA
				fIH = 16 MHz[Note 4]	VDD = 5.0 V		0.49	1.2	mA
					VDD = 3.0 V		0.49	1.2	mA
				fIH = 12 MHz[Note 4]	VDD = 5.0 V		0.41	1.0	mA
					VDD = 3.0 V		0.41	1.0	mA
				fIH = 6 MHz[Note 4]	VDD = 5.0 V		0.36	0.8	mA
					VDD = 3.0 V		0.36	0.8	mA
				fIH = 3 MHz[Note 4]	VDD = 5.0 V		0.33	0.7	mA
					VDD = 3.0 V		0.33	0.7	mA
			LS (low-speed main) mode[Note 7] (MCSEL = 0)	fIH = 8 MHz[Note 4]	VDD = 3.0 V		290	755	µA
					VDD = 2.0 V		290	755	µA
				fIH = 6 MHz[Note 4]	VDD = 3.0 V		240	655	µA
					VDD = 2.0 V		240	655	µA
				fIH = 3 MHz[Note 4]	VDD = 3.0 V		210	556	µA
					VDD = 2.0 V		210	556	µA
			LS (low-speed main) mode[Note 7] (MCSEL = 1)	fIH = 4 MHz[Note 4]	VDD = 3.0 V		220	450	µA
					VDD = 2.0 V		220	450	µA
				fIM = 4 MHz[Note 8]	VDD = 3.0 V		60	350	µA
					VDD = 2.0 V		60	350	µA
			LV (low-voltage main) mode[Note 7]	fIH = 4 MHz[Note 4]	VDD = 3.0 V		625	1200	µA
					VDD = 2.0 V		625	1200	µA
			LP (low-power main) mode[Note 7] (MCSEL = 1)	fIH = 1 MHz[Note 4]	VDD = 3.0 V		200	410	µA
					VDD = 2.0 V		200	410	µA
				fIM = 1 MHz[Note 8]	VDD = 3.0 V		35	150	µA
					VDD = 2.0 V		35	150	µA
			HS (high-speed main) mode[Note 7]	fMX = 20 MHz[Note 3], VDD = 5.0 V	Square wave input		0.31	1.15	mA
					Resonator connection		0.53	1.35	mA

(TA = −40 to +85° C, 1.6 V ≤ AVDD = EVDD = VDD ≤ 5.5 V, AVSS = VSS = EVSS = 0V) (3/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	IDD2 [Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	fIH = 32 MHz[Note 4]	VDD = 5.0 V		0.69	1.9	mA
					VDD = 3.0 V		0.68	1.9	mA
				fCLK = 32 MHz[Note 4], PLL operation	VDD = 5.0 V		1.2	2.2	mA
					VDD = 3.0 V		1.2	2.2	mA
				fIH = 24 MHz[Note 4]	VDD = 5.0 V		0.56	1.5	mA
					VDD = 3.0 V		0.56	1.5	mA
				fIH = 16 MHz[Note 4]	VDD = 5.0 V		0.49	1.2	mA
					VDD = 3.0 V		0.49	1.2	mA
				fIH = 12 MHz[Note 4]	VDD = 5.0 V		0.41	1.0	mA
					VDD = 3.0 V		0.41	1.0	mA
				fIH = 6 MHz[Note 4]	VDD = 5.0 V		0.36	0.8	mA
					VDD = 3.0 V		0.36	0.8	mA
				fIH = 3 MHz[Note 4]	VDD = 5.0 V		0.33	0.7	mA
					VDD = 3.0 V		0.33	0.7	mA
			LS (low-speed main) mode[Note 7] (MCSEL = 0)	fIH = 8 MHz[Note 4]	VDD = 3.0 V		290	755	µA
					VDD = 2.0 V		290	755	µA
				fIH = 6 MHz[Note 4]	VDD = 3.0 V		240	655	µA
					VDD = 2.0 V		240	655	µA
				fIH = 3 MHz[Note 4]	VDD = 3.0 V		210	556	µA
					VDD = 2.0 V		210	556	µA
			LS (low-speed main) mode[Note 7] (MCSEL = 1)	fIH = 4 MHz[Note 4]	VDD = 3.0 V		220	450	µA
					VDD = 2.0 V		220	450	µA
				fIM = 4 MHz[Note 5]	VDD = 3.0 V		60	350	µA
					VDD = 2.0 V		60	350	µA
			LV (low-voltage main) mode[Note 7]	fIH = 4 MHz[Note 4]	VDD = 3.0 V		625	1200	µA
					VDD = 2.0 V		625	1200	µA
			LP (low-power main) mode[Note 7] (MCSEL = 1)	fIH = 1 MHz[Note 4]	VDD = 3.0 V		200	410	µA
					VDD = 2.0 V		200	410	µA
				fIM = 1 MHz[Note 5]	VDD = 3.0 V		35	150	µA
					VDD = 2.0 V		35	150	µA
			HS (high-speed main) mode[Note 7]	fMX = 20 MHz[Note 3], VDD = 5.0 V	Square wave input		0.31	1.15	mA
					Resonator connection		0.53	1.35	mA

(T_A = −40 to +85° C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0V) (4/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	LS (low-speed main) mode[Note 7] (MCSEL = 0)	f_{MX} = 8 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		113	420	μA
					Resonator connection		176	485	μA
				f_{MX} = 8 MHz[Note 3], V_{DD} = 2.0 V	Square wave input		113	420	μA
			Sub clock operation	f_{SUB} = 32.768 kHz[Note 5], T_A = −40°C	Square wave input		0.80	6.6	μA
					Resonator connection		1.00	6.8	μA
				f_{SUB} = 32.768 kHz[Note 5], T_A = +25°C	Square wave input		1.0	4.1	μA
					Resonator connection		1.4	4.3	μA
				f_{SUB} = 32.768 kHz[Note 5], T_A = +50°C	Square wave input		1.2	5.6	μA
					Resonator connection		1.6	5.7	μA
				f_{SUB} = 32.768 kHz[Note 5], T_A = +70°C	Square wave input		1.6	9.0	μA
					Resonator connection		2.0	10.6	μA
				f_{SUB} = 32.768 kHz[Note 5], T_A = +85°C	Square wave input		2.80	16.2	μA
					Resonator connection		3.00	19.6	μA
				f_{IL} = 15 kHz[Note 9], T_A = −40°C			0.83	1.85	μA
									μA
				f_{IL} = 15 kHz[Note 9], T_A = +25°C			1.07	2.25	μA
									μA
				f_{IL} = 15 kHz[Note 9], T_A = +85°C			2.68	28.1	μA
									μA
	I_{DD3}[Note 6]	STOP mode[Note 8]	T_A = −40°C				0.47	0.95	μA
			T_A = +25°C				0.66	1.60	μA
			T_A = +50°C				0.84	4.80	μA
			T_A = +70°C				1.22	10.60	μA
			T_A = +85°C				1.94	13	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, 12-bit A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors.**

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and Subsystem clock are stopped.

(T_A = −40 to +85° C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0V) (4/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	LS (low-speed main) mode[Note 7] (MCSEL = 0)	f_{MX} = 8 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		113	420	μA
					Resonator connection		176	485	μA
				f_{MX} = 8 MHz[Note 3], V_{DD} = 2.0 V	Square wave input		113	420	μA
			Sub clock operation	f_{SUB} = 32.768 kHz[Note 6], T_A = −40°C	Square wave input		0.80	6.6	μA
					Resonator connection		1.00	6.8	μA
				f_{SUB} = 32.768 kHz[Note 6], T_A = +25°C	Square wave input		1.0	4.1	μA
					Resonator connection		1.4	4.3	μA
				f_{SUB} = 32.768 kHz[Note 6], T_A = +50°C	Square wave input		1.2	5.6	μA
					Resonator connection		1.6	5.7	μA
				f_{SUB} = 32.768 kHz[Note 6], T_A = +70°C	Square wave input		1.6	9.0	μA
					Resonator connection		2.0	10.6	μA
				f_{SUB} = 32.768 kHz[Note 6], T_A = +85°C	Square wave input		2.80	16.2	μA
					Resonator connection		3.00	19.6	μA
				f_{IL} = 15 kHz[Note 9], T_A = −40°C			0.83	1.85	μA
									μA
				f_{IL} = 15 kHz[Note 9], T_A = +25°C			1.07	2.25	μA
									μA
				f_{IL} = 15 kHz[Note 9], T_A = +85°C			2.68	28.1	μA
									μA
	I_{DD3}	STOP mode[Note 8]	T_A = −40°C				0.47	0.95	μA
			T_A = +25°C				0.66	1.60	μA
			T_A = +50°C				0.84	4.80	μA
			T_A = +70°C				1.22	10.60	μA
			T_A = +85°C				1.94	13	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} V_{RTC} or V_{SS}, EV_{SS}.

The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, the 12-bit A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

5. When operating independent power supply RTC and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. **However, not including the current flowing into the 12-bit interval timer and watchdog timer. When high-speed on-chip oscillator and high-speed system clock are stopped**.
6. **When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. However, not including the current flowing into independent power supply RTC, 12-bit interval timer, and watchdog timer.**
7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
   2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
   2.5 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
   2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 12 MHz
   2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
   LS (low-speed main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
   LP (low-power main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz
   LV (low-voltage main) mode: 1.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.
9. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
4. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and Subsystem clock are stopped.
5. When high-speed on-chip oscillator system clock, low-speed on-chip oscillator, high-speed system clock, and Subsystem clock are stopped.
6. When operating independent power supply RTC and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.
7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
   2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
   2.5 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
   2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 12 MHz
   2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
   LS (low-speed main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
   LP (low-power main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz
   LV (low-voltage main) mode: 1.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.
9. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C