# **RENESAS TECHNICAL UPDATE**

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A0259A/E	Rev.	1.00
Title	Errata to the User's Manual Regarding BGO Function in Linear Mode for Products with 2 Mbytes of Code Flash Memory		Information Category	Technical Notification		
		Lot No.				
Applicable Product	RX72M Group, RX72N Group, RX66N Group	All	Reference Document	User's Manual: Hardware for applic products (Refer to the table on the page for details)		

This document describes corrections to the description about BGO function in linear mode in the "Flash Memory (FLASH)" section of the User's Manual: Hardware for the applicable products stated above. Page and table numbers are based on the manual for the RX72M Group. Refer to the table on the last page of this update for the corresponding page and table numbers in the other groups.

# • Page 3243 of 3362

The "Products with 2 Mbytes of code flash memory" row in "Linear mode" in Table 64.25, Conditions under which Background Operation is Usable, is to be deleted as follows.

## Before correction

#### Table 64.25 Conditions under which Background Operation is Usable

		Range for Rewriting	Range for Reading	
Common to linear and dual modes		Data flash memory	Code flash memory	
Linear mode	Products with 4 Mbytes of code flash memory	First half (2 Mbytes) of the code flash memory (addresses FFC0 0000h to FFDF FFFFh)	Second half (2 Mbytes) of the code flash memory (addresses FFE0 0000h to FFFF FFFFh) Data flash memory	
		Second half (2 Mbytes) of the code flash memory (addresses FFE0 0000h to FFFF FFFFh)	First half (2 Mbytes) of the code flash memory (addresses FFC0 0000h to FFDF FFFFh) Data flash memory	
	Products with 2 Mbytes of code flash memory	First half (1 Mbytes) of the code flash memory (addresses FFE0 0000h to FFEF FFFFh)	Second half (1 Mbytes) of the code flash memory (addresses FFF0 0000h to FFFF FFFFh) Data flash memory	
		Second half (1 Mbytes) of the code flash memory (addresses FFF0 0000h to FFFF FFFFh)	First half (1 Mbytes) of the code flash memory (addresses FFE0 0000h to FFEF FFFFh) Data flash memory	
Dual mode	When the BANKSEL.BANKSWP[2:0] bits are 111b:	Bank 1 area of the code flash memory	Bank 0 area of the code flash memory Data flash memory	
	When the BANKSEL.BANKSWP[2:0] bits are 000b:	Bank 0 area of the code flash memory	Bank 1 area of the code flash memory Data flash memory	

# After correction

## Table 64.25 Conditions under which Background Operation is Usable

		Range for Rewriting	Range for Reading
Common to linear and dual modes		Data flash memory	Code flash memory
Linear mode	Products with 4 Mbytes of code flash memory	First half (2 Mbytes) of the code flash memory (addresses FFC0 0000h to FFDF FFFFh)	Second half (2 Mbytes) of the code flash memory (addresses FFE0 0000h to FFFF FFFFh) Data flash memory
		Second half (2 Mbytes) of the code flash memory (addresses FFE0 0000h to FFFF FFFFh)	First half (2 Mbytes) of the code flash memory (addresses FFC0 0000h to FFDF FFFFh) Data flash memory
Dual mode	When the BANKSEL.BANKSWP[2:0] bits are 111b:	Bank 1 area of the code flash memory	Bank 0 area of the code flash memory Data flash memory
	When the BANKSEL.BANKSWP[2:0] bits are 000b:	Bank 0 area of the code flash memory	Bank 1 area of the code flash memory Data flash memory

## • Reference Documents

Group	Manual Title (Document Number)	Page Number	Section Number	Table Number
RX72M Group	RX72M Group User's Manual: Hardware Rev.1.11 (R01UH0804EJ0111)	Page 3243 of 3362	64.17.2	Table 64.25
RX72N Group	RX72N Group User's Manual: Hardware Rev.1.11 (R01UH0824EJ0111)	Page 3115 of 3232	62.17.2	Table 62.25
RX66N Group	RX66N Group User's Manual: Hardware Rev.1.11 (R01UH0825EJ0110)	Page 2941 of 3058	60.17.2	Table 60.25

