# **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU	Document No.	TN-SY*-A0040A/E	Rev.	1.00	
Title	Errata for User's Manual regarding the IIC	Information Category	Technical Notification			
Applicable Product	Renesas Synergy™ S7G2 MCU Group	Lot No. All	Reference Document	S7G2 Microcontroller Group User's Manual Rev.1.40		

The specified Renesas Synergy S7G2 User's Manual has incorrect statements about the IIC.

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#### Incorrect

In slave mode, when a restart condition is detected (a start condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)

#### Correct

In slave mode, when a restart condition is detected (a restart condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)

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#### Incorrect

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.

#### Correct

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.

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#### Incorrect

The IIC can also set the flag to indicate the detection of arbitration loss during NACK transmission in master mode or during data transmission in slave mode.

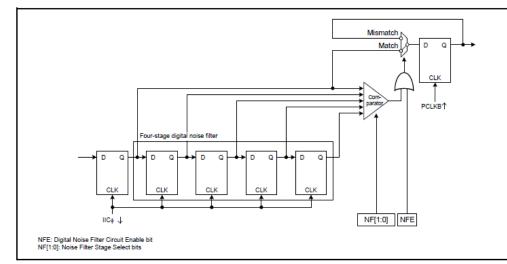
#### Correct

The IIC can also set the flag to indicate the detection of arbitration loss during NACK transmission in master mode or during data transmission in slave mode.

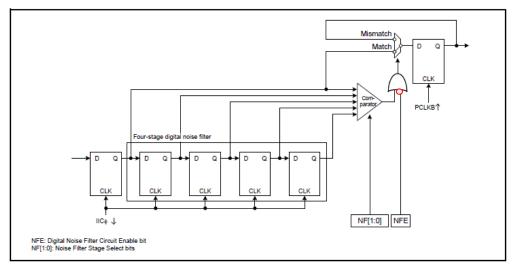


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#### Incorrect Figure



#### **Correct Figure**



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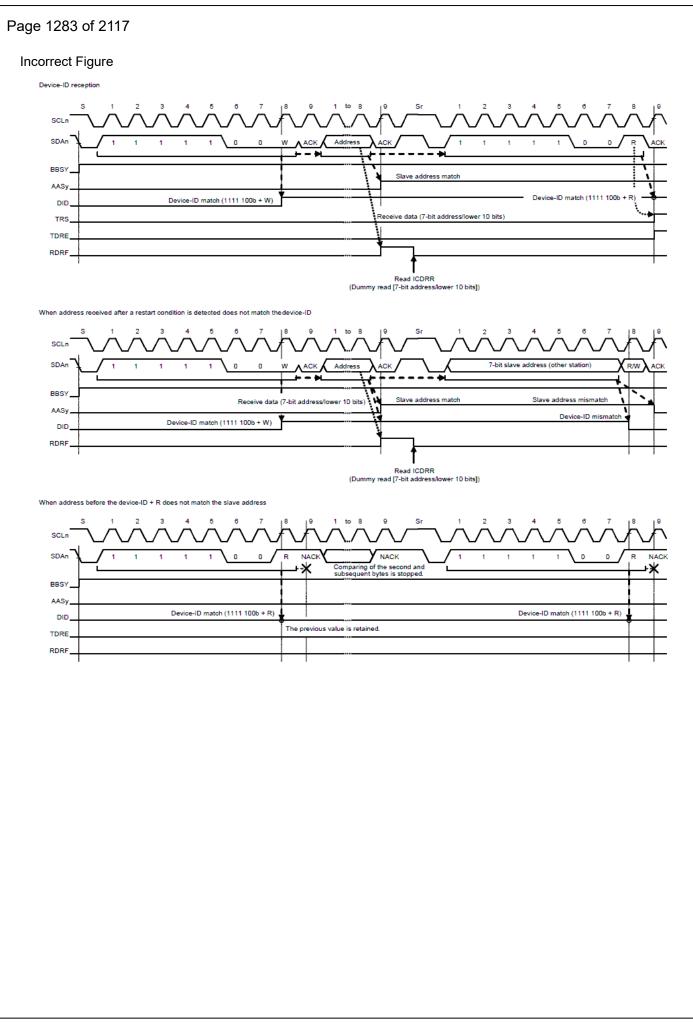
#### Incorrect

The IIC module provides detection of device-ID address compliant with the I2C bus specification (revision 03). When the IIC receives 1111 100b as the first byte after a start or restart condition was issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the eighth SCL clock cycle when the subsequent R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address.

#### Correct

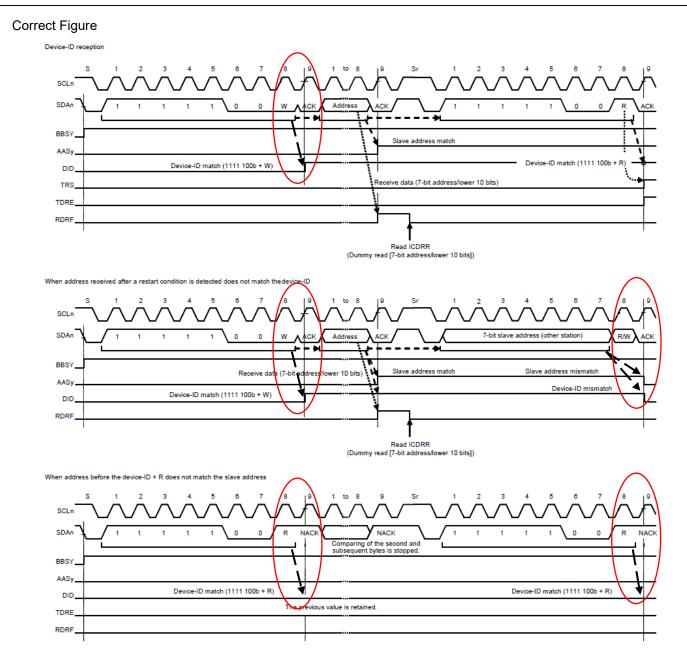
The IIC module provides detection of device-ID address compliant with the I2C bus specification (revision 03). When the IIC receives 1111 100b as the first byte after a start or restart condition was issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the 9th SCL clock cycle when the subsequent R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address.







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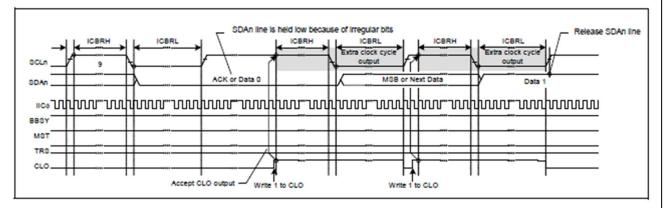
#### Page 1295 of 2117 Incorrect Figure (7-bit address + W) [Slave transmit mode] Automatic low-hold (to prevent wrong transmission) Bus free time (ICBRL) 5 2 3 4 6 7 Data (DATA 1) 7-bit slave address Transfer su ended .... BBSY Address match AASy .... Transmit data (DATA 1) Transmit data (DATA 2) TRS TDRE NACKE Write data to ICDRT Write data to ICDRT Write 1 to SP bit Clear NACKF flag register (DATA 1) register (DATA 2) **Correct Figure** [Slave transmit mode] utomatic low-hold (to prevent wrong transmission) Bus free time (ICBRL) 2 3 4 2 3 4 5 6 5 6 7-bit slave address W ACK Data (DATA 1) Transfer sus pended BBSY .... Address match .... AASy Transmit data (DATA 1) Transmit data (DATA 2) TRS TDRE NACKE Write 1 to SP bit Write data to ICDRT Write data to ICDRT Clear NACKF flag register (DATA 1) register (DATA 2) Page 1305 of 2117 Incorrect More extra clock cycles can be output consecutively by the software writing 1 to the CLO bit after having read CLO = 0. Correct If the BBSY flag is 1, SCL terminal keeps low output, if BBSY flag is 0, SCL terminal keeps high output. Additional clock cycles can be output consecutively by writing 1 to the CLO bit with software after reading the bit as 0. Page 1305 of 2117 Incorrect Use this function with the MALE bit in ICFER set to 0 (master arbitration-lost detection disabled). If the MALE bit is set to 1 (enabled), arbitration is lost when the value of the SDAO bit in ICCR1 does not match the state of the SDAn line. Correct this function with the MALE bit in ICFER set to 0 (master arbitration lost detection disabled). If the MALE bit is

set to 1 (enabled), arbitration is lost when the value of the SDAO bit in ICCR1 does not match the state of the SDAn line.

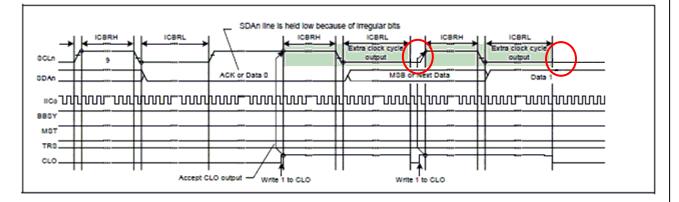


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Incorrect Figure



#### **Correct Figure**





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Incorrect Table

Registers	3	Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection	
ICCR1	ICE, IICRST	In reset	Saved	Saved	Saved	Saved	
	SCLO, SDAO		In reset	In reset			
	Others			Saved			
ICCR2	BBSY	In reset	In reset	Saved	Set	Saved	
	ST			In reset	Saved	Saved	
	TRS,MST				Set or saved	In reset	
	Others				In reset	In reset or Saved	
ICMR1 BC[2:0]	BC[2:0]	In reset In reset		In reset	In reset	Saved	
	Others			Saved	Saved		
ICMR2		In reset	In reset	Saved	Saved	Saved	
ICMR3		In reset	In reset	Saved	Saved	Saved	
ICFER		In reset	In reset	Saved	Saved	Saved	
ICSER		In reset	In reset	Saved	Saved	Saved	
ICIER		In reset	In reset	Saved	Saved	Saved	
ICSR1		In reset	In reset	In reset	Saved	In reset	
ICSR2	TDRE, TEND	In reset	In reset	In reset	Saved	In reset	
	START				Set		
	STOP				Saved	Set	
	Others				Saved	Saved	
ICWUR		In reset	In reset	Saved	Saved	Saved	
	SARL1, SARL2 SARU1, SARU2	In reset	In reset	Saved	Saved	Saved	
ICBRH,	ICBRL	In reset	In reset	Saved	Saved	Saved	
ICDRT		In reset	In reset	Saved	Saved	Saved	
ICDRR		In reset	In reset	Saved	Saved	Saved	
ICDRS		In reset	In reset	In reset	Saved	Saved	
Timeout	function	In reset	In reset	Operating	Operating	Operating	
Bus free measure		In reset	In reset	Operating	Operating	Operating	



Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	In reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		In reset	In reset		
	Others			Saved		
ICCR2	BBSY	In reset	In reset	Saved	Set	In reset
	ST, <mark>RS</mark>			In reset	In reset	Saved
	SP					In reset
	TRS				Set or saved	
	MST					
ICMR1	BC[2:0]	In reset	In reset	In reset	In reset	Saved
	Others			Saved	Saved	
ICMR2		In reset	In reset	Saved	Saved	Saved
ICMR3	ACKBIT	In reset	In reset	Saved	Saved	In reset
	Others					Saved
ICFER		In reset	In reset	Saved	Saved	Saved
ICSER		In reset	In reset	Saved	Saved	Saved
ICIER		In reset	In reset	Saved	Saved	Saved
ICSR1		In reset	In reset	In reset	Saved	In reset
CSR2	TEND	In reset	In reset	In reset	Saved	In reset
	TDRE				Set or saved	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		In reset	In reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		In reset	In reset	Saved	Saved	Saved
ICBRH, ICBRL		In reset	In reset	Saved	Saved	Saved
ICDRT		In reset	In reset	Saved	Saved	Saved
ICDRR		In reset	In reset	Saved	Saved	Saved
ICDRS		In reset	In reset	In reset	Saved	Saved
Timeout function		In reset	In reset	In reset	Operating	Operating
Bus free time measurement		In reset	In reset	Operating	Operating	Operating

