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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A039A/E	Rev.	1.00
Title	I²C bus interface（RIIC） Precautions for using timeout detection function and stop condition issuance timing when receiving master.		Information Category	Technical Notification		
Applicable Product	RX210 group	Lot No. All lots	Reference Document	RX210 group User's Manual, Hardware section		

Regarding I²C bus interface (RIIC), please have a look at the following two precautions.

1. Precautions for stop condition issuance timing when receiving master

With I²C bus interface (RIIC), one clock cycle may be inserted between the ninth clock cycle of master reception and stop condition issuance.

When this clock affects the communication, follow the avoidance flow "Figure 29.10 Example of Master Reception Flowchart (7-Bit Address Format)" indicated on the Page.6 of this Technical Update.

(1) Conditions

・While holding at low at the falling edge of the ninth clock cycle, writing SP=1 and reading data from ICDRR are performed in a row.

・When data is read from ICDRR after the falling edge of the ninth clock of master reception and writing SP=1 are detected at the same time in the RIIC.

・After SP=1 is written, when the falling edge of the ninth clock cycle of master reception and data reading from ICDRR are detected at the same time in the RIIC.

(2) Phenomenon

One clock cycle is inserted between the ninth clock cycle of master reception and stop condition issuance.

2. Precautions when using timeout detection function

While timeout detection function of I²C bus interface（RIIC） is set to CMR1.CKS [2:0] ≠ 000b, timeout is detected even when communications are proceeding correctly. To avoid this, use registered disclosed in this document and follow the avoidance flow. In this avoidance flow, every time data is accessed, write 00h to the timeout internal counter and clear counter.

Thus, it is applicable only to data transfer using CPU or one using DTC. When you use DMAC for data transfer of RIIC, you need to set ICMR1.CKS [2:0] ＝ 000b or change it to transfer using CPU or one using DTC.

(1) Condition

When using timeout detection function of I²C bus interface (RIIC) under the setting of CMR1.CKS [2:0] ≠ 000.

(2) Phenomenon

Even when communications are proceeding correctly, timeout is detected from a set of ICFER.TMOE bit after a certain period of time for detection has elapsed.

(3) Disclosed register

① ICMR2.TMWE bit (b3) of I2C bus mode register (ICMR2) will be disclosed.

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			TMWE	TMOH	TMOL	TMOS
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3	TMWE	Timeout internal counter write enable bit	0: Writing to internal counter of timeout detection function is disabled 1: Writing to internal counter of timeout detection function is enabled When this bit is set to "1", the address of timeout internal counter (TMOCNTL/U) is allocated to the address of SARL0/SARU0.	R/W

② Disclose the timeout internal counter register (TMOCNT).

Timeout internal counter (TMOCNT)

Address RIIC0.TMOCNTL 0008 830Ah*, RIIC0.TMOCNTU 0008 830Bh*

Table. Register Allocation for 16-Bit Access

Address	Upper 8 Bits	Lower 8 Bits
0008 830Ah*	RIIC0.TMOCNTU	RIIC0.TMOCNTL

*Same addresses with ones of the slave address registers, SARL0, SARU0. Care should be taken.

・TMOS=0 (Long mode)

	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TMOCNTU								TMOCNTL							

・TMOS=1 (Short mode)

	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TMOCNTU								TMOCNTL							

Bit	Symbol	Bit name	Description	R/W
b7-0	TMOCNTL	Timeout internal counter	Timeout internal counter low-order	W *1

*1 : Value in timeout internal counter cannot be read. When value is read, the read value is FFh.

Bit	Symbol	Bit name	Description	R/W
b7-0	TMOCNTU	Timeout internal counter	Timeout internal counter high-order *1	W *2

*1 : With TMOS=1 (Short mode), b7-b4 are reserved bits. They are writable, however value written is disabled.

*2 : Value in timeout internal counter cannot be read. When value is read, the read value is FFh.

Timeout internal counter （TMOCNTL/TMOCNTU） is initialized (00h) after a reset, while ICCR1.IICRST=1 or ICFER.TMOE=1 and PCLK/1 is selected with ICMR1.CKS[2:0]=000b setting, and when counter clear conditions specified by TMOH/TMOL of ICMR2（SCL rising edge/falling edge detection）are satisfied.

TMOCNTL register and TMOCNTU register comprise a single 16-bit register so they can be accessed together by 16-bit transfer instruction. In case of 16-bit access, please access to the address indicated in the table “Register Allocation for 16-Bit Access” on page2.

3. Avoidance Flow

To avoid “1. Precautions for stop condition issuance timing when receiving master” and “2. Precautions for timeout detection function”, add the procedures to the flowchart in the user’s manual.
Additional procedures for “1. Precautions for stop condition issuance timing when receiving master” are marked in blue, and those for “2. Precautions for using timeout detection function” are marked in red.

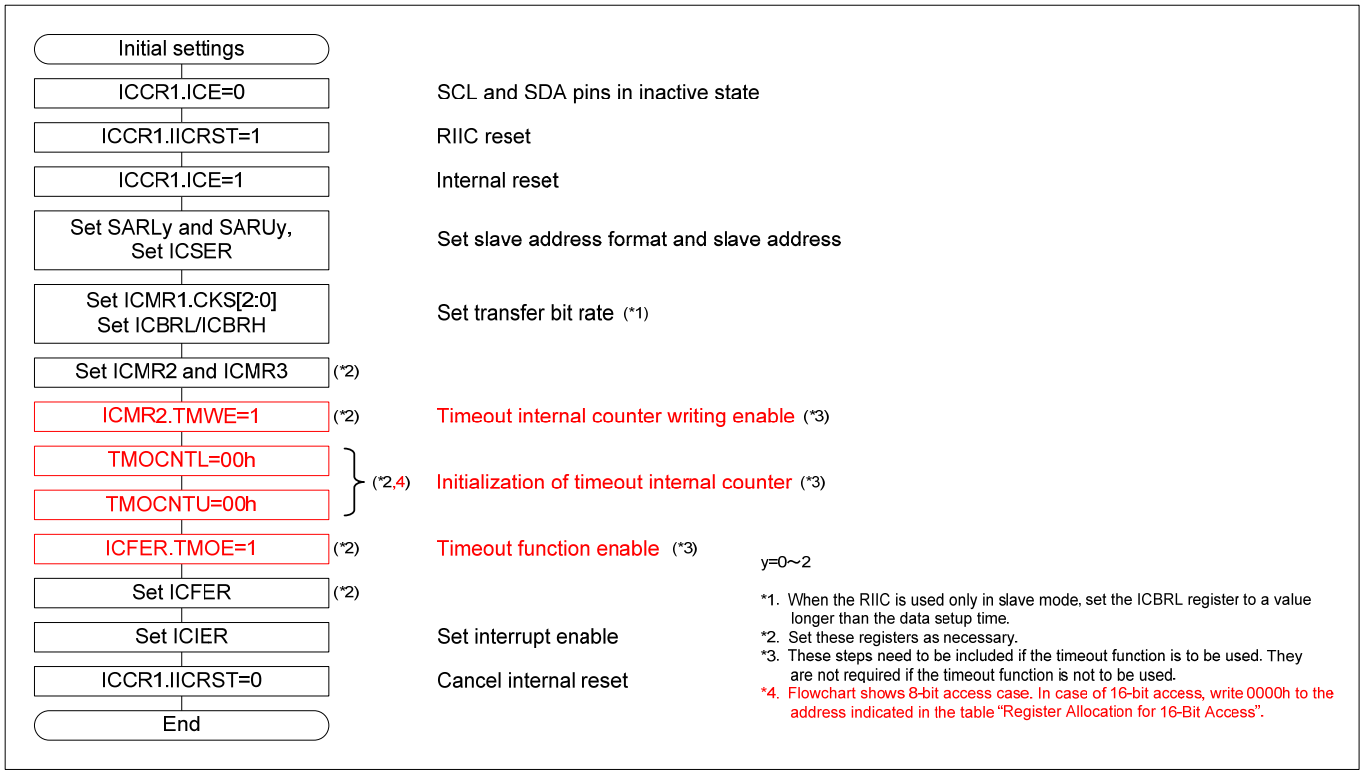


Figure 29.5 Example of RIIC Initialization Flow

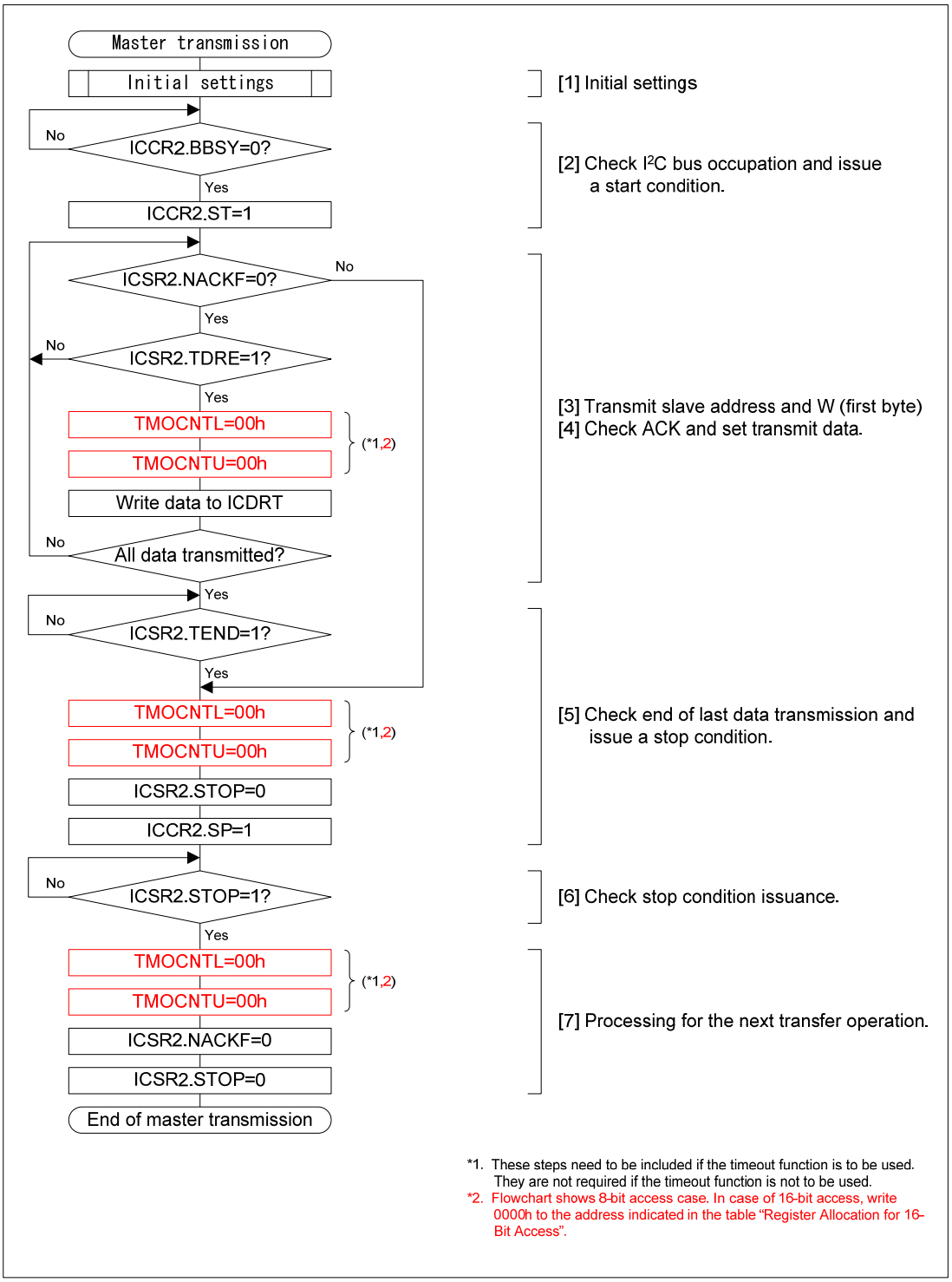


Figure 29.6 Example of Master Transmission Flowchart

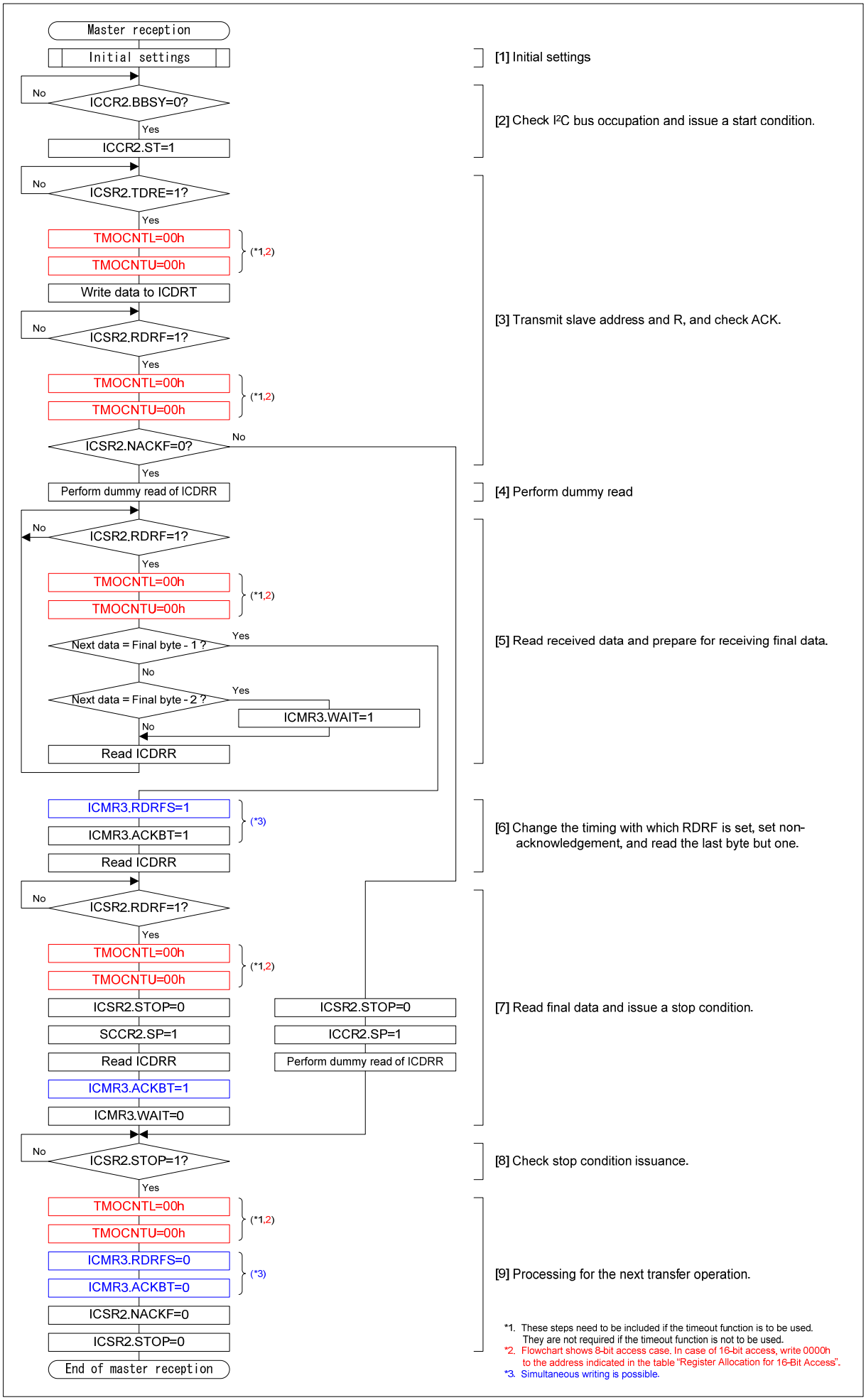


Figure 29.10 Example of Master Reception Flowchart (7-Bit Address Format)

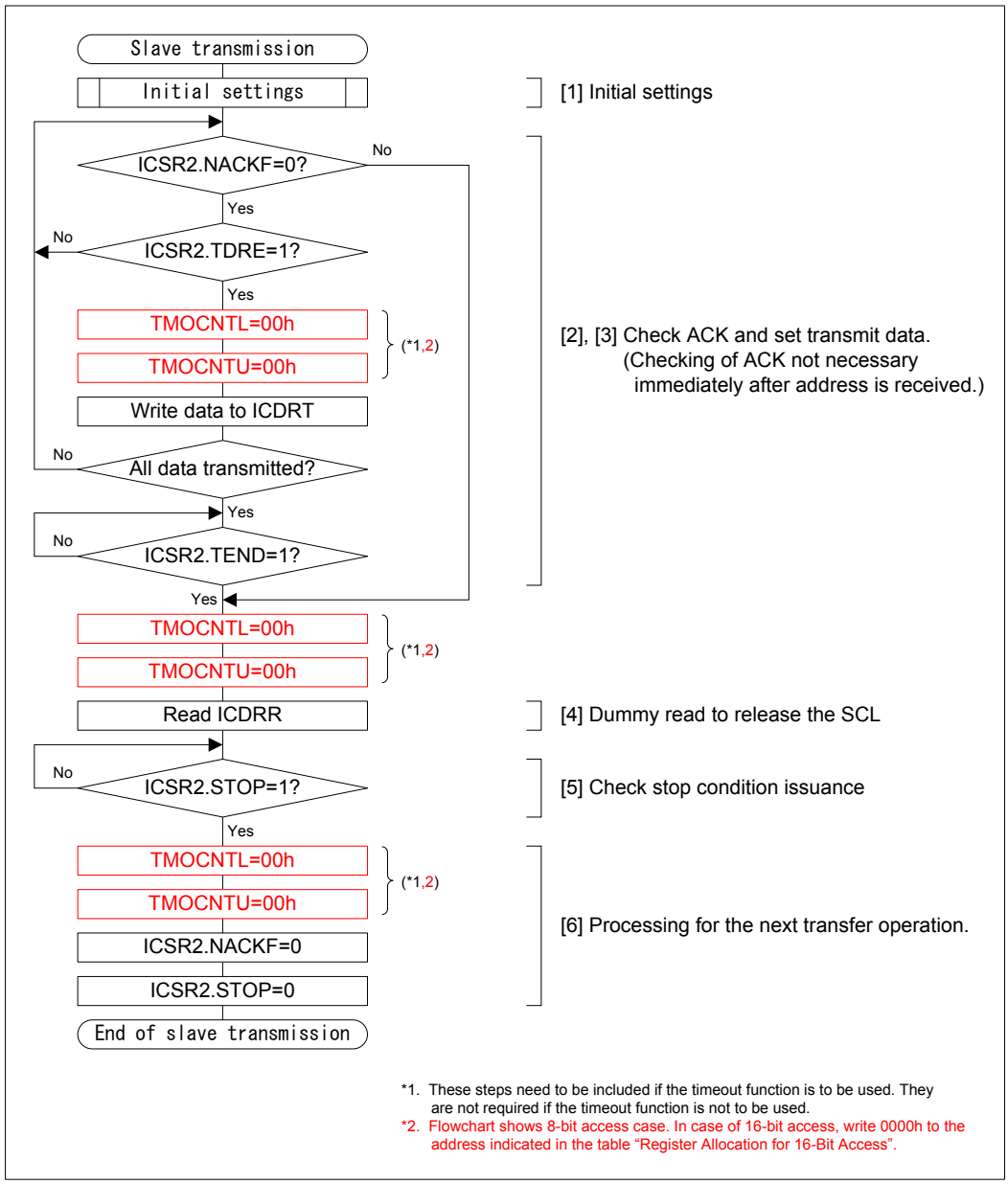


Figure 29.14 Example of Slave Transmission Flowchart

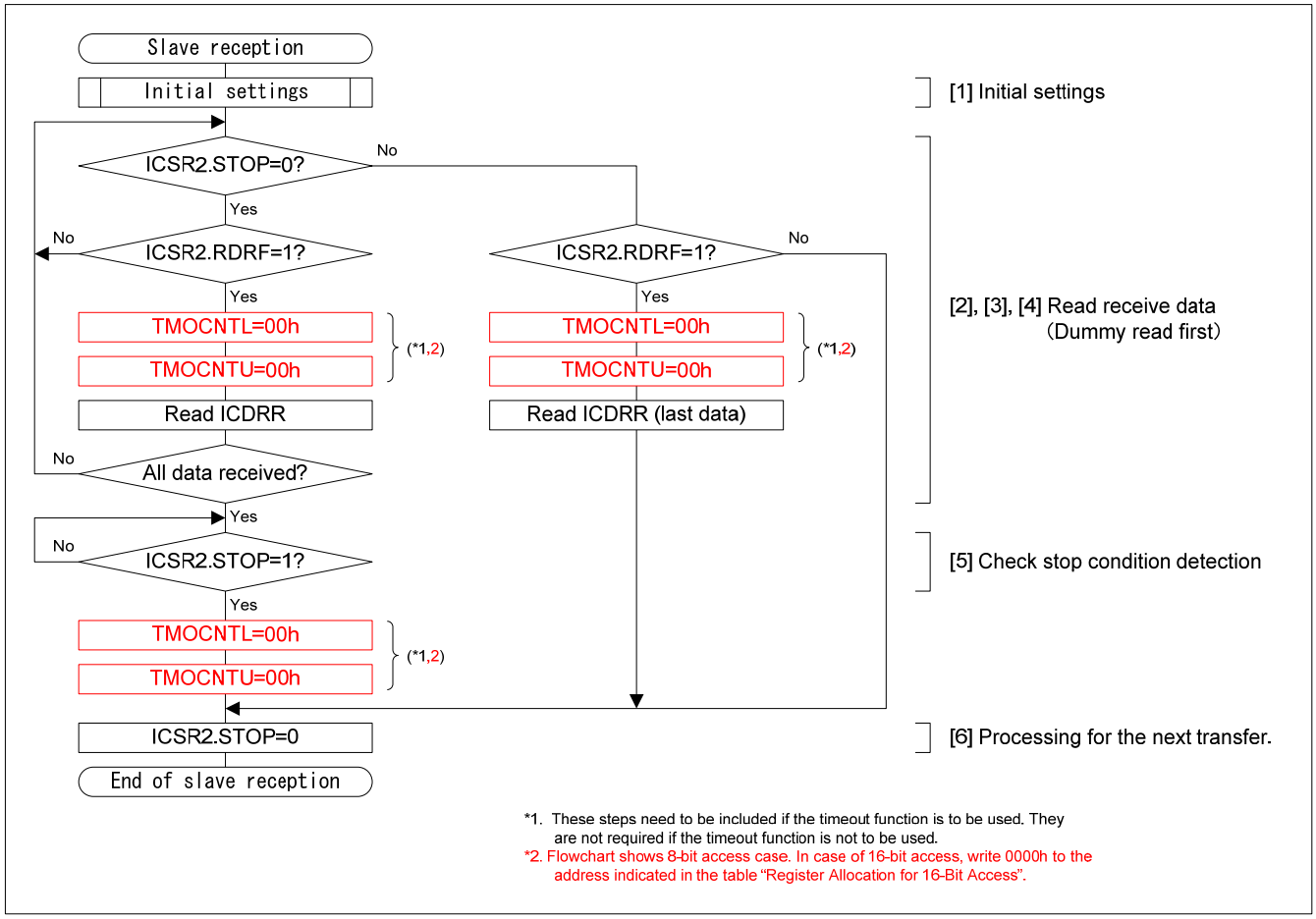


Figure 29.17 Example of Slave Reception Flowchart

4. Avoidance when using DTC

When writing transmit data to ICDRT or reading receive data from ICDRR by the DTC during master transmission/reception, use the following flow to avoid the phenomenon. Set the DTC to chain transfer, and clear internal counter every time transmit data or receive data is transferred.

Master reception flowchart is indicated below.

This flowchart shows only flow involved with DTC transfer. For the rest of the flow, refer to the flowcharts indicated on page 4 to 8.

(1) Initial settings flow: What is indicated on page 4 + DTC setting

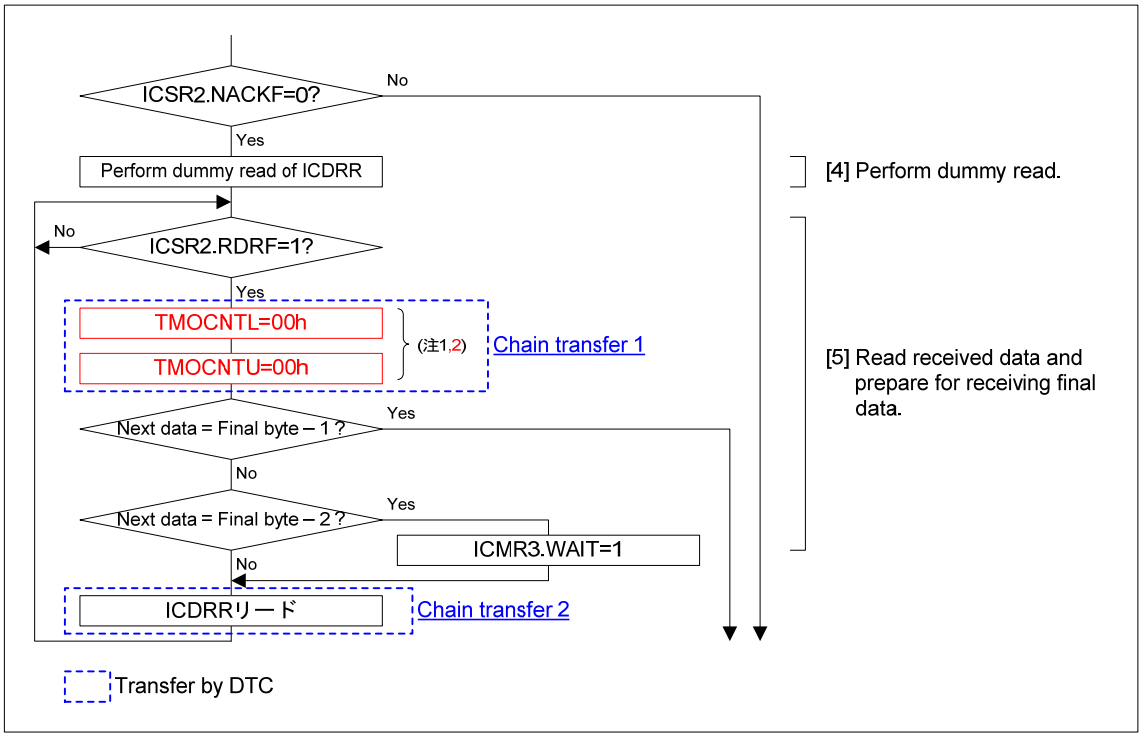
The DTC needs to be set to enable the following operation.

Set the DTC to chain transfer.

・First chain transfer (Chain transfer 1): Write 00h to TMOCNTL and TMOCNTU.

・Subsequent chain transfer (Chain transfer 2): Transfer specified by user（Read ICDRR, etc）

(2) Example of flowchart during N-2 times transfer by DTC（excerpt comments from the flowchart on page 6）



■Target Products and Reference

Group	Title	Rev.	Document No.	Chapter of I^2C
RX210 group	RX210 group User's Manual, Hardware section	Rev.1.10	R01UH0037EJ0110	29