Date: Oct. 23, 2012

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A850A/E	Rev.	1.00
Title	Notes about compression processing of Jpeg Codec Unit		Information Category	Technical Notification		
Applicable Product	SH7268 Group SH7269 Group	Lot No.				
		All	Reference Document	SH7268 Group, SH7269 Group User'sManual: Hardware Rev1.00 (R01UH0048EJ0100)		

We would like to inform you of the notice about compression processing of Jpeg Codec Unit.

[Notice]

When the remainder that divides the amount of output coded data by 8 is 1~6 bytes in compression, the last 1~6 bytes data may not be normally transferred.

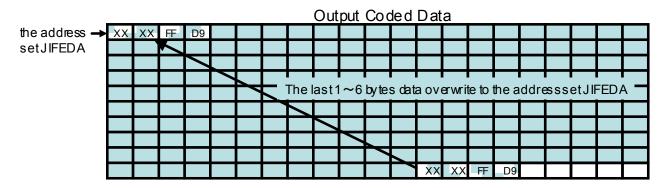
When it is not normally transferred, the last 1~6 bytes data overwrite to the address set JPEG Interface compression destination address register(JIFEDA).

*This module handles the output of coded data in 16-bit units.

For this reason, if the coded data have an odd code length, the final code for output will be H'D9FF.(H'FF is added)

When the remainder that divides the amount of output coded data by 8 is 1,3,5 bytes in compression, (the last 1,3,5 bytes + H'FF) data overwrite to the address set JIFEDA.

[Image]



[Workaround]

In compression you need to confirm whether output coded data is normally transferred. If it is not normally transferred, you need to correct error data. Refer to the following flow chart for how to correct error data.



[Flowchart]

[Before]

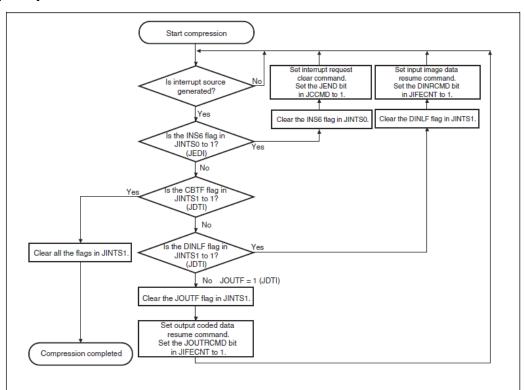


Figure 41.3 Compression Process Flow

[After]

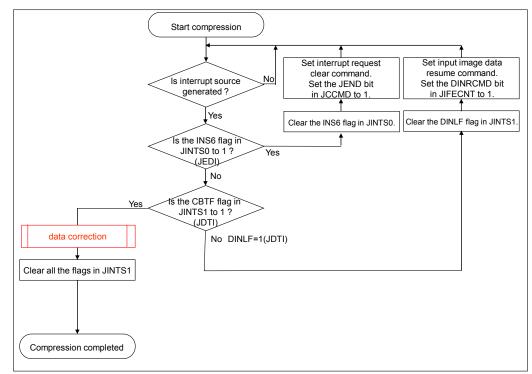


Figure 41.3 Compression Process Flow

Date: October 23, 2012

