9DBL02x2/9DBL04x2/9DBL06x1/9DBL08x1C

2 to 8-Output 3.3V PCIe Zero-Delay/Fanout Buffers

The 9DBL02x2/9DBL04x2/9DBL06x1/9DBL08x1C buffers are low-power, high-performance members of Renesas' full featured PCIe family. The buffers support PCIe Gen1 through Gen5.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum (SRIS, SRNS)

Typical Applications

- PCIe Riser Cards
- nVME Storage
- Networking
- Accelerators
- Industrial Control/Embedded

Key Specifications

- Additive PCIe Gen5 CC jitter < 60fs RMS (fanout mode)
- PCIe Gen5 CC jitter < 150fs RMS (High-BW ZDB Mode)

Features

- 2 to 8 Low-Power HCSL (LP-HCSL) outputs eliminate 4 resistors per output pair
- 9DBLxx4x devices provide integrated 100Ω terminations
- 9DBLxx5x devices provide integrated 85Ω terminations
- See AN-891 for easy coupling to other logic families
- Spread-spectrum compatible
- Dedicated OE# pin for each output
- 1MHz to 200MHz operation in fan-out mode
- 3 selectable SMBus addresses
- Extensive SMBus-selectable features allow optimization to customer requirements
- SMBus interface not required for device operation
- -40°C to +85°C operating temperature range
- Space-saving packages:
  - 4 × 4 mm 24-VFQFPN (9DBL02x2C)
  - 5 × 5 mm 32-VFQFPN (9DBL04x2C)
  - 5 × 5 mm 40-VFQFPN (9DBL06x1C)
  - 6 × 6 mm 48-VFQFPN (9DBL08x1C)

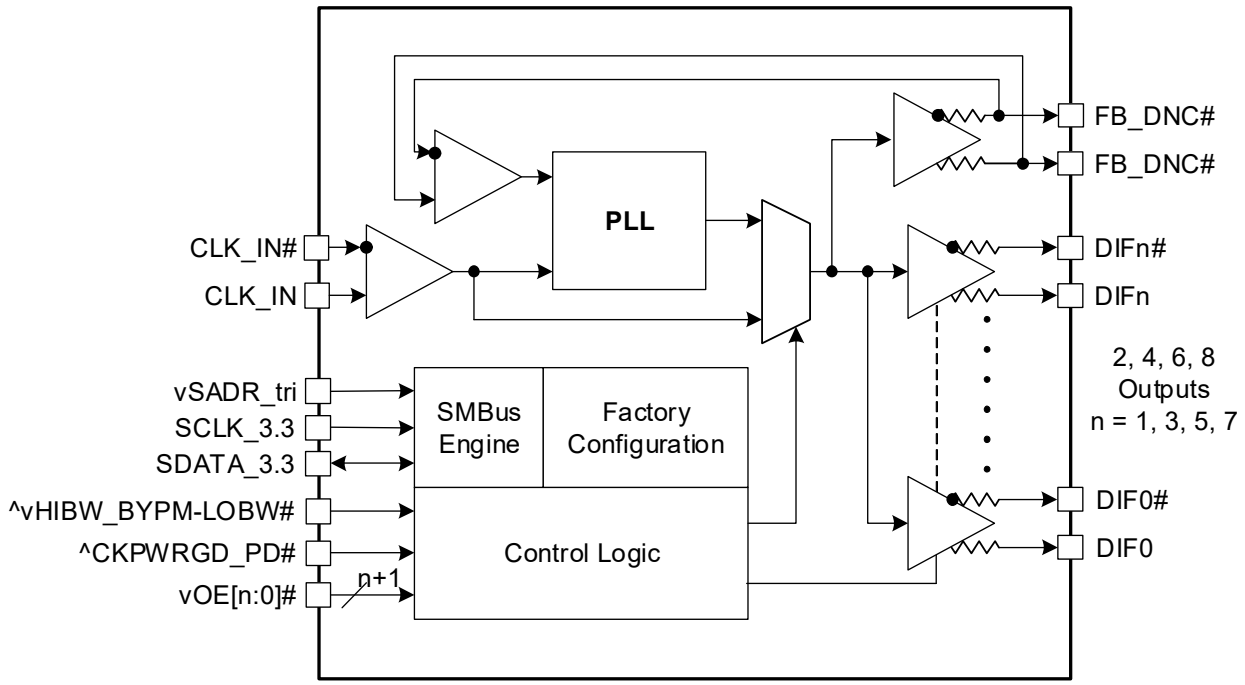

Figure 1. Block Diagram

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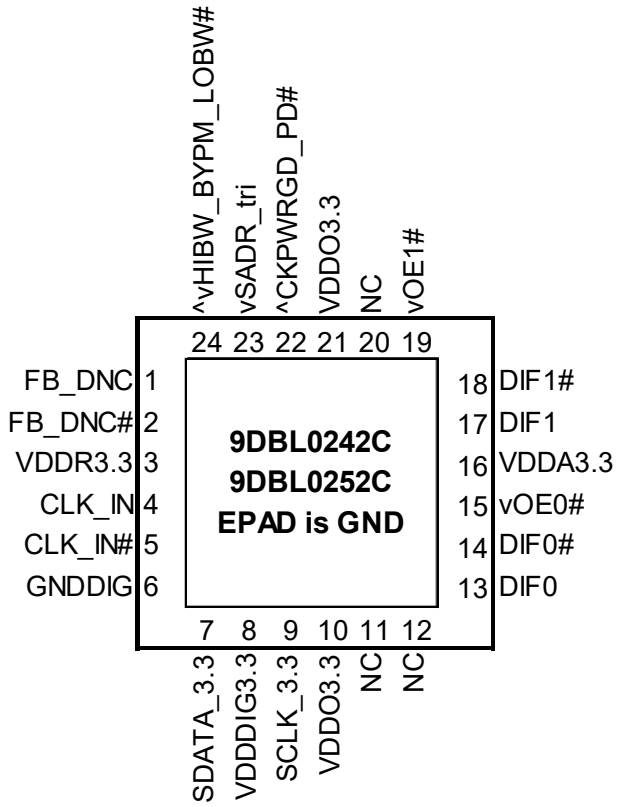
1. Pin Information

1.1 Pin Assignments – 9DBL02x2C



24-VFQFPN, 4 x 4 mm, 0.5mm pitch

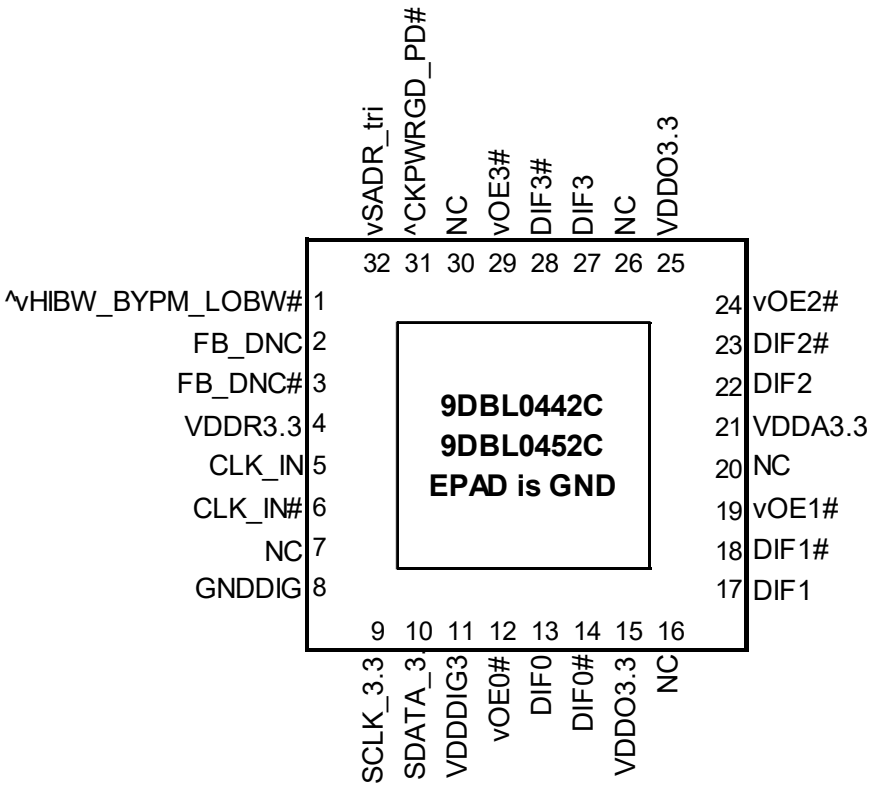
^ prefix indicates internal 120kOhm pull-up resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistor (biased to VDD/2)

v prefix indicates internal 120kOhm pull-down resistor

Figure 2. Pin Assignments for 4 × 4 mm 24-VFQFPN Package – Top View

1.2 Pin Assignments – 9DBL04x2C



32-VFQFPN, 5 × 5 mm, 0.5mm pitch

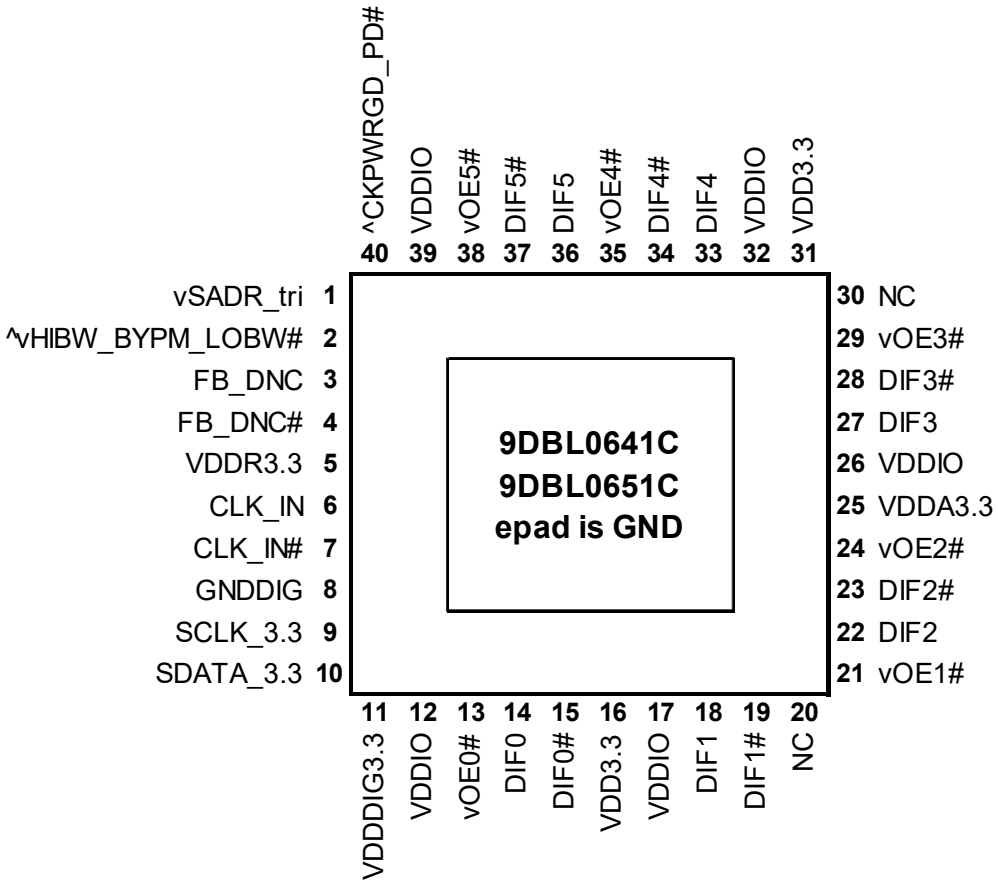
^v prefix indicates internal 120kOhm pull-up and pull-down resistors (biased to VDD/2)

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

Figure 3. Pin Assignments for 5 × 5 mm 32-VFQFPN Package – Top View

1.3 Pin Assignments – 9DBL06x1C



40-VFQFPN, 5mm x 5mm 0.4mm pin pitch

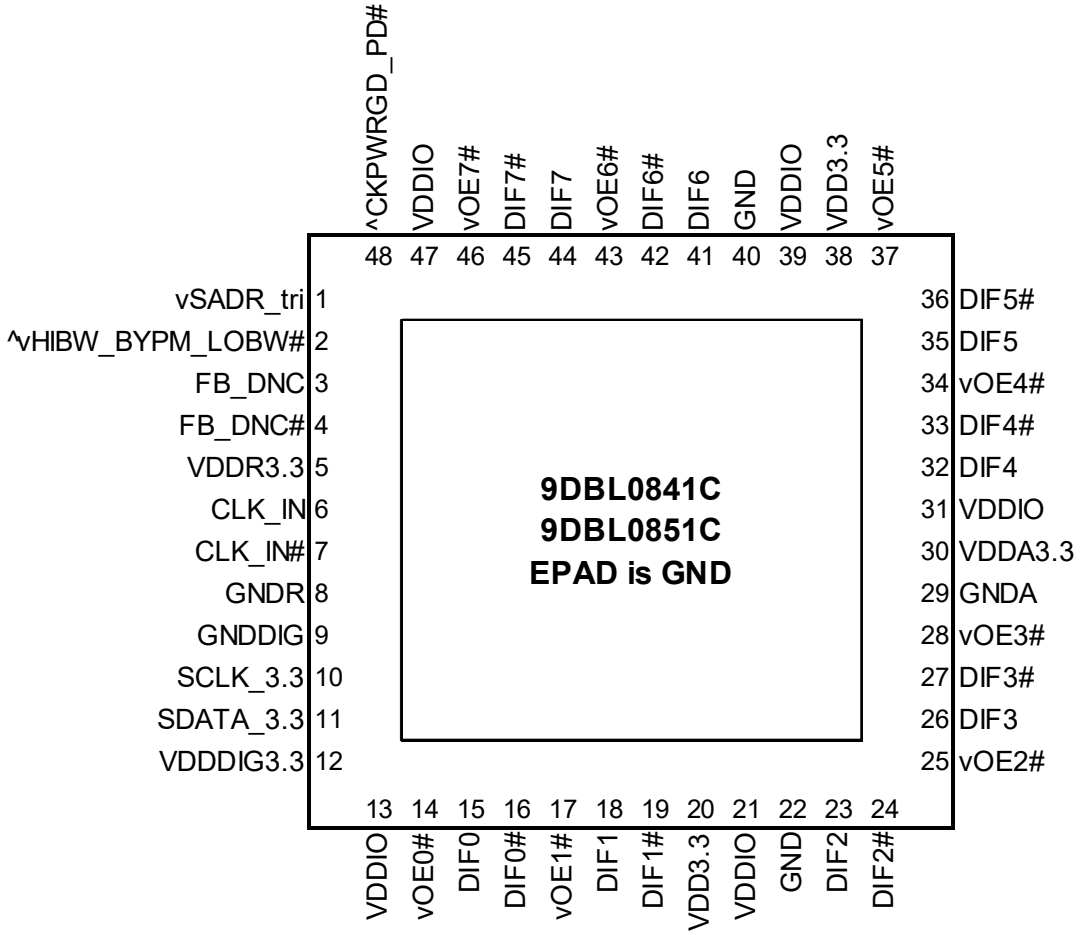
^v prefix indicates internal 120kOhm pull-up and pull-down resistor (biased to VDD/2)

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

Figure 4. Pin Assignments for 5 × 5 mm 40-VFQFPN Package – Top View

1.4 Pin Assignments – 9DBL08x1C



48-pin VFQFPN, 6x6 mm, 0.4mm pitch

^v prefix indicates internal 120kOhm pull-up and pull-down resistor (biased to VDD/2)

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

Figure 5. Pin Assignments for 6 × 6 mm 48-VFQFPN Package – Top View

1.5 Pin Descriptions

Table 1. Pin Descriptions

Pin Name [1] [2] [3]	Type	Description	08x1C Pin No.	06x1C Pin No.	04x2C Pin No.	02x2C Pin No.
^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kΩ pull-up resistor.	48	40	31	22
^vHIBW_BYPM_LOBW#	Latched In	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull-up/pull-down resistors.	2	2	1	24
CLK_IN	Input	True input of differential input clock.	6	6	5	4
CLK_IN#	Input	Complementary input if differential input clock.	7	7	6	5

Table 1. Pin Descriptions (Cont.)

Pin Name [1] [2] [3]	Type	Description	08x1C Pin No.	06x1C Pin No.	04x2C Pin No.	02x2C Pin No.
DIF0	Output	Differential true clock output.	15	14	13	13
DIF0#	Output	Differential complementary clock output.	16	15	14	14
DIF1	Output	Differential true clock output.	18	18	17	17
DIF1#	Output	Differential complementary clock output.	19	19	18	18
DIF2	Output	Differential true clock output.	23	22	22	-
DIF2#	Output	Differential complementary clock output.	24	23	23	-
DIF3	Output	Differential true clock output.	26	27	27	-
DIF3#	Output	Differential complementary clock output.	27	28	28	-
DIF4	Output	Differential true clock output.	32	33	-	-
DIF4#	Output	Differential complementary clock output.	33	34	-	-
DIF5	Output	Differential true clock output.	35	36	-	-
DIF5#	Output	Differential complementary clock output.	36	37	-	-
DIF6	Output	Differential true clock output.	41	-	-	-
DIF6#	Output	Differential complementary clock output.	42	-	-	-
DIF7	Output	Differential true clock output.	44	-	-	-
DIF7#	Output	Differential complementary clock output.	45	-	-	-
EPAD	GND	Connect to ground.	49	41	33	25
FB_DNC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.	3	3	2	1
FB_DNC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.	4	4	3	2
GND	GND	Ground pin.	22, 40	-	-	-
GNDA	GND	Ground pin for the PLL core.	29	-	-	-
GNDDIG	GND	Ground pin for digital circuitry.	9	8	8	6
GNDR	GND	Analog ground pin for the differential input (receiver).	8	-	-	-
NC	–	No connection.	-	20, 30	7, 16, 20, 26, 30	11, 12, 20
SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.	10	9	9	9
SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.	11	10	10	7
VDD3.3	Power	Power supply, nominal 3.3V.	20, 38	16, 31	-	-
VDDA3.3	Power	3.3V power for the PLL core.	30	25	21	16
VDDDIG3.3	Power	3.3V digital power (dirty power).	12	11	11	8
VDDIO	Power	Power supply for differential outputs.	13, 21, 31, 39, 47	12, 17, 26, 32, 39	-	-

Table 1. Pin Descriptions (Cont.)

Pin Name [1] [2] [3]	Type	Description	08x1C Pin No.	06x1C Pin No.	04x2C Pin No.	02x2C Pin No.
VDDO3.3	Power	Power supply for outputs. Nominally 3.3V.	-	-	15, 25	10, 21
VDDR3.3	Power	3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.	5	5	4	3
vOE0#	Input	Active low input for enabling output 0. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	14	13	12	15
vOE1#	Input	Active low input for enabling output 1. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	17	21	19	19
vOE2#	Input	Active low input for enabling output 2. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	25	24	24	–
vOE3#	Input	Active low input for enabling output 3. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	28	29	29	–
vOE4#	Input	Active low input for enabling output 4. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	34	35	–	–
vOE5#	Input	Active low input for enabling output 5. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	37	38	–	–
vOE6#	Input	Active low input for enabling output 6. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	43	–	–	–
vOE7#	Input	Active low input for enabling output 7. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs	46	–	–	–
vSADR_tri	Latched In	Tri-level latch to select SMBus Address. It has an internal pull-down resistor. See the SMBus Address Selection table.	1	1	32	23

1. A '^' prefix indicates internal 120kΩ pull-up resistor.
2. A '^v' prefix indicates internal 120kΩ pull-up and pull-down resistor (biased to VDD/2).
3. A 'v' prefix indicates internal 120kΩ pull-down resistor.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{DDx}	Supply Voltage[2]	Applies to V_{DD}, V_{DDA} and V_{DDIO}.	-0.5	-	3.9	V
V_{IN}	Input Voltage[3]		-0.5	-	V_{DD} + 0.5	V
V_{IHSMB}	Input High Voltage, SMBus	SMBus clock and data pins.	-	-	3.9	V
Ts	Storage Temperature		-65	-	150	°C
Tj	Junction Temperature		-	-	125	°C
ESD prot	Input ESD Protection	Human Body Model.	2500	-	-	V

1. Confirmed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied nor guaranteed.
3. Not to exceed 3.9V.

2.2 Thermal Characteristics

Table 3. Thermal Characteristics [1]

Parameter	Symbol	Conditions	Package	Typical Values	Unit
9DBL08xxC Thermal Resistance	θ_{JC}	Junction to case.	NDG48	33	°C/W
	θ_{Jb}	Junction to base.		2	°C/W
	θ_{JA0}	Junction to air, still air.		37	°C/W
	θ_{JA1}	Junction to air, 1 m/s air flow.		30	°C/W
	θ_{JA3}	Junction to air, 3 m/s air flow.		27	°C/W
	θ_{JA5}	Junction to air, 5 m/s air flow.		26	°C/W
9DBL06xxC 9DBL04xxC Thermal Resistance	θ_{JC}	Junction to case.	NDG40 NLG32	42	°C/W
	θ_{Jb}	Junction to base.		2	°C/W
	θ_{JA0}	Junction to air, still air.		39	°C/W
	θ_{JA1}	Junction to air, 1 m/s air flow.		33	°C/W
	θ_{JA3}	Junction to air, 3 m/s air flow.		28	°C/W
	θ_{JA5}	Junction to air, 5 m/s air flow.		27	°C/W
9DBL02xxC Thermal Resistance	θ_{JC}	Junction to case.	NLG24	60	°C/W
	θ_{Jb}	Junction to base.		5.4	°C/W
	θ_{JA0}	Junction to air, still air.		50	°C/W
	θ_{JA1}	Junction to air, 1 m/s air flow.		43	°C/W
	θ_{JA3}	Junction to air, 3 m/s air flow.		39	°C/W
	θ_{JA5}	Junction to air, 5 m/s air flow.		38	°C/W

1. Epad soldered to ground.

2.3 Electrical Specifications

Table 4. Additive PCIe Phase Jitter (Fan-out Buffer Mode) [1] [2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Industry Limit	Unit
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s) SSC ≤ -0.5%	-	0.57	1.89	86	ps (pk-pk)
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s) SSC ≤ -0.5%	-	0.098	0.128	3.1	ps (RMS)
		PCIe Gen2 Lo Band (5.0 GT/s) SSC ≤ -0.5%	-	0.028	0.032	3	ps (RMS)
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s) SSC ≤ -0.5%	-	0.042	0.061	1	ps (RMS)
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [c] [d] SSC ≤ -0.5%	-	0.042	0.061	0.5	ps (RMS)
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [c] [e] SSC ≤ -0.5%	-	0.014	0.024	0.15	ps (RMS)
$t_{jphPCIeG1-SRIS}$	Additive PCIe Phase Jitter (SRIS Architecture) [6]	PCIe Gen1 (2.5 GT/s) SSC ≤ -0.3%	-	-	-	N/A	ps (pk-pk)
$t_{jphPCIeG2-SRIS}$		PCIe Gen2 Band (5.0 GT/s) SSC ≤ -0.3%	-	0.126	0.160	N/A	ps (RMS)
$t_{jphPCIeG3-SRIS}$		PCIe Gen3 (8.0 GT/s) SSC ≤ -0.3%	-	0.033	0.042	N/A	ps (RMS)
$t_{jphPCIeG4-SRIS}$		PCIe Gen4 (16.0 GT/s) [3] [4] SSC ≤ -0.3%	-	0.034	0.044	N/A	ps (RMS)
$t_{jphPCIeG5-SRIS}$		PCIe Gen5 (32.0 GT/s) [3] [5] SSC ≤ -0.3%	-	0.029	0.038	N/A	ps (RMS)

Table 5. PCIe Phase Jitter (Zero-Delay Buffer Mode)[1] [2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Industry Limit	Unit
$t_{jphPCIeG1-CC}$	PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s), SSC ≤ -0.5% Any BW ZDB Mode	-	16	19	86	ps (pk-pk)
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s), SSC ≤ -0.5%, Any BW ZDB Mode	-	0.5	0.64	3.1	ps (RMS)
		PCIe Gen2 Lo Band (5.0 GT/s), SSC ≤ -0.5%, Any BW ZDB Mode	-	0.6	0.7	3	ps (RMS)
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s), SSC ≤ -0.5%, High BW ZDB Mode	-	0.33	0.38	1	ps (RMS)
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [3] [4] SSC ≤ -0.5%, High BW ZDB Mode	-	0.33	0.38	0.5	ps (RMS)
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [3] [5] SSC ≤ -0.5%, High BW ZDB Mode	-	0.1	0.13	0.15	ps (RMS)

Table 5. PCIe Phase Jitter (Zero-Delay Buffer Mode)[1] [2] (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Industry Limit	Unit
$t_{jphPCIeG2-SRIS}$	PCIe Phase Jitter (SRIS Architecture) [6]	PCIe Gen2 (5.0 GT/s), SSC ≤ -0.5% High BW ZDB Mode	-	1.36	1.65	N/A	ps (RMS)
$t_{jphPCIeG3-SRIS}$		PCIe Gen3 (8.0 GT/s), SSC ≤ -0.5% High BW ZDB Mode	-	0.45	0.52	N/A	ps (RMS)
$t_{jphPCIeG4-SRIS}$		PCIe Gen4 (16.0 GT/s), SSC ≤ -0.5% High BW ZDB Mode	-	0.47	0.54	N/A	ps (RMS)

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. Jitter may be subtracted from the limit using RSS subtraction to determine remaining margin. Confirmed by design and characterization, not 100% tested in production.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the N/A in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2. It is up to the user to divide the clock output budget or the clock input budget by √2 to arrive at a target limit.

Table 6. 12kHz to 20MHz Phase Jitter [1] [2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$t_{jph156M12k-20}$	Additive Phase Jitter, Fanout Mode	156.25MHz, 12kHz to 20MHz.	-	249	-	fs (rms)

1. Confirmed by design and characterization, not 100% tested in production.
2. Additive jitter is calculated using Root-Sum-Square (RSS) subtraction.

Table 7. Clock Input Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CROSS}	Input Crossover Voltage [1]	Crossover voltage.	150	-	900	mV
V_{SWING}	Input Swing [1]	Differential value.	300	-		mV
dv/dt	Input Slew Rate [1] [2]	Measured differentially.	0.4	-	8	V/ns
I_{IN}	Input Leakage Current	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5	-	5	µA
d_{tin}	Input Duty Cycle [1]	Differential measurement.	45	-	55	%
J_{DIFIn}	Input Jitter – Cycle to Cycle [1]		0	-	125	ps

1. Confirmed by design and characterization, not 100% tested in production.
2. Slew rate measured through ±75mV window centered around differential zero.

Table 8. Output Duty Cycle, Skew and PLL Characteristics [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
BW	PLL BW [2]	-3dB point in High BW Mode (100MHz).	2	2.8	4	MHz
		-3dB point in Low BW Mode (100MHz).	1	1.3	2	MHz
t_{JPEAK}	PLL Jitter Peaking	Peak Pass band gain (100MHz).	-	1.1	2	dB
t_{DC}	Duty Cycle [3]	Measured differentially, PLL Mode.	45	50	55	%
t_{DCD}	Duty Cycle Distortion [3] [4]	Measured differentially, Bypass Mode.	-1	-0.9	1	%
t_{pdBYP}	Skew, Input to Output [5]	Bypass Mode, V_T = 50%.	1400	1884	2200	ps
t_{pdPLL}		PLL Mode V_T = 50%.	-100	9	100	ps
t_{sk3}	Skew, Output to Output [5]	V_T = 50%.	-	32	50	ps
$t_{jcyc-cyc}$	Jitter, Cycle to Cycle	PLL Mode.	-	21	50	ps

1. Confirmed by design and characterization, not 100% tested in production.
2. The Minimum/Typical/Maximum values of each BW setting track each other, i.e., maximum low BW will never occur with minimum high BW.
3. Measured from differential waveform.
4. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
5. All outputs at default slew rate.

Table 9. LP-HCSL (DIF) Output Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
dV/dt	Slew Rate [1] [2] [3]	Scope averaging on, fast setting.	2.9	3.7	4.7	V/ns
		Scope averaging on, slow setting.	2	2.7	3.7	
ΔtR/tF	Rise/Fall Matching [1] [4]	Single-ended measurement.	-	6	20	%
V_{HIGH}	Voltage High [5]	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	761	850	mV
V_{LOW}	Voltage Low [5]		-150	-7	150	
Vmax	Max Voltage [5]	Measurement on single ended signal using absolute value (scope averaging off).	-	819	1150	
Vmin	Min Voltage [5]		-300	-46	-	
Vcross_abs	Crossing Voltage (abs) [1] [6]	Scope averaging off.	250	409	550	
Δ-Vcross	Crossing Voltage (var) [1] [7]	Scope averaging off.	-	14	140	

1. Confirmed by design and characterization, not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.
4. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
5. At default SMBus settings.
6. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
7. The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Table 10. Current Consumption – 9DBL02xxC

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDDIG}	Operating Supply Current, ZDB Mode	VDDDIG, all outputs at 100MHz.	-	0.8	1	mA
$I_{DDO+O+R}$		VDDA+VDDO+VDDR, all outputs at 100MHz.	-	30	35	mA
I_{DDDIG}	Operating Supply Current, Fanout (bypass) Mode	VDDDIG, all outputs at 100MHz	-	0.5	1	mA
$I_{DDO+O+R}$		VDDA+VDDO+VDDR, all outputs at 100MHz.	-	22	26	mA
$I_{DDDIGPD}$	Powerdown Current[1]	VDDDIG, CKPWRGD_PD# = 0.	-	0.5	0.6	mA
$I_{DDO+O+RPD}$		VDDA+VDDO+VDDR, CKPWRGD_PD# = 0.	-	2.1	2.5	mA

1. Input clock stopped.

Table 11. Current Consumption – 9DBL04xxC

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDDIG}	Operating Supply Current, ZDB Mode	VDDDIG, all outputs at 100MHz	-	0.8	1	mA
$I_{DDO+O+R}$		VDDA+VDDO+VDDR, all outputs at 100MHz.	-	37	44	mA
I_{DDDIG}	Operating Supply Current, Fanout (bypass) Mode	VDDDIG, all outputs at 100MHz	-	0.5	1	mA
$I_{DDO+O+R}$		VDDA+VDDO+VDDR, all outputs at 100MHz.	-	30	36	mA
$I_{DDDIGPD}$	Powerdown Current[1]	VDDDIG, CKPWRGD_PD# = 0.	-	0.5	1	mA
$I_{DDO+O+RPD}$		VDDA+VDDO+VDDR, CKPWRGD_PD# = 0.	-	1.9	3	mA

1. Input clock stopped.

Table 12. Current Consumption – 9DBL06xxC

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDA}	Operating Supply Current, PLL Mode	VDDA, PLL Mode at 100MHz.	-	8.1	10	mA
I_{DDDIG}		VDDDIG, all outputs active at 100MHz.	-	0.80	1.0	mA
I_{DD+R}		VDD3.3 + VDDR, all outputs active at 100MHz.	-	18	22	mA
I_{DDIO}		VDDIO, all outputs active at 100MHz.		22	26	mA
I_{DDA}	Operating Supply Current, BP Mode	VDDA, BP Mode, at 100MHz.	-	0.94	1.1	mA
I_{DDDIG}		VDDDIG, BP Mode, all outputs active at 100MHz.	-	0.49	0.6	mA
I_{DD+R}		VDD3.3 + VDDR, BP Mode, all outputs active at 100MHz.	-	17	20	mA
I_{DDIO}		VDDIO, BP Mode, all outputs active at 100MHz.		22	26	mA
I_{DDAPD}	Powerdown Current[1]	VDDA, CKPWRGD_PD# = 0.	-	0.94	1.1	mA
$I_{DDDIGPD}$		VDDIG, CKPWRGD_PD# = 0.	-	0.49	0.6	mA
I_{DD+RPD}		VDD3.3 + VDDR, CKPWRGD_PD# = 0.	-	1.04	1.3	mA
I_{DDIOPD}		VDDIO, CKPWRGD_PD# = 0.		0.04	0.1	mA

1. Input clock stopped.

Table 13. Current Consumption – 9DBL08xxC

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDA}	Operating Supply Current, PLL Mode	VDDA, PLL Mode at 100MHz.	-	7.9	10	mA
I_{DDDIG}		VDDDIG, all outputs active at 100MHz.	-	0.8	1.0	mA
I_{DD+R}		VDD3.3 + VDDR, all outputs active at 100MHz.	-	20.1	25	mA
I_{DDIO}		VDDIO, all outputs active at 100MHz.		27.6	33	mA
I_{DDA}	Operating Supply Current, BP Mode	VDDA, BP Mode, at 100MHz.	-	0.9	1.1	mA
I_{DDDIG}		VDDDIG, BP Mode, all outputs active at 100MHz.	-	0.5	0.6	mA
I_{DD+R}		VDD3.3 + VDDR, BP Mode, all outputs active at 100MHz.	-	18.4	23	mA
I_{DDIO}		VDDIO, BP Mode, all outputs active at 100MHz.		28.2	33	mA

Table 13. Current Consumption – 9DBL08xxC (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDAPD}	Powerdown Current[1]	VDDA, CKPWRGD_PD# = 0.	-	0.92	1.1	mA
$I_{DDDIGPD}$		VDDx, CKPWRGD_PD# = 0.	-	0.5	0.6	mA
I_{DD+RPD}		VDD3.3 + VDDR, CKPWRGD_PD# = 0.	-	1.4	2	mA
I_{DDIOPD}		VDDIO, CKPWRGD_PD# = 0.		0.039	0.1	mA

1. Input clock stopped.

Table 14. Input/Supply/Common Parameters – Normal Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VDDx	Supply Voltage	Supply voltage for core and analog.	3.135	3.3	3.465	V
VDDIO	Output Supply Voltage [1]	Supply voltage for Low Power HCSL outputs.	0.95	1.05-3.3	3.465	V
T_{AMB}	Ambient Operating Temperature	Industrial range.	-40	25	85	°C
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus.	0.75 V_{DDx}	-	V_{DDx} + 0.3	V
V_{IL}	Input Low Voltage		-0.3	-	0.25 V_{DDx}	V
V_{IHtri}	Input High Voltage	Single-ended tri-level inputs ('_tri' suffix).	0.75 V_{DDx}	-	V_{DD} + 0.3	V
V_{IMtri}	Input Mid Voltage		0.4 V_{DDx}	0.5 V_{DDx}	0.6 V_{DDx}	V
V_{ILtri}	Input Low Voltage		-0.3		0.25 V_{DDx}	V
IIL_{OE}	OE Input Leakage	V_{IN} = 0V	-1	-	1	µA
IIH_{OE}		V_{IN} = V_{DD}	20	-	35	µA
IIL_{PWRGD_PD}	PWRGD_PD Input Leakage	V_{IN} = 0V	-35	-	-20	µA
IIH_{PWRGD_PD}		V_{IN} = V_{DD}	-1	-	1	µA
$IIL_{HI_BYP_LO}$	HI_BYP_LO Input Leakage	V_{IN} = 0V	-35	-	-20	µA
$IIM_{HI_BYP_LO}$		V_{IN} = V_{DD}/2	-1	-	1	µA
$IIH_{HI_BYP_LO}$		V_{IN} = V_{DD}	20	-	35	µA
IIL_{SAR_Tri}	SADR_Tri Input Leakage	V_{IN} = 0V	-1	-	1	µA
IIM_{SAR_Tri}		V_{IN} = V_{DD}/2	5	-	20	µA
IIH_{SAR_Tri}		V_{IN} = V_{DD}	20	-	35	µA
$IIL_{SCLK, SDATA}$	SMBUS Input Leakage	V_{IN} = 0V	-1	-	1	µA
$IIH_{SCLK, SDATA}$		V_{IN} = V_{DD}	-1	-	1	µA
F_{IN}	Input Frequency	Bypass Mode.	1	-	200	MHz
		100MHz PLL Mode.	60	100.00	140	MHz
		50MHz PLL Mode.	30	50.00	65	MHz
		125MHz PLL Mode.	75	125.00	175	MHz
L_{pin}	Pin Inductance [2]	-	-	-	7	nH
C_{IN}	Capacitance [2]	Logic Inputs, except DIF_IN.	1.5	-	5	pF
C_{INDIF_IN}		DIF_IN differential clock inputs.	1.5	-	2.7	pF
C_{OUT}		Output pin capacitance.	-	-	6	pF

Table 14. Input/Supply/Common Parameters – Normal Operating Conditions (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T_{STAB}	Clk Stabilization [3]	From V_{DD} Power-Up and after input clock stabilization or deassertion of PD# to 1st clock.	-	-	1	ms
$f_{SSCMODIN}$	Input SS Modulation Frequency	PCIe applications.	30	-	33	kHz
		Non-PCIe applications.	0	-	66	kHz
$t_{LATOE\#}$	OE# Latency [2] [3]	DIF start after OE# assertion DIF stop after OE# deassertion.	3	4	5	clocks
t_F	Tfall [3]	Fall time of single-ended control inputs.	-	-	5	ns
t_R	Trise [3]	Rise time of single-ended control inputs.	-	-	5	ns

1. Only present on 9DBL06xxC and 9DBL08xxC devices.
2. Confirmed by design and characterization, not 100% tested in production.
3. Control inputs must be monotonic from 20% to 80% of input swing.

Table 15. SMBus Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{ILSMB}	SMBus Input Low Voltage	V_{DDSMB} = 3.3V.	-	-	0.8	V
V_{IHSMB}	SMBus Input High Voltage	V_{DDSMB} = 3.3V.	2.1	-	3.6	V
V_{OLSMB}	SMBus Output Low Voltage	At $I_{PULLUP.}$	-	-	0.4	V
I_{PULLUP}	SMBus Sink Current	At $V_{OL.}$	4	-		mA
V_{DDSMB}	Nominal Bus Voltage		2.7	-	3.6	V
t_{RSMB}	SCLK/SDATA Rise Time [1]	(Max VIL - 0.15) to (Min VIH + 0.15).	-	-	1000	ns
t_{FSMB}	SCLK/SDATA Fall Time [1]	(Min VIH + 0.15) to (Max VIL - 0.15).	-	-	300	ns
f_{SMB}	SMBus Operating Frequency [2] [3]	SMBus operating frequency.	-	-	500	kHz

1. Confirmed by design and characterization, not 100% tested in production.
2. The device must be powered up for the SMBus to function.
3. The differential input clock must be running for the SMBus to be active.

2.4 Power Management

Table 16. Power Management

CKPWRGD_PD#	CLK_IN	SMBus OEn bit	OEn# Pin	DIFn	DIFn#	PLL State (ZDB Mode)
0	X	X	X	Low [1]	Low [1]	Off
1	Running	0	X	Low [1]	Low [1]	On [2]
1	Running	1	0	Running	Running	On [2]
1	Running	1	1	Low [1]	Low [1]	On [2]

1. The output state is set by B11[1:0] (Low/Low default).
2. If Bypass mode is selected, the PLL will always be off.

2.5 ZDB Operating Mode

Table 17. ZDB (PLL) Operating Mode[1]

HiBW_BypM_LoBW#	Operating Mode	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	Low Bandwidth PLL (ZDB) Mode	00	00
Mid-level (VDD/2)	Bypass Mode (Fanout buffer)	01	01
1	High Bandwidth PLL (ZDB) Mode	11	11

1. '10' value is reserved.

3. Test Loads

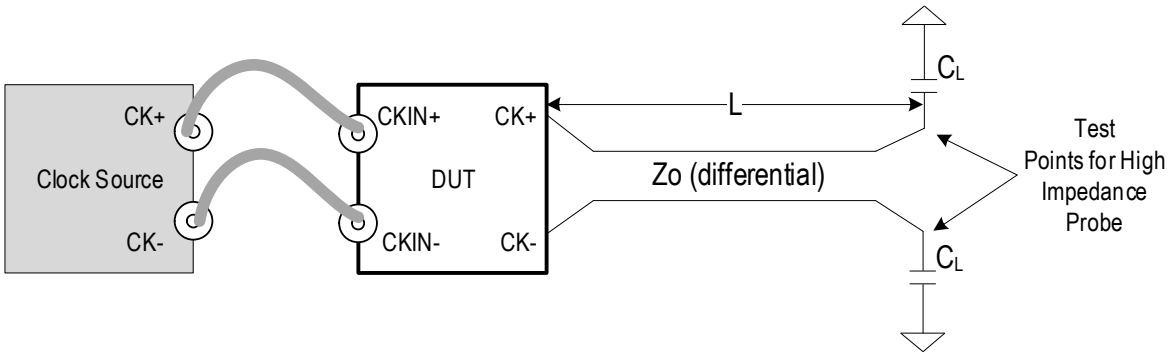


Figure 6. Test Load for AC/DC Measurements and ZDB Mode PCIe Jitter Measurements

Table 18. Parameters for Measurements Using Test Setup in Figure 6 [1]

Parameters Measured	Clock Source	Device Under Test (DUT)	Differential Zo (Ω)	L (cm)	C_L (pF)
AC/DC Parameters	SMA100B	9DBLxx5xC	85	12.7	2
	SMA100B	9DBLxx4xC	100	12.7	2
ZDB-Mode PCIe Jitter	9SQ440	9DBLxx5xC	85	12.7	2
	9SQ440	9DBLxx4xC	100	12.7	2

1. A DSO is used for all measurements in this table. Equipment noise is removed from all jitter measurements taken with this setup.

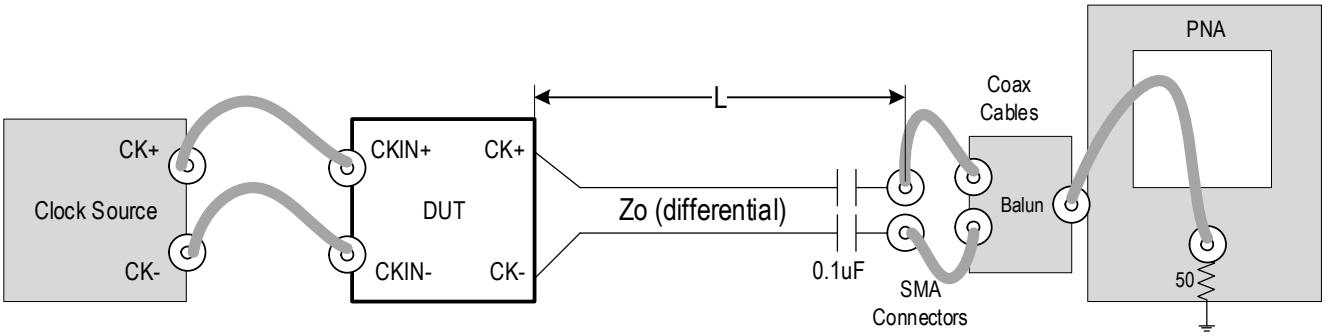


Figure 7. Test Loads for Additive Phase Jitter Measurements

Table 19. Parameters for Measurements Using Test Setup in Figure 7

Parameters Measured	Clock Source	Device Under Test (DUT)	Differential Zo (Ω)	L (cm)	C_L (pF)
Fanout Buffer Mode Additive Phase Jitter	SMA100B	9DBLxx5xC	85	12.7	2
	SMA100B	9DBLxx4xC	100	12.7	2
ZDB Mode Jitter	9SQ440	9DBLxx5xC	85	12.7	2
	9SQ440	9DBLxx4xC	100	12.7	2

4. Alternate Terminations

The LP-HCSL output can easily drive other logic families. See “AN-891 Driving LVPECL, LVDS, and CML Logic with “Universal” Low-Power HCSL Outputs” for termination schemes for LVPECL, LVDS, CML and SSTL.

4.1 Alternate HCSL Terminations

Device	Differential Zo (Ω)	Rs (Ω)
9DBLxx4xC	85	N/A
9DBLxx4xC	100	None Needed
9DBLxx5xC	85	None Needed
9DBLxx5xC	100	7.5

5. General SMBus Serial Interface Information

5.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

5.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 20. SMBus Address Selection

State of SADR_tri pin on first high assertion of CKPWRGD_PD#	Address[1]
0	1101011x
M	1101100x
1	1101101x

1. 'x' is the Read/Write bit.

Table 21. Byte 0: Output Enable Control

Byte 0	Bit	7	6	5	4	3	2	1	0
	Function	Output Enable	-	-	-	-	-	-	-
	Type	RW	RW	RW	RW	RW	RW	RW	RW
Device	Definition	0 = Output is disabled [1] 1 = OE# Pin Controls Output							
9DBL08xxC	Name	DIF7oe	DIF6oe	DIF5oe	DIF4oe	DIF3oe	DIF2oe	DIF1oe	DIF0oe
	Default	1	1	1	1	1	1	1	1
9DBL06xxC	Name	DIF5oe	DIF4oe	Reserved	DIF3oe	DIF2oe	DIF1oe	Reserved	DIF0oe
	Default	1	1	–	1	1	1	–	1
9DBL04xxC	Name	Reserved	DIF3oe	Reserved	DIF2oe	DIF1oe	Reserved	DIF0oe	Reserved
	Default	-	1	-	1	1	-	1	-
9DBL02xxC	Name	Reserved			DIF1oe	DIF0oe	Reserved		
	Default	-	-	-	1	1	-	-	-

1. See Byte11[1:0] for disabled state.

Table 22. Byte 1: PLL Operating Mode and Output Amplitude Control

Byte 1	Bit	7	6	5	4	3	2	1	0
	Function	PLL Mode Readback		Enable software PLL Mode control	Software PLL Mode Control [1]		-	Output Amplitude	
	Type	R	R	RW	RW	RW	-	RW	RW
	Definition	See Table 17 (ZDB Operating Mode)		0 = B1[7:6] sets PLL Mode 1 = B1[4:3] sets PLL Mode	See Table 17 (ZDB Operating Mode)		Reserved	00 = 0.60V 01 = 0.68V 10 = 0.75V 11 = 0.85V	
All Devices	Name	PLLrbk1	PLLrbk0	PLLmdctrl	PLLmd1	PLLmd0	-	Amp1	Amp0
	Default	Latch	Latch	0	0	0	1	1	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

Table 23. Byte 2: Slew Rate Control 0

Byte 2	Bit	7	6	5	4	3	2	1	0
	Function	Slew Rate Selection							
	Type	RW	RW	RW	RW	RW	RW	RW	RW
Device	Definition	0 = Slow Setting 1 = Fast Setting See electrical characteristics for actual slew rates.							
9DBL08xxC	Name	DIF7slew	DIF6slew	DIF5slew	DIF4slew	DIF3slew	DIF2slew	DIF1slew	DIF0slew
	Default	1	1	1	1	1	1	1	1
9DBL06xxC	Name	DIF5slew	DIF4slew	Reserved	DIF3slew	DIF2slew	DIF1slew	Reserved	DIF0slew
	Default	1	1	-	1	1	1	-	1
9DBL04xxC	Name	Reserved	DIF3slew	Reserved	DIF2slew	DIF1slew	Reserved	DIF0slew	Reserved
	Default	-	1	-	1	1	-	1	-
9DBL02xxC	Name	Reserved			DIF1slew	DIF0slew	Reserved		
	Default	-	-	-	1	1	-	-	-

Table 24. Byte 3: ZDB Mode Frequency Select and Feedback Slew Rate Control

Byte 3	Bit	7	6	5	4	3	2	1	0
-	Function	-	-	Enable software (SW) selection of ZDB frequency	ZDB Frequency Select [1]		-	-	Feedback Slew Rate
-	Type	-	-	RW	RW	RW	-	-	RW
-	Definition	Reserved		0 = SW frequency select disabled 1 = SW frequency select enabled	00 = 100M 01 = 50M 10 = 125M 11= Reserved		Reserved		0 = Slow Setting 1 = Fast Setting
All Devices	Name	-	-	FSelEn	FSel1	Fsel0	-	-	FBKslew
	Default	1	1	0	0	0	1	1	1

1. B3[5] must be set to a 1 for these bits to have any effect on the part.

Byte 4 is Reserved

Table 25. Byte 5: Revision ID/Vendor ID

Byte 5	Bit	7	6	5	4	3	2	1	0
-	Function	Revision ID				VENDOR ID			
-	Type	R	R	R	R	R	R	R	R
All Devices	Name	RID3	RID2	RID1	RID0	VID3	VID2	VID1	VID0
	Default	C rev = 0010				0001 = IDT			

Table 26. Byte 6: Device Type/Device ID

Byte 6	Bit	7	6	5	4	3	2	1	0
-	Function	Device Type		Device ID					
-	Type	R	R	R	R	R	R	R	R
All Devices	Name	DevType 1	DevType0	Dev ID5	Dev ID4	Dev ID3	Dev ID2	Dev ID1	Dev ID0
	Default	01 = DBx ZDB/FOB		9DBL08x1C = 0b001000 9DBL06x1C = 0b000110 9DBL04x2C = 0b000100 9DBL02x2C = 0b000010					

Table 27. Byte 7: Byte Count

Byte 7	Bit	7	6	5	4	3	2	1	0
-	Function	-	-	-	Byte Count Programming				
-	Type	-	-	-	RW	RW	RW	RW	RW
Device	Definition	Reserved			Writing to this register will configure how many bytes will be read back on a block read. Default is = 8 bytes.				
All	Name	-	-	-	BC4	BC3	BC2	BC1	BC0
-	Default	0	0	0	0	1	0	0	0

Bytes 8 and 9 are reserved

Table 28. Byte 10: Power-Down (PD) Restore

Byte 10	Bit	7	6	5	4	3	2	1	0
-	Function	-	Restore Default Config in Power Down	-	-	-	-	-	-
-	Type	-	RW	-	-	-	-	-	-
-	Definition	Reserved	0 = Clear Config. in Power Down 1 = Keep Config. in Power Down	Reserved					
All Devices	Name	-	PD_Restore	-	-	-	-	-	-
	Default	Reserved	1	0	0	0	0	0	0

Table 29. Byte 11: Impedance Control 0 and Stop State

Byte 11	Bit	7	6	5	4	3	2	1	0
-	Function	Output Impedance - Feedback		-	-	-	-	DIF/DIF# Disable State	
-	Type	RW	RW	-	-	-	-	RW	RW
Device	Definition	00 = Reserved 01 = 85ohm 10 = 100ohm 11 = Reserved		Reserved				00 = Low/Low 01 = HiZ/HiZ 10 = High/Low 11 = Low/High	
All	Name	FBz1	FBz0	-	-	-	-	Stop1	Stop0
	Default	10 = 9DBLxx4xC 01 = 9DBLxx5xC		0	0	0	0	0	0

Table 30. Byte 12: Impedance Control 1

Byte 12	Bit	7	6	5	4	3	2	1	0
-	Function	Output Impedance							
-	Type	RW	RW	RW	RW	RW	RW	RW	RW
Device	Definition	00 = Reserved, 01 = 85ohm, 10 = 100ohm, 11 = Reserved							
9DBL08xxC	Name	DIF3z1	DIF3z0	DIF2z1	DIF2z0	DIF1z1	DIF1z0	DIF0z1	DIF0z0
	Default	9DBL084xC= 0b10101010 9DBL085xC = 0b01010101							
9DBL06xxC	Name	DIF2z1	DIF2z0	DIF1z1	DIF1z0	Reserved		DIF0z1	DIF0z0
	Default	9DBL064xC = 0b1010xx10 9DBL065xC = 0b0101xx01							
9DBL04xxC	Name	DIF1z1	DIF1z0	Reserved		DIF0z1	DIF0z0	Reserved	
	Default	9DBL044xC = 0b10xx10xx 9DBL045xC = 0b01xx01xx							
9DBL02xxC	Name	DIF0z1	DIF0z0	Reserved					
	Default	9DBL024xC = 0b10xxxxxx 9DBL025xC = 0b01xxxxxx							

Table 31. Byte 13: Impedance Control 2

Byte 13	Bit	7	6	5	4	3	2	1	0
-	Function	Output Impedance							
-	Type	RW	RW	RW	RW	RW	RW	RW	RW
Device	Definition	00 = Reserved, 01 = 85ohm, 10 = 100ohm, 11 = Reserved							
9DBL08xxC	Name	DIF7z1	DIF7z0	DIF6z1	DIF6z0	DIF5z1	DIF5z0	DIF4z1	DIF4z0
	Default	9DBL084xC = 0b10101010 9DBL085xC = 0b01010101							
9DBL06xxC	Name	DIF5z1	DIF5z0	DIF4z1	DIF4z0	Reserved		DIF3z1	DIF3z0
	Default	9DBL064xC = 0b1010xx10 9DBL065xC = 0b0101xx01							
9DBL04xxC	Name	Reserved		DIF3z1	DIF3z0	Reserved		DIF2z1	DIF2z0
	Default	9DBL044xC = 0bxx10xx10 9DBL045xC = 0bxx01xx01							
9DBL02xxC	Name	Reserved						DIF1z1	DIF1z0
	Default	9DBL024xC = 0bxxxxxx10 9DBL025xC = 0bxxxxxx01							

Table 32. Byte 14: Pull-up/Pull-down Control 0

Byte 14	Bit	7	6	5	4	3	2	1	0
-	Function	Pull-up (PuP)/Pull-down (Pdwn) control							
-	Type	RW	RW	RW	RW	RW	RW	RW	RW
Device	Definition	00 = None, 01 = Pdwn, 10 = Pup, 11 = Pup+Pdwn							
9DBL08xxC	Name	OE3pu/pd1	OE3pu/pd0	OE2pu/pd1	OE2pu/pd0	OE1pu/pd1	OE1pu/pd0	OE0pu/pd1	OE0pu/pd0
	Default	0	1	0	1	0	1	0	1
9DBL06xxC	Name	OE2pu/pd1	OE2pu/pd0	OE1pu/pd1	OE1pu/pd0	Reserved		OE0pu/pd1	OE0pu/pd0
	Default	0	1	0	1	-	-	0	1
9DBL04xxC	Name	OE1pu/pd1	OE1pu/pd0	Reserved		OE0pu/pd1	OE0pu/pd0	Reserved	
	Default	0	1	-	-	0	1	-	-
9DBL02xxC	Name	OE0pu/pd1	OE0pu/pd0	Reserved					
	Default	0	1	-	-	-	-	-	-

Table 33. Byte 15: Pull-up/Pull-down Control 1

Byte 15	Bit	7	6	5	4	3	2	1	0
-	Function	Pull-up (PuP)/Pull-down (Pdwn) control							
-	Type	RW	RW	RW	RW	RW	RW	RW	RW
Device	Definition	00 = None, 01 = Pdwn, 10 = Pup, 11 = Pup+Pdwn							
9DBL08xxC	Name	OE7pu/pd1	OE7pu/pd0	OE6pu/pd1	OE6pu/pd0	OE5pu/pd1	OE5pu/pd0	OE4pu/pd1	OE4pu/pd0
	Default	0	1	0	1	0	1	0	1
9DBL06xxC	Name	OE5pu/pd1	OE5pu/pd0	OE4pu/pd1	OE4pu/pd0	Reserved		OE3pu/pd1	OE3pu/pd0
	Default	0	1	0	1	-	-	0	1
9DBL04xxC	Name	Reserved		OE3pu/pd1	OE3pu/pd0	Reserved		OE2pu/pd1	OE2pu/pd0
	Default	-	-	0	1	-	-	0	1
9DBL02xxC	Name	Reserved						OE1pu/pd1	OE1pu/pd0
	Default	-	-	-	-	-	-	0	1

Table 34. Byte 16: Pull-up_Pull-down Control 2

Byte 16	Bit	7	6	5	4	3	2	1	0
-	Function	-	-	-	-	-	-	Pull-up(PuP)/ Pull-down (Pdwn) control	
-	Type	-	-	-	-	-	-	RW	RW
Device	Definition	Reserved						00 = None, 01 = Pdwn, 10 = Pup, 11 = Pup+Pdwn	
All	Name	-	-	-	-	-	-	CKPWRGD_PD_ pu/pd1	CKPWRGD_PD_ pu/pd0
	Default	Reserved						1	0

Byte 17 is Reserved

Table 35. Byte 18: Polarity Control 0

Byte 18	Bit	7	6	5	4	3	2	1	0
-	Function	OE pin polarity							
-	Type	RW	RW	RW	RW	RW	RW	RW	RW
Device	Definition	0 = Output enabled when OE pin is Low 1 = Output enabled when OE pin is High							
9DBL08xxC	Name	OE7pol	OE6pol	OE5pol	OE4pol	OE3pol	OE2pol	OE1pol	OE0pol
	Default	0	0	0	0	0	0	0	0
9DBL06xxC	Name	OE5pol	OE4pol	Reserved	OE3pol	OE2pol	OE1pol	Reserved	OE0pol
	Default	0	0	0	0	0	0	0	0
9DBL04xxC	Name	Reserved	OE3pol	Reserved	OE2pol	OE1pol	Reserved	OE0pol	Reserved
	Default	0	0	0	0	0	0	0	0
9DBL02xxC	Name	Reserved			OE1pol	OE0pol	Reserved		
	Default	0	0	0	0	0	0	0	0

Table 36. Byte 19: Polarity Control 1

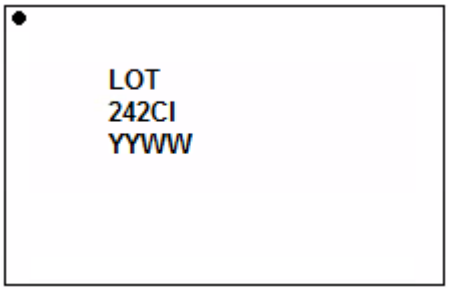
Byte 19	Bit	7	6	5	4	3	2	1	0
-	Function	-	-	-	-	-	-	-	CKPWRGD_PD pin polarity
-	Type	-	-	-	-	-	-	-	RW
-	Definition	Reserved							0 = Power Down when Low 1 = Power Down when High
All Devices	Name	-	-	-	-	-	-	-	CKPWRGD_Pdpol
	Default	0	0	0	0	0	0	0	0

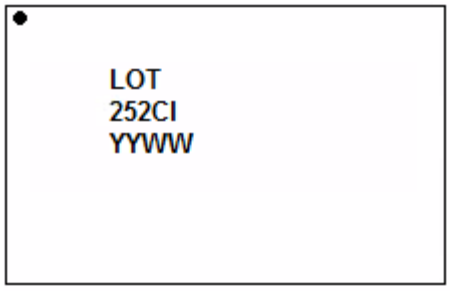
6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagrams

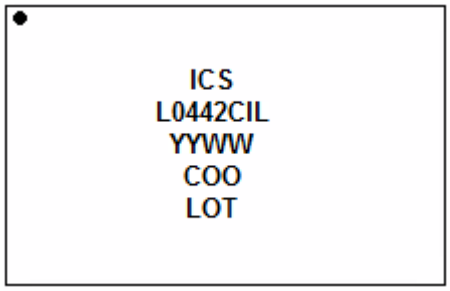
7.1 9DBL02x2C

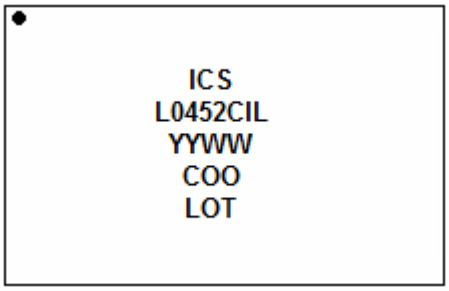




- Line 1: “LOT” is the lot sequence number.
- Line 2: truncated part number.
  - “I” denotes industrial temperature range.
- Line 3: “YYWW” is the last two digits of the year and work week that the part was assembled.

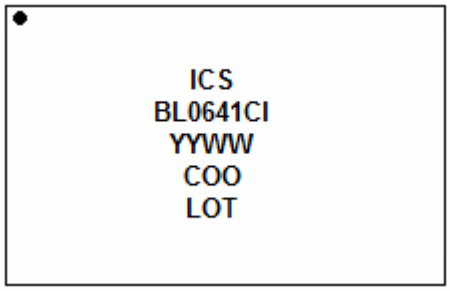
7.2 9DBL04x2C

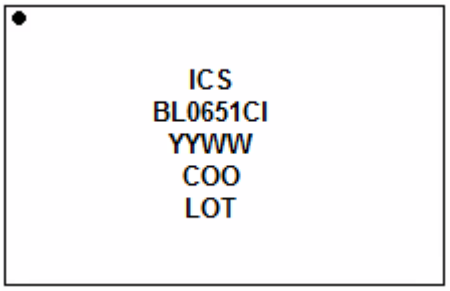




- Line 2: truncated part number.
  - “I” denotes industrial temperature range.
- Line 3: “YYWW” is the last two digits of the year and work week the part was assembled.
- Line 4: “COO” denotes country of origin.
- Line 5: “LOT” is the lot sequence number.

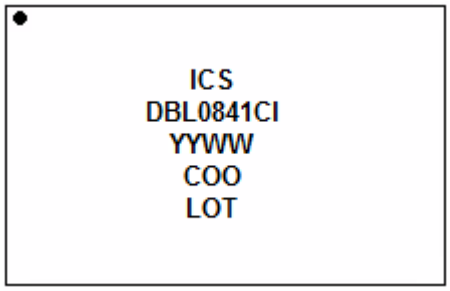
7.3 9DBL06x1C

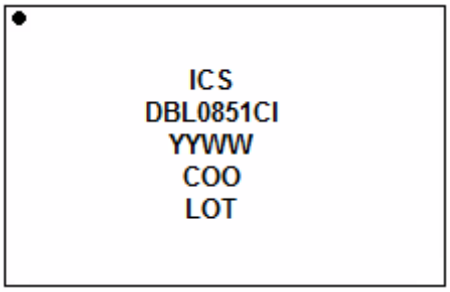




- Line 2: truncated part number.
  - “I” denotes industrial temperature range.
- Line 3: “YYWW” is the last two digits of the year and work week the part was assembled.
- Line 4: “COO” denotes country of origin.
- Line 5: “LOT” is the lot sequence number.

7.4 9DBL08x1C





- Line 2: truncated part number.
  - “I” denotes industrial temperature range.
- Line 3: “YYWW” is the last two digits of the year and work week the part was assembled.
- Line 4: “COO” denotes country of origin.
- Line 5: “LOT” is the lot sequence number.

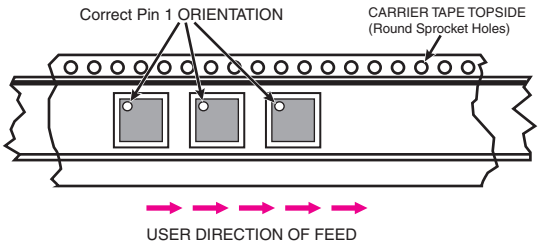
8. Ordering Information

Table 37. Ordering Information [1] [2] [3] [4]

Output Impedance (ohms)	Number of Clock Outputs	Package Description	Part Number	Carrier Type
85	2	24-VFQFPN - 4 × 4 × 0.9 mm, 0.50mm Pitch	9DBL0252CKILF	Tray
			9DBL0252CKILFT	“T” = Tape and Reel
	4	32-VFQFPN - 5 × 5 × 0.9 mm, 0.50mm Pitch	9DBL0452CKILF	Tray
			9DBL0452CKILFT	“T” = Tape and Reel
	6	40-VFQFPN - 5 × 5 × 0.9 mm, 0.40mm Pitch	9DBL0651CKILF	Tray
			9DBL0651CKILFT	“T” = Tape and Reel
	8	48-VFQFPN - 6 × 6 × 0.9 mm, 0.40mm Pitch	9DBL0851CKILF	Tray
			9DBL0851CKILFT	“T” = Tape and Reel
100	2	24-VFQFPN - 4 × 4 × 0.9 mm, 0.50mm Pitch	9DBL0242CKILF	Tray
			9DBL0242CKILFT	“T” = Tape and Reel
	4	32-VFQFPN - 5 × 5 × 0.9 mm, 0.50mm Pitch	9DBL0442CKILF	Tray
			9DBL0442CKILFT	“T” = Tape and Reel
	6	40-VFQFPN - 5 × 5 × 0.9 mm, 0.40mm Pitch	9DBL0641CKILF	Tray
			9DBL0641CKILFT	“T” = Tape and Reel
	8	48-VFQFPN - 6 × 6 × 0.9 mm, 0.40mm Pitch	9DBL0841CKILF	Tray
			9DBL0841CKILFT	“T” = Tape and Reel

1. “C” is the device revision designator (will not correlate with the datasheet revision).
2. “LF” denotes Pb-free configuration, RoHS compliant.
3. “I” indicates that all devices are specified over the -40°C to +85°C (industrial) temperature range.
4. “T” = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 38 for more details).

Table 38. Pin 1 Orientation in Tape and Reel Packaging

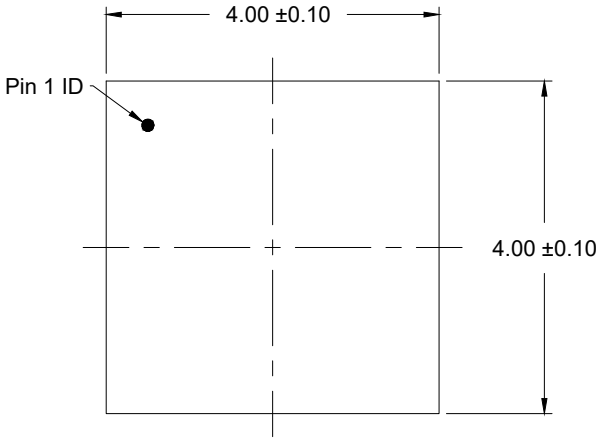
Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	

9. Revision History

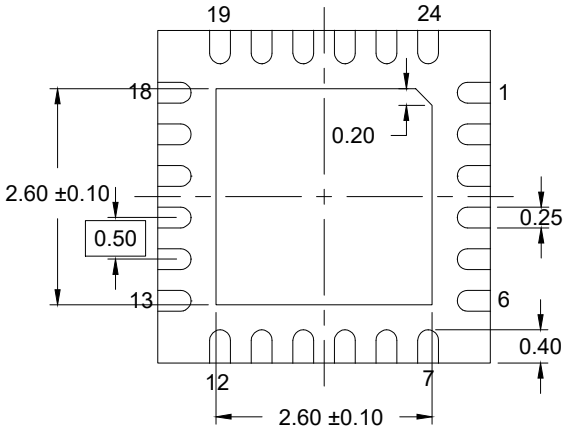
Revision	Date	Description
1.02	Nov 25, 2022	▪ Changed the default value of Bit 7 in Byte 10 to Reserved (see Table 28). ▪ Changed the default value of Bit 7-2 in Byte 16 to Reserved (see Table 34).
1.01	Jul 25, 2022	▪ Updated $I_{DDO+O+RPD}$ maximum value in Table 10. ▪ Updated I_{DDIOPD} maximum value in Table 13. ▪ Removed Single-ended Input Current parameter in Table 14.
1.00	Jul 7, 2022	Initial release.

Package Outline Drawing

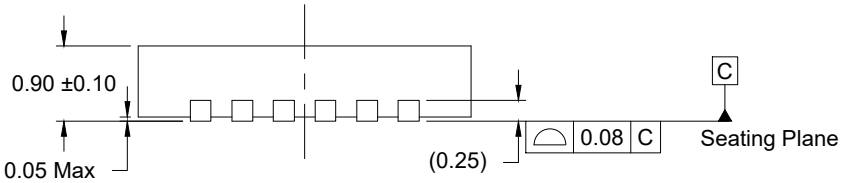
Package Code: NLG24P3
24-VFQFPN 4.0 x 4.0 x 0.90 mm Body, 0.5mm Pitch, Epad 2.60 x 2.60 mm
PSC-4192-03, Revision: 05, Date Created: July 13, 2022



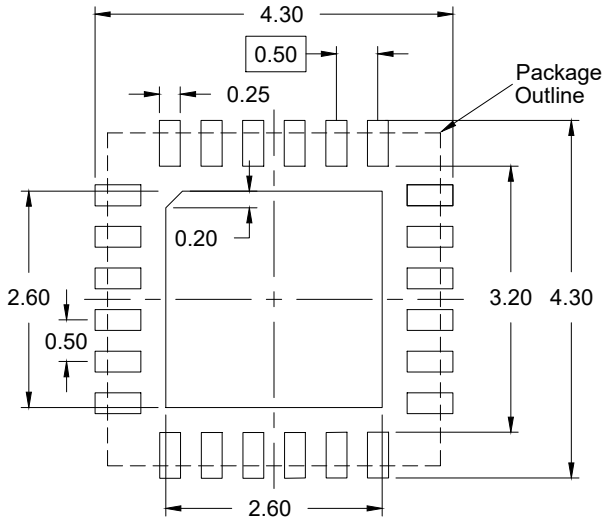
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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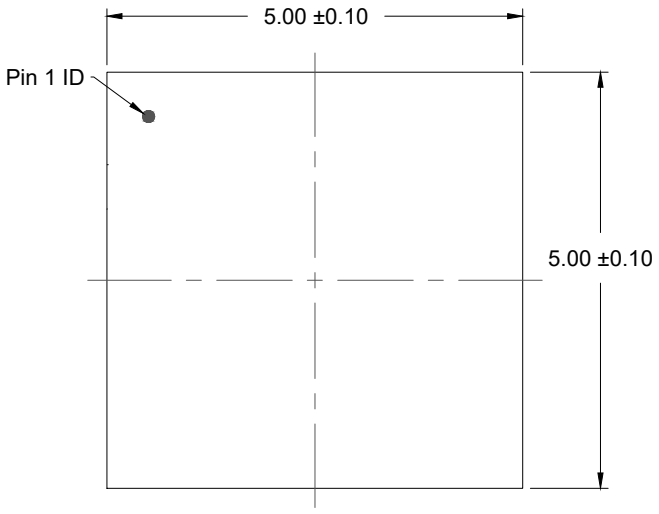
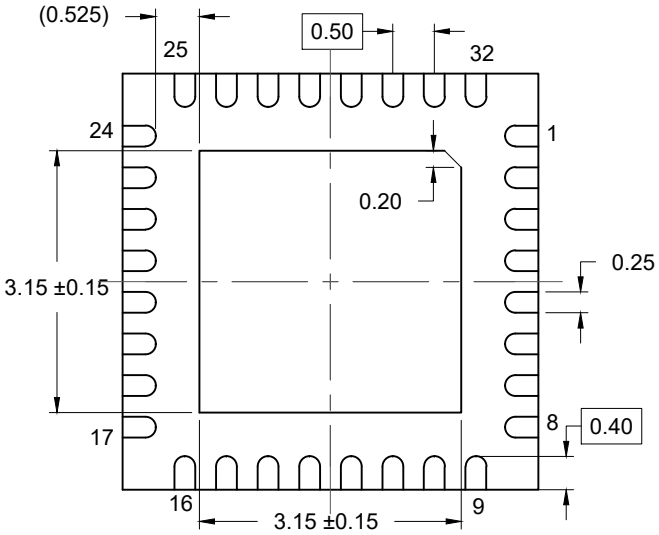
Package Outline Drawing

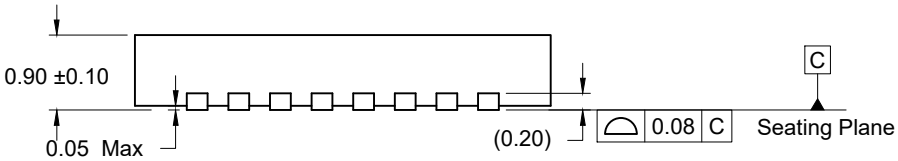
Package Code:NLG32P1
32-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4171-01, Revision: 04, Date Created: Aug 15, 2022



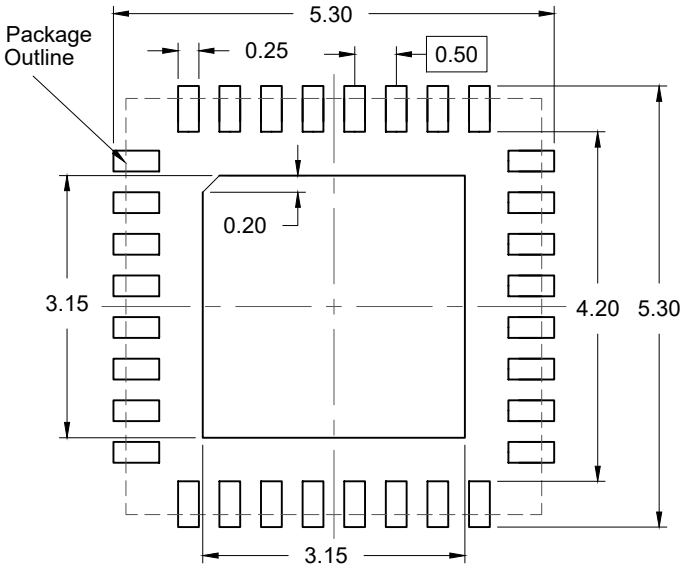
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

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2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
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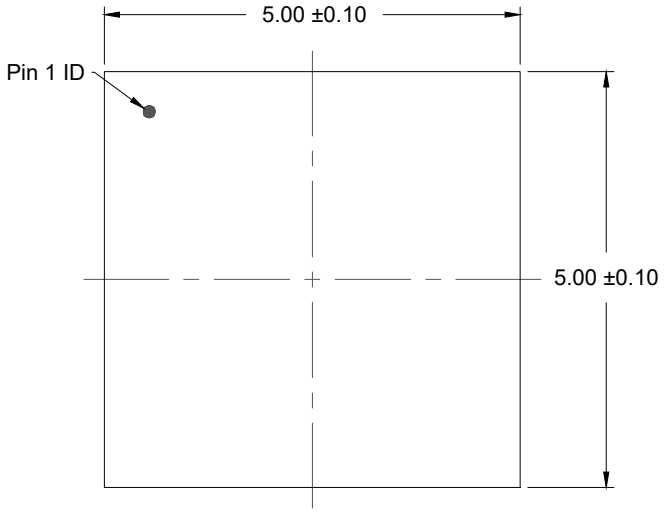
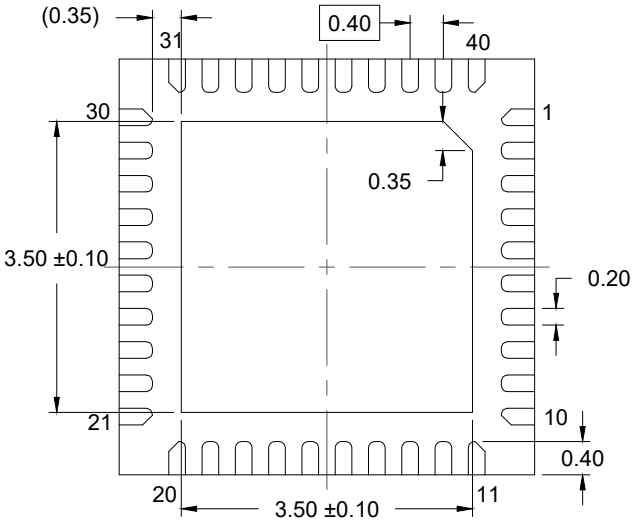
Package Outline Drawing

Package Code:NDG40P2
40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch
PSC-4292-02, Revision: 02, Date Created: Aug 30, 2022

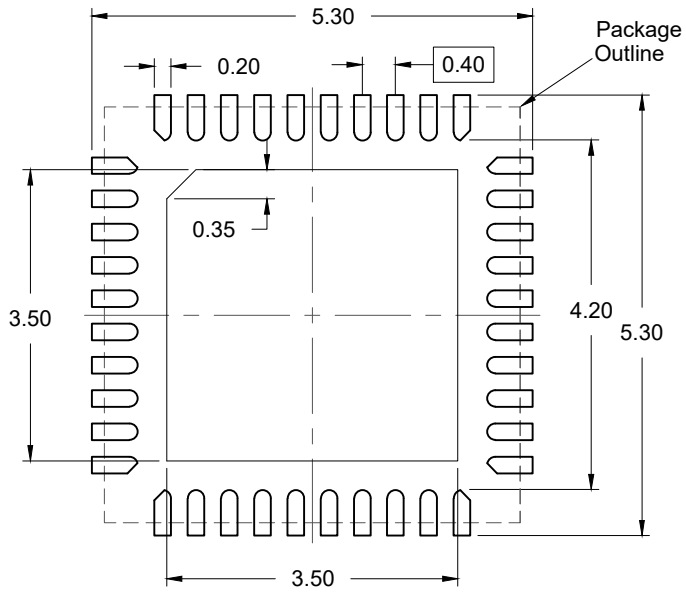


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
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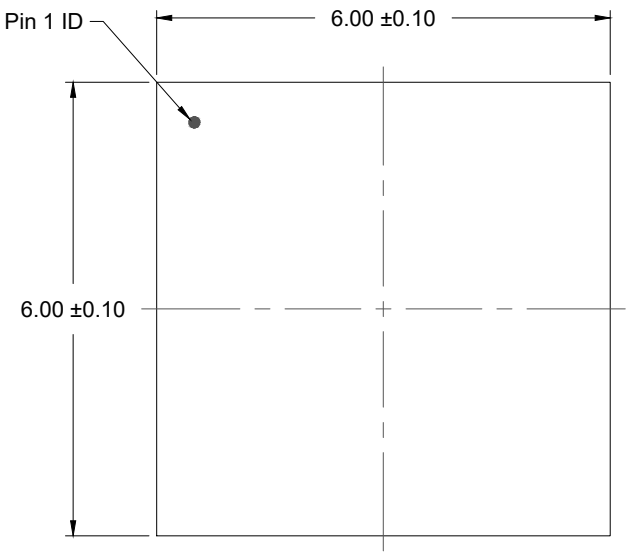
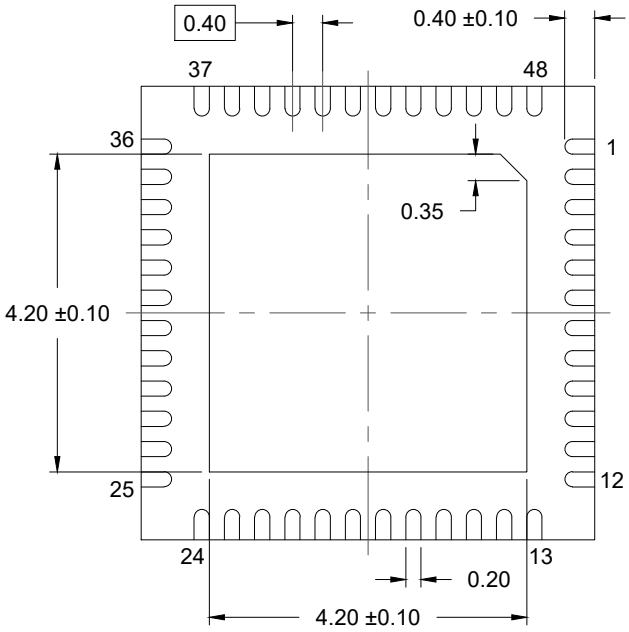
Package Outline Drawing

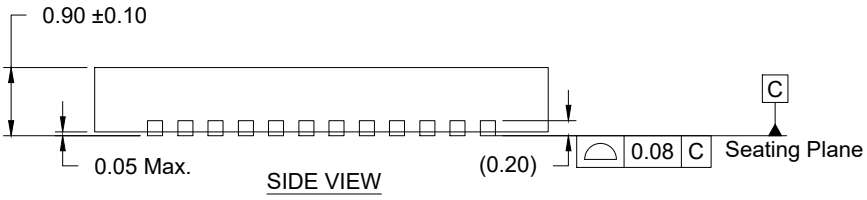
Package Code:NDG48P2
48-VFQFPN 6.0 x 6.0 x 0.9 mm Body, 0.4mm Pitch
PSC-4212-02, Revision: 04, Date Created: Sep 28, 2022



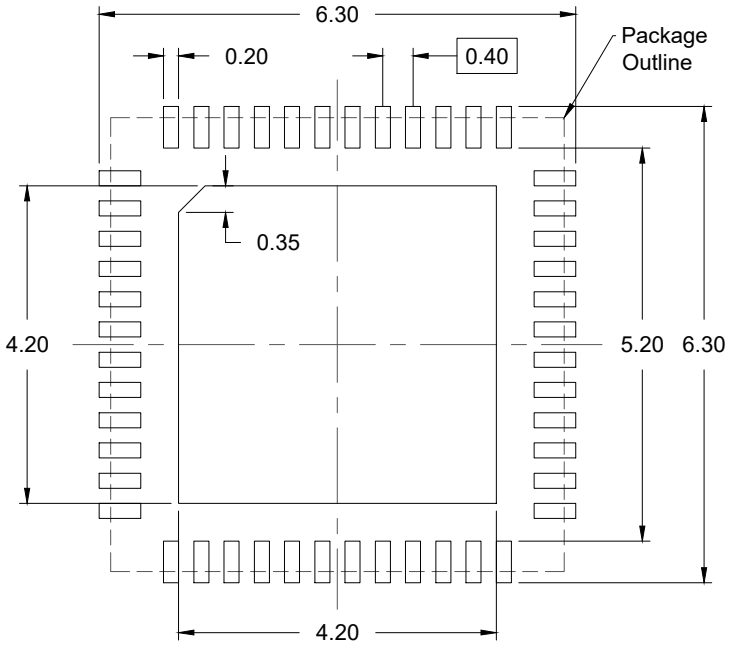
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

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