R9A06G037/NJM45001 PCB Design Guideline

PCB Layout Design Guide

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Summary

This material is a guideline on PCB layout for PLC board design by using R9A06G037, the PLC modem LSI by Renesas Electronics and NJM45001 as an AFE-IC. For device and power circuit design, follow guidelines and application notes of the target device.

Note that cautions on this material are based on general board design, and may not be applicable in some cases depending on the board size, parts, and layout.

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1. PLC Board Configuration Example

Figure 1-1 shows a PLC board configuration example using R9A06G037, the PLC modem LSI by Renesas Electronics and NJM45001 as an AFE-IC. This material explains cautions on PCB layout for PLC board design based on the configuration below.

The AFE-IC integrates the attenuator and the reception amplifier in this example. Even in cases where the AFE -IC doesn't integrate the reception path, the principle that is described in this document remains the same.

(Renesas Electronics can provide a reference board with the PLC board configuration shown in Figure 1-1 except for the AC-DC circuit.)

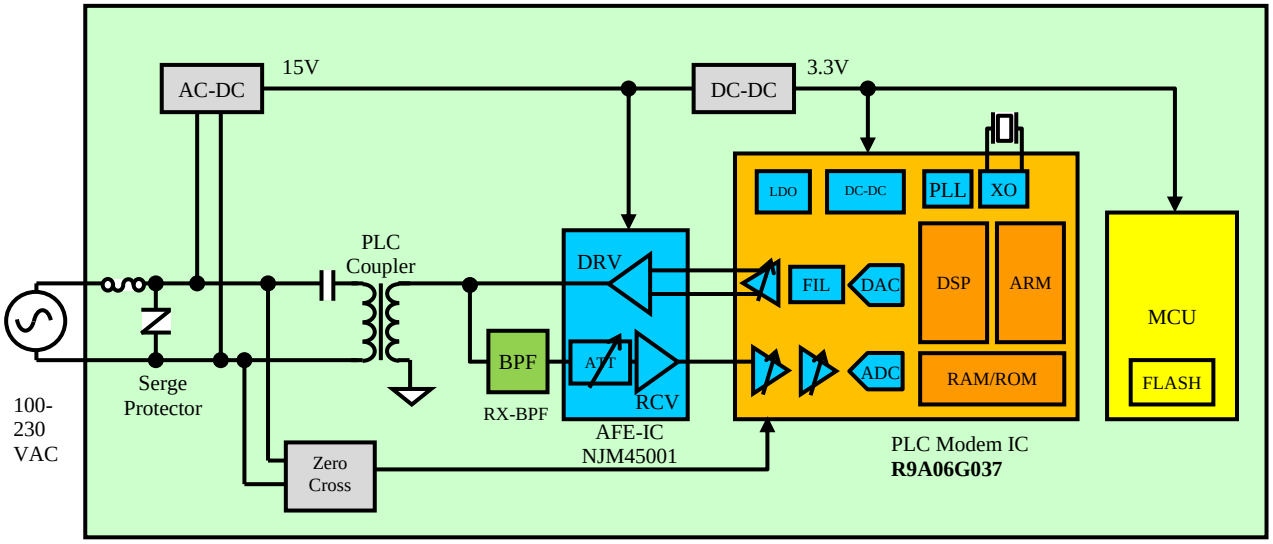


Figure 1-1 PLC Board Configuration Example

2. Cautions on the PLC Board and PCB Layout

This chapter explains cautions on PCB layout related to board parts and wiring. The PLC board consists of 2 domains: a high voltage circuit domain for 100V to 230V AC voltage, and a low voltage circuit domain for DC voltage of 1.1V, 3.3V, and 15V(or 12V in some cases. This material shows examples of using 15V). The following sections explain cautions on PCB layout for each domain respectively.

2.1 Cautions on Parts Layout for the High Voltage Circuit Domain

- The PCB patterns for the high voltage circuit domain and the low voltage circuit domain should be separated as shown in Figure 2-1.
- It is recommended to connect the high voltage circuit and the low voltage circuit with an insulating element such as a transformer (PLC Coupler) or photo-coupler (Zero Cross) for safety.
- For the insulating element part, it is recommended to insert a slit on the PCB to separate the PCB patterns for the high voltage circuit domain and the low voltage circuit domain.
- For the distance between LINE-NEUTRAL electrodes or between the high voltage circuit and the low voltage circuit, creeping/space distance should be designed in compliance with the safety standards of the target usage region. (An example is shown in Figure 2-3.)
- It is recommended to separate the PLC coupler and the AC-DC power supply circuit for 4cm or more as it may affect the EMC standards.

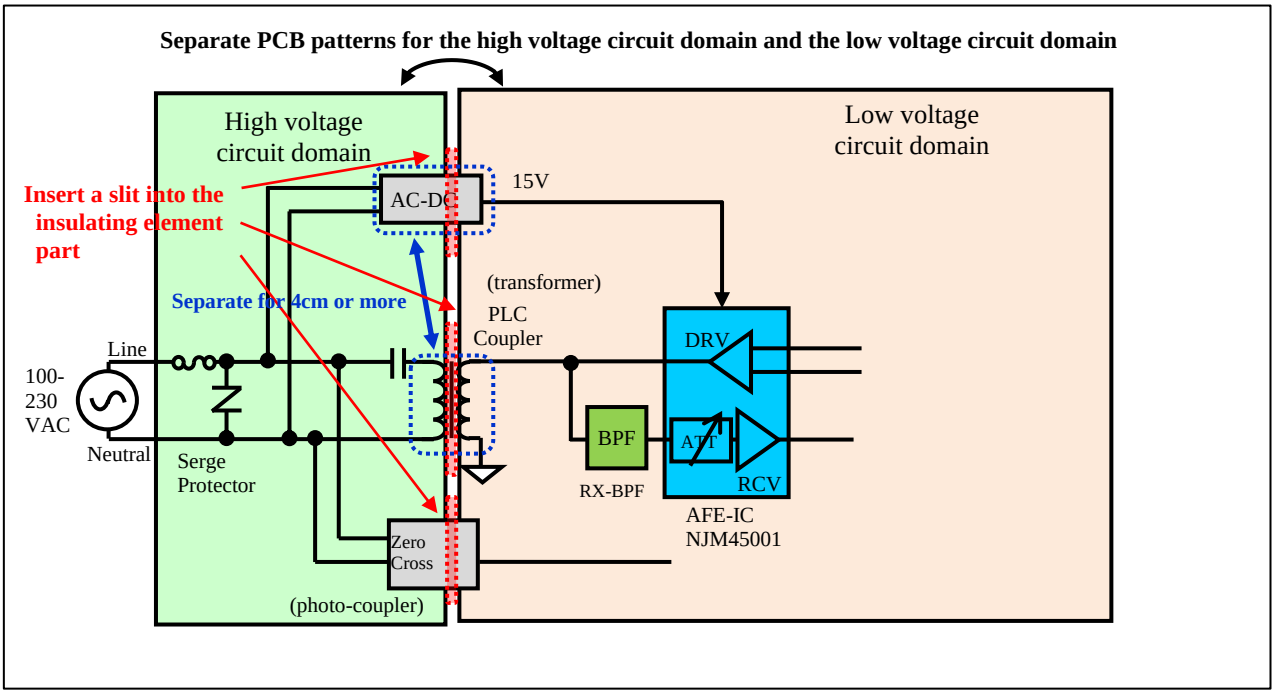


Figure 2-1 Parts Layout for High Voltage Circuit Domains

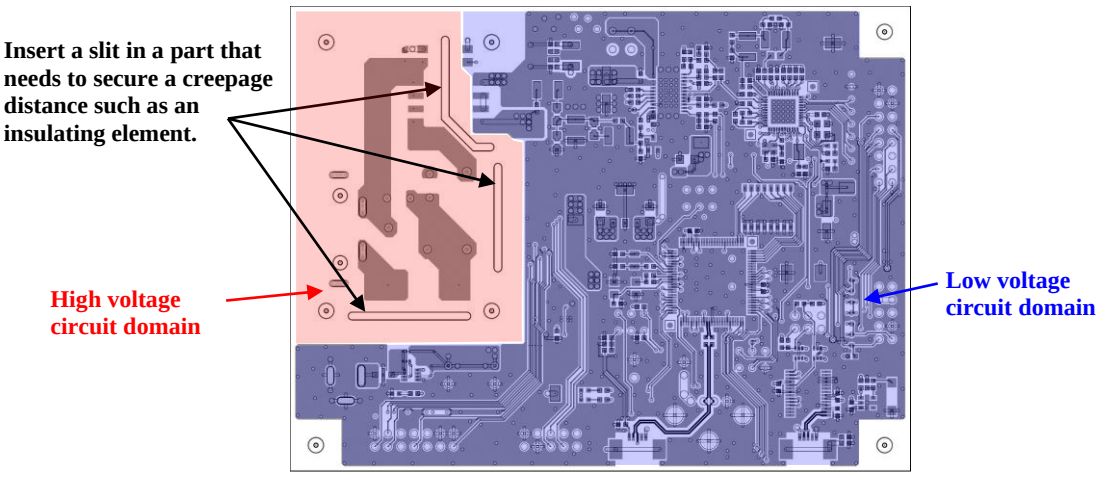


Figure 2-2 Example of PCB pattern separation in high voltage circuit domain and low voltage circuit domain

Creepage distances and clearances

Description	Rated impulse voltage 4 kV (mm)	Rated impulse voltage 6 kV (mm)
Creepage distances		
1. Between live parts of different polarity, including parts for looping-in of external conductors	4[1)]	5,5
2. Between live parts, including parts for looping-in of external conductors, and:		
- accessible metal parts,	5,5	8
- earthed metal parts, including the earthing circuits	3	5,5
- screws or other devices for fixing bases, covers or cover plates	3	5,5
Clearances		
3. Between live parts of different polarity, including parts for looping-in of external conductors	3	5,5
4. Between live parts, including parts for looping-in of external conductors, and		
- accessible metal parts,	5,5	8
- earthed metal parts, including the earthing circuits	3	5,5
- screws or other devices for fixing bases, covers or cover plates	3	5,5
5. Between live parts, including parts for looping-in of external conductors, and the surface on which the base of surface-type equipment is mounted	5,5	8
Distances through insulating sealing compound		
6. Between live parts covered with at least 2 mm of sealing compound and the surface on which the base of surface-type equipment is mounted	4	5,5

1) The value is reduced to 3 mm for nominal voltage up to and including 250 V

Figure 2-3 Examples of Creepage distance and Clearance of EN650065-4-2 (CE marking)

2.2 Cautions on Parts Layout for the Low Voltage Circuit Domain

- Figure 2-4 shows cautions on PCB layout for the low voltage circuit domain.
- The critical sections of the PLC signal path: PLC coupling circuit, AFE (Reception and transmission stages, filters etc.), connections to R9A06G037 and to the HOST MCU should be arranged along the flow of the PLC signal so that the wiring of the PLC signal is as short as possible with minimal intersections.
- In DC-DC power supply circuits, switching noise may affect the transmission and reception signals of the PLC. Therefore, in order to prevent interference, between the DC-DC power supply circuit of the noise source and the circuit parts / signal path of the AFE circuit / R9A06G037, take measures such as increasing the distance and inserting a GND pattern.
- RX-BPF is particularly susceptible to noise, so do not place parts separately, shorten the wiring as much as possible, put them together in one place, and keep them at least 3 cm away from the power supply circuit.
- If the distance cannot be secured more than 3 cm, place the power supply circuit on the back side (separate layer from RX-BPF).
- Avoid or minimize area where the PLC signal wiring and the power supply wiring cross each other.

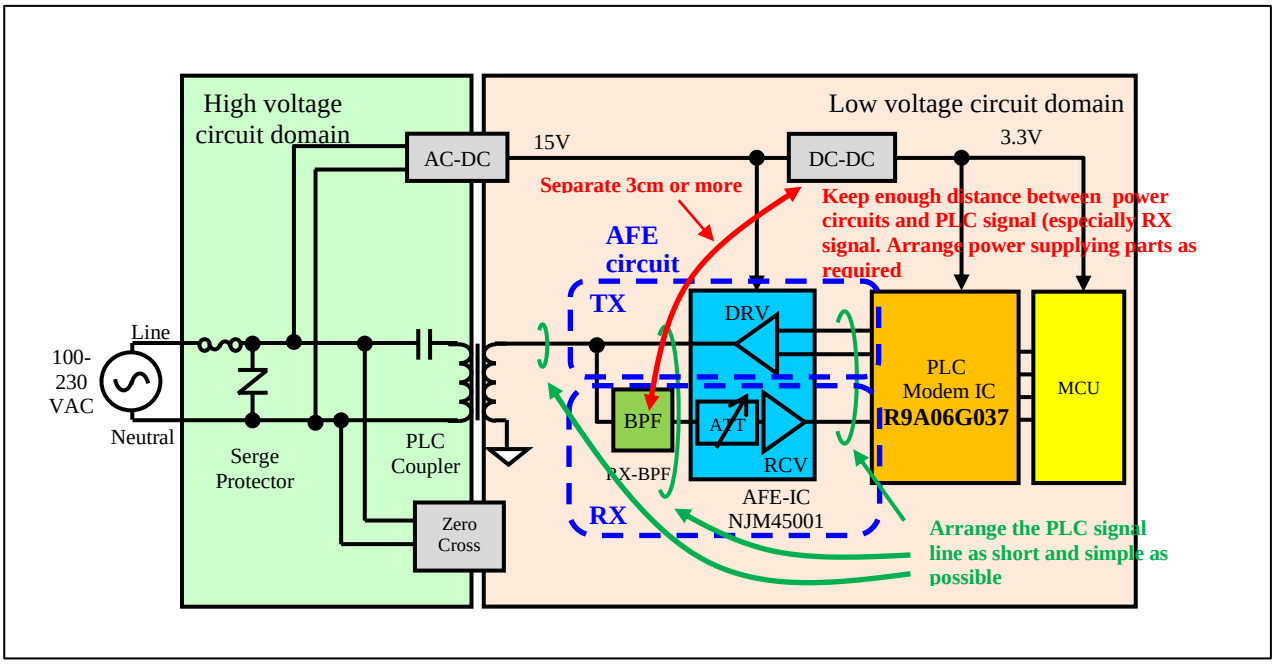


Figure 2-4 Parts Layout for the Low Voltage Circuit Domain

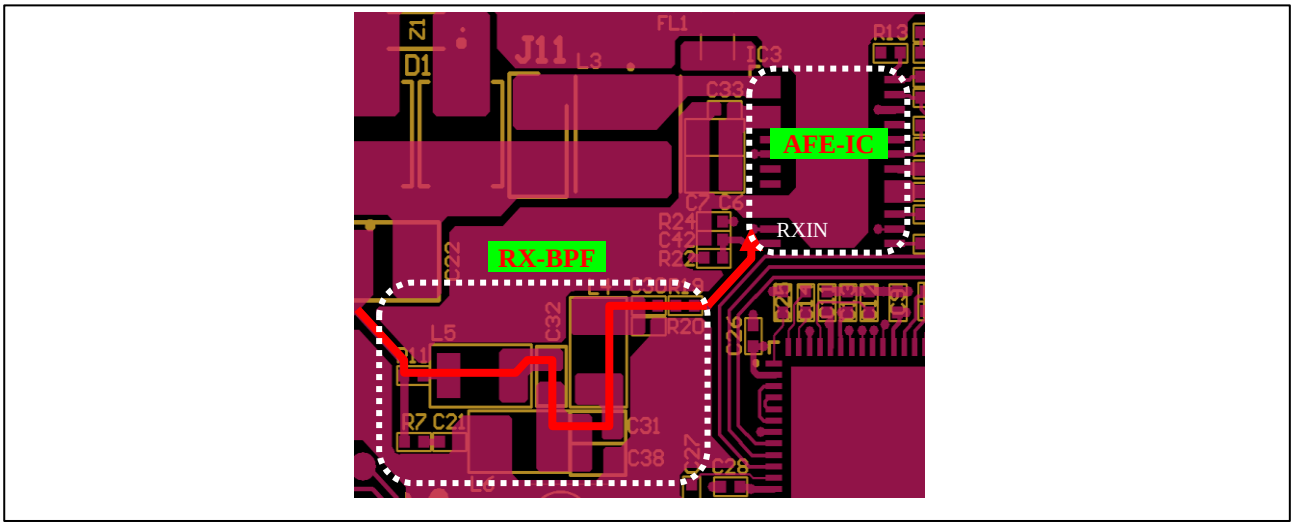


Figure 2-5 RX-BPF layout example

2.3 Cautions on Parts Layout around R9A06G037 and PCB Pattern

- Arrange the R9A06G037 decoupling capacitors and the external parts for DC-DC close to the R9A06G037 terminal and make the wiring as short as possible.
- Arrange the crystal oscillator and peripheral parts connecting to R9A06G037 close to R9A06G037 as much as possible, and make the wiring as short as possible. Also, arrange GND under and around the crystal oscillator, and connect to the GND solid pattern to avoid making an isolated island pattern.

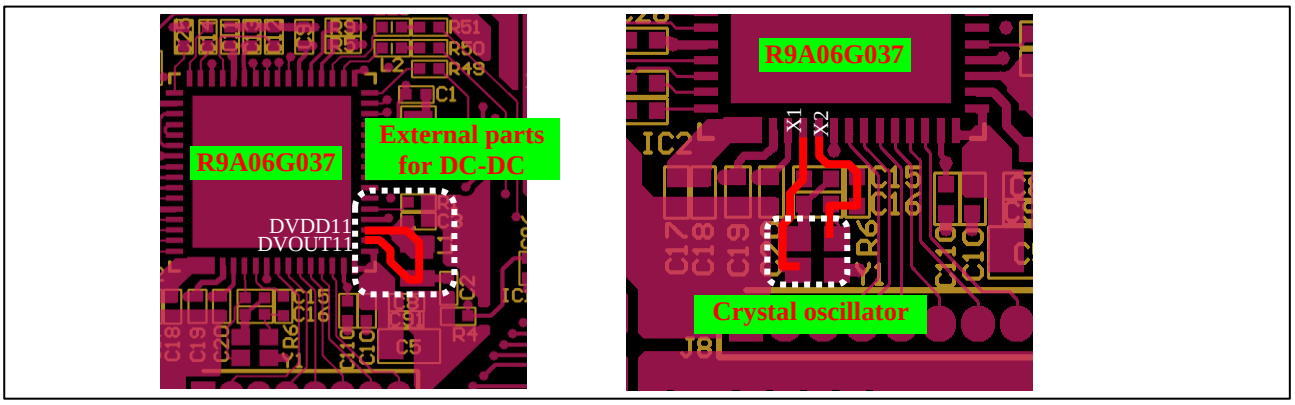


Figure 2-6 Placement of the external parts for R9A06G037 built-in DC-DC and the crystal oscillator

2.4 Cautions on Parts Layout around the AFE Circuit and PCB Pattern

- Arrange the decoupling capacitor of AFE circuit close to the AFE device terminal and make the wiring pattern as short as possible.
- Widen the wiring width for the AFE circuit TX output signal part to support approximately 3A large current flowing into this area. (3mm or more is recommended.)
- Make the wiring length as equal as possible when using a differential signal.
- The TX / RX signal line between R9A06G037 and AFE-IC should be the shortest possible and balanced wiring. (Figure 2-8 shows an example of routing the TX / RX signal lines)
- Since the 15V power supply wiring generates much noise, avoid the TX signal and the RX signal crossing each other as much as possible. Also it is recommended to use the GND pattern in the area where the TX/RX signals or TX/RX parts overlap as much as possible for the power supply layer (3rd Layer).
- Especially be careful with RX-BPF which is highly affected by noise. It is recommended to make the wiring as short as possible, avoid crossing the RX-BPF signal paths and arrange all the parts in one place, and separate RX-BPF from the power supply circuit for 3cm or more. When it is not possible to keep 3cm or more distance in-between, consider arranging the power supply circuit on a layer different from the RX-BPF) .

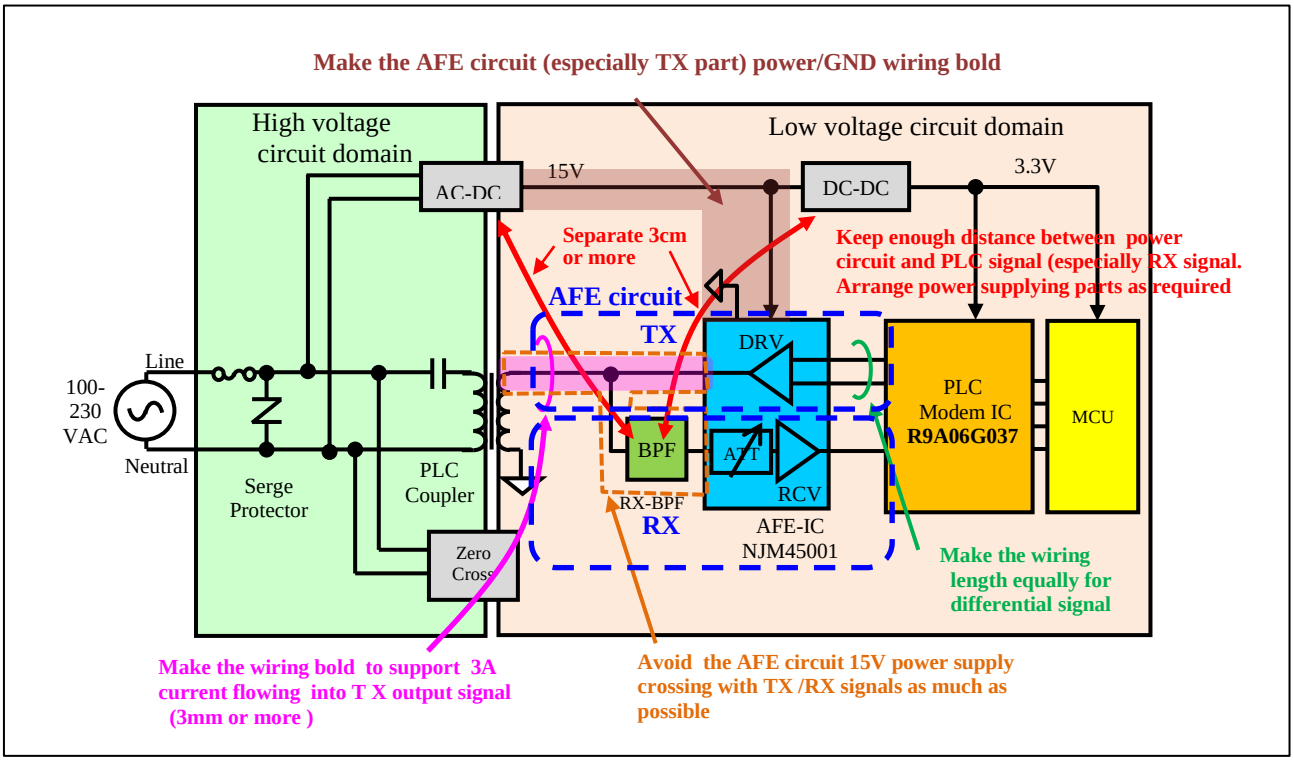
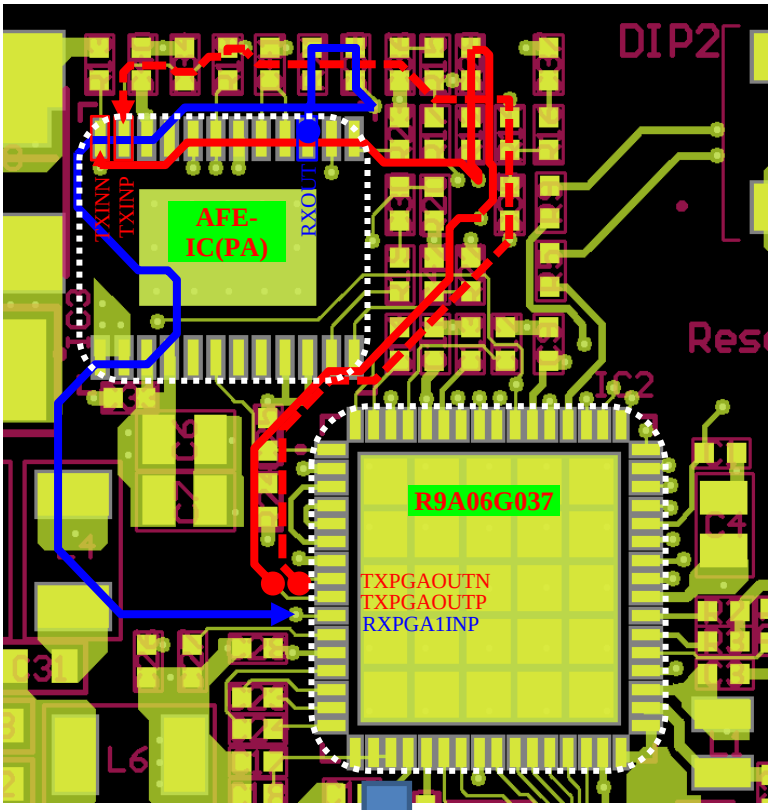


Figure 2-7 Cautions on Power Supply Wiring for AFE Circuit Signal

The following Figure 2-8 is shown as an example of connecting the TX / RX signal lines.
In the figure (a), the TX / RX signal paths are routed relatively long, there are intersections between the TX / RX signals, and the length of the differential TX signal path is unbalanced.
In the figure (b), the TX / RX signal paths have the minimum required length, there is no intersection between the TX / RX signals, and the differential TX signal path has a balanced length.

(a) Signal line before improvement

· Between R9A06G037 and AFE-IC (PA)
-TX signal
TXPGAOUTN → TXINN
TXPGAOUTP → TXINP
-RX signal
RXOUT → RXPGAINP
The wiring of these wires is long, and TX signal is not balanced.



(b) Signal line after improvement

· Between R9A06G037 and AFE-IC (PA)
-TX signal
TXPGAOUTN → TXINN
TXPGAOUTP → TXINP
-RX signal
RXOUT → RXPGAINP
The wiring of these wires is short, and TX signal is well-balanced.

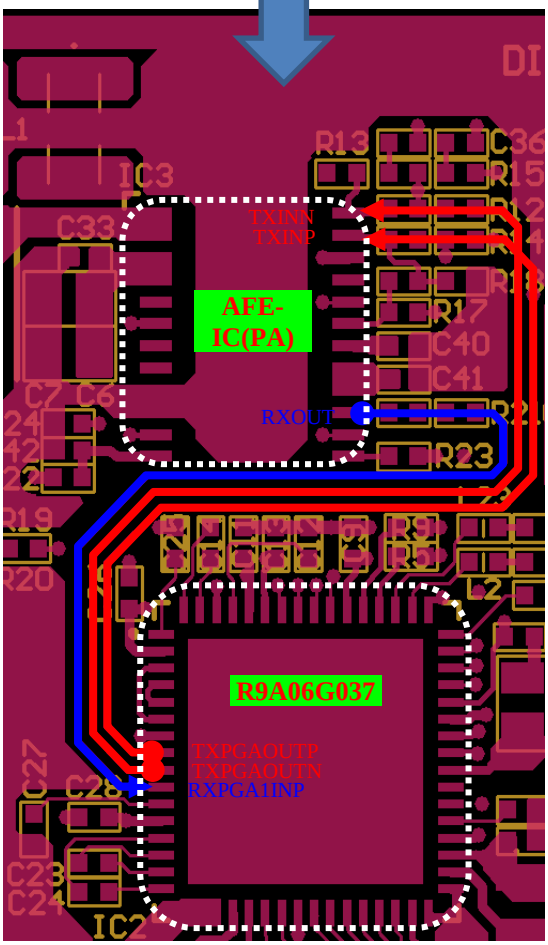


Figure 2-8 Example of routing the TX / RX signal line between R9A06G037 and AFE-IC

2.5 Cautions on the DC-DC Power Supply Circuit

This chapter explains cautions when implementing the DC-DC power supply circuit into the PLC board.

- It is necessary to generate 3.3V to use R9A06G037 and 15V or 12V to use NJM45001 on the PLC board.
- In DC-DC power supply circuits, switching noise may affect the transmission and reception signals of the PLC. Therefore, in order to prevent interference, between the DC-DC power supply circuit of the noise source and the circuit parts / signal path of the AFE circuit / R9A06G037, take measures such as increasing the distance and inserting a GND pattern.
- Since RX-BPF is particularly susceptible to noise, keep it at least 3 cm away from the DC-DC power supply circuit.
- If the distance cannot be secured more than 3 cm, place the DC-DC power supply circuit on a different layer from the RX-BPF.

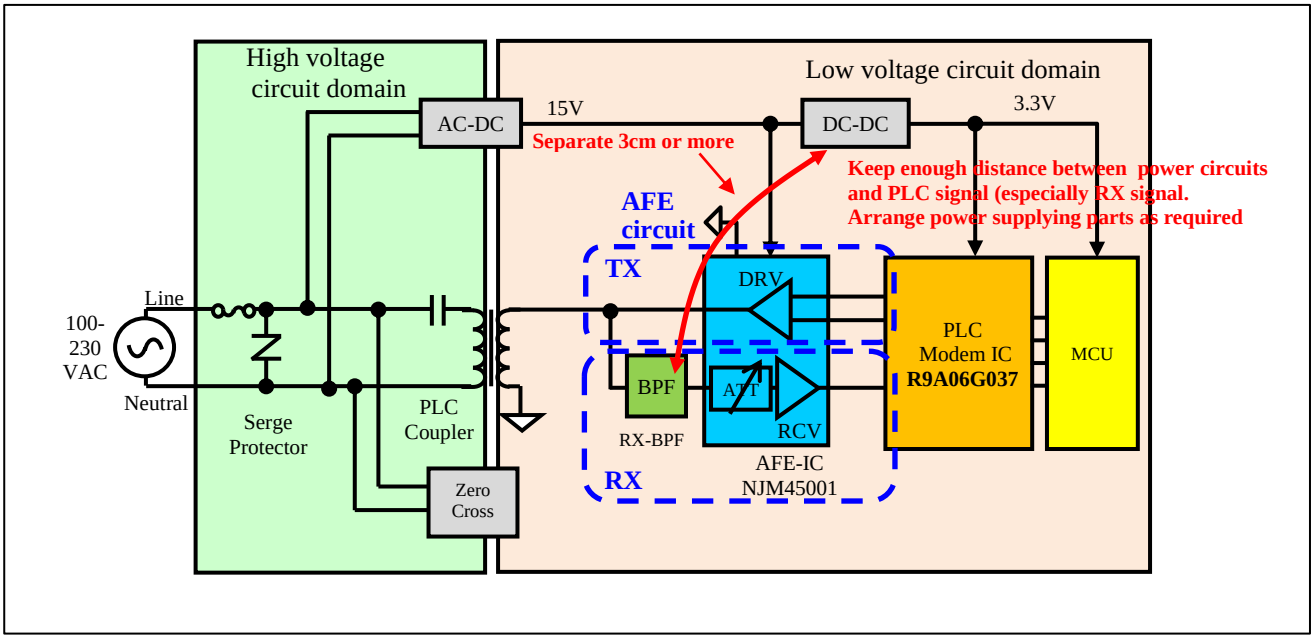


Figure 2-9 Cautions on DC-DC Power Source Circuit Implementation

2.6 Cautions on the AC-DC Power Supply Circuit

This chapter explains cautions when implementing the AC-DC power supply circuit to the PLC board. Follow the cautions below when designing the AC-DC power supply circuit, as the switching noise may interrupt the EMC standards and PLC transmission/reception characteristics.

- Separate the AC-DC circuit GND from GND for other circuits.
- The creepage/space distance between the AC-DC circuit and other circuits depends on the local safety standards. Follow the safety standards of the target region. (An example is shown in Figure 2-3.)
- It is recommended to separate the PLC coupler and the AC-DC power supply circuit for 4 cm or more as it may affect the EMC standards.

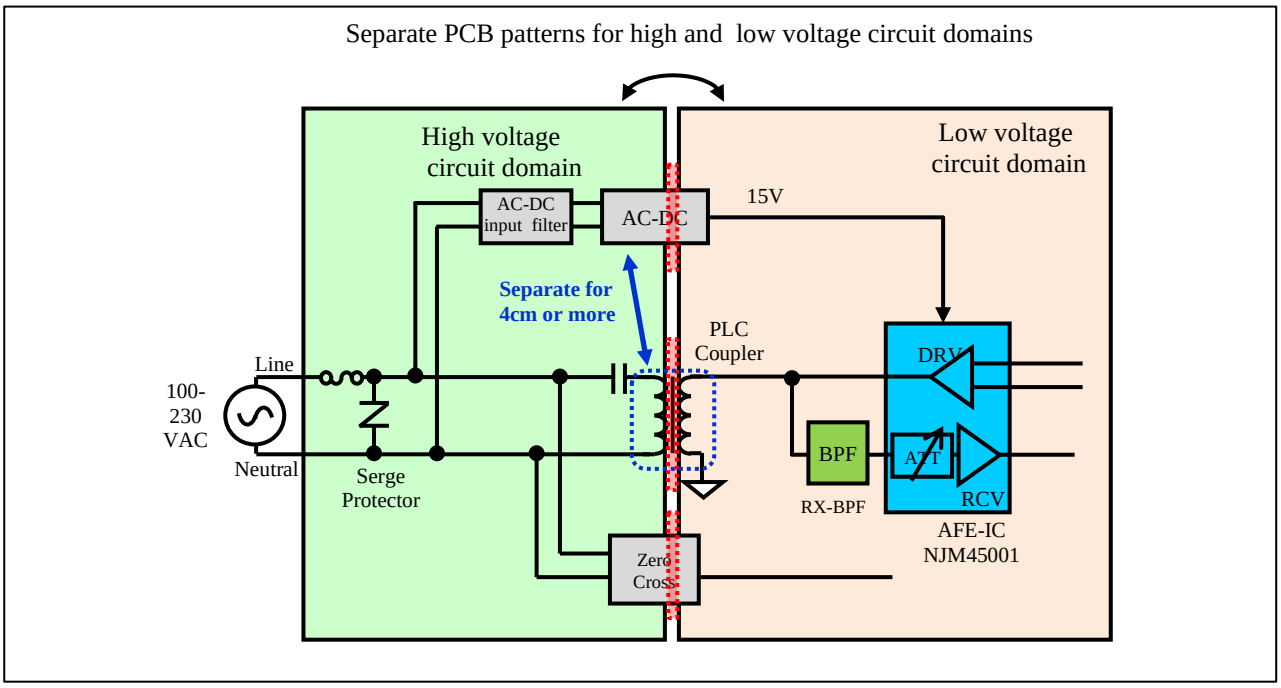


Figure 2-10 Cautions on AC-DC Power Source Circuit Implementation

2.7 Cautions on GND Patterns

2.7.1 Cautions regarding GND reinforcement and heat dissipation design

- For PLC board design, it is recommended to use a PCB substrate with 4 or more layers.
  - The 1st layer is used as the signal layers, fill the unused area with GND patterns for heat dissipation, and signal separation.
  - For the 2nd layer, it is important to use the GND layer for signal separation, noise shielding and heat dissipation.
  - The 3rd layer is used as the power supply layer. In addition arrange the GND pattern partially for noise shielding and heat dissipation.
  - The 4th layer is used as the signal layer and fill the unused area with GND patterns for heat dissipation, and signal separation.
- There is the exposed die pad (internally connected to GND) on the back side of R9A06G037 and AFE-IC for heat dissipation. Place GND pattern to connect the exposed die pad on 1st layer, 2nd layer, 3rd layer and 4th layer, and connect the GND pattern of each layer with via holes. Place via holes as much as possible on GND pattern (recommendation: hole diameter: 0.3mm, R9A06G037: more than 12 pcs, AFE-IC: more than 9pcs).
- In the 1st layer, connect the Exposed die pad of AFE-IC to the GND plane of the first layer as much as possible to improve heat dissipation. (An example is shown in Figure 2-12 (a)-(b))
- In the GND layer of the 2nd layer, connect the path to the GND supply terminal on the PCB smoothly with the Exposed die pad of R9A06G037 and AFE-IC. (An example is shown in Figure 2-12 (c)-(d))
- In the power supply layer of the 3rd layer, place a GND pattern in the via hole part connected to the Exposed die pad of R9A06G037 and AFE-IC. (An example is shown in Figure 2-12 (e)-(f))
- In the 4th layer, the GND pattern is especially important for heat dissipation design. In order to further improve heat dissipation performance, widen the area of the GND pattern and connect the Exposed die pad of R9A06G037, AFE-IC to the GND pattern. Then, connect as smoothly as possible so that there are no obstacles in the path to the Exposed die pad of the AFE-IC and the GND supply terminal on the PCB. (An example is shown in Figure 2-12 (g)-(h)) (Reason: Since large current flows in AFE-IC (Power amplifier for transmission) when transmitting at low load, heat dissipation will deteriorate if the connection between the Exposed die pad of AFE-IC and the GND pattern is not appropriate. Then, the thermal shutdown function of the AFE-IC may intermittently stop the output of the signal.)
- When checking PCB artwork, in the paste mask (paste data) used for component mounting, it is recommended to check if the appropriate pattern is placed on the exposed die pad part of R9A06G037 and AFE-IC. (See Figure 2-13 for details)
- Fill the unused area of 1st and 4th layer as the signal layer with GND patterns. However, if the GND pattern becomes a small island or fine antenna-shape, it is not necessary to fill it.

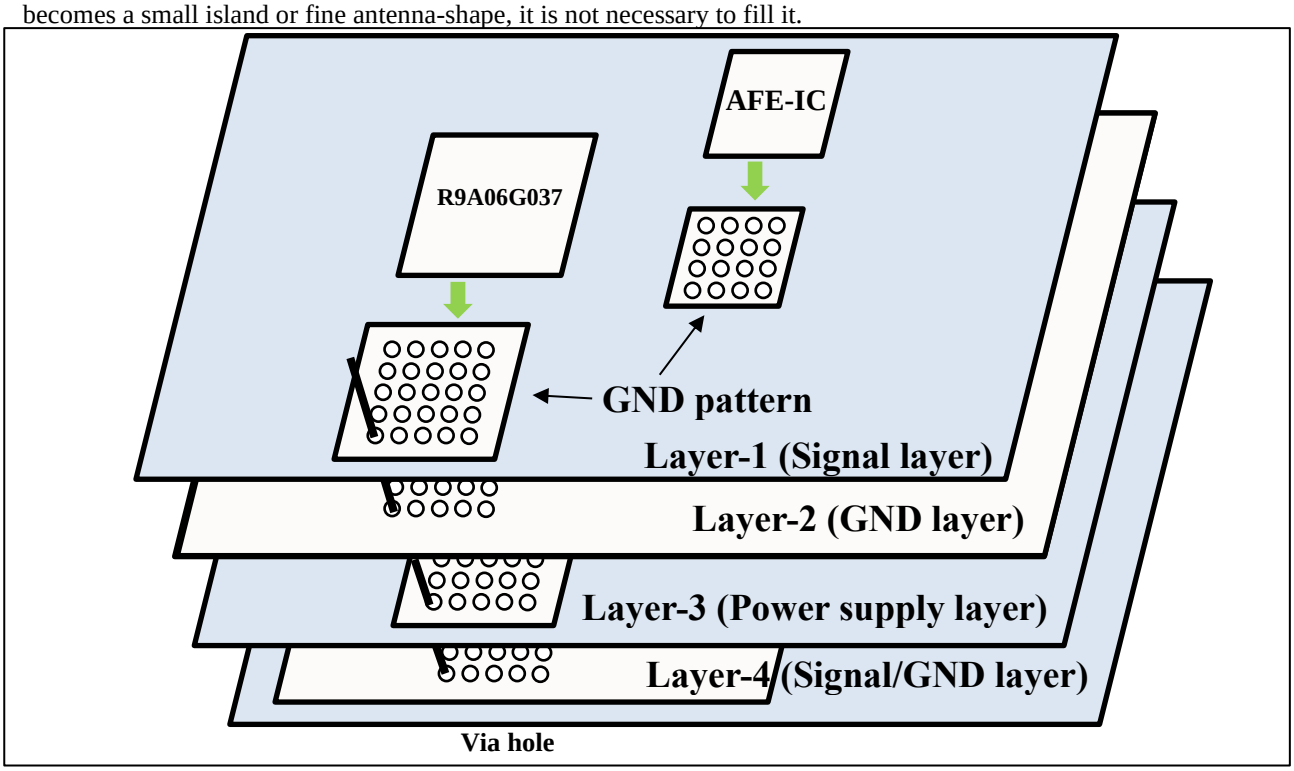
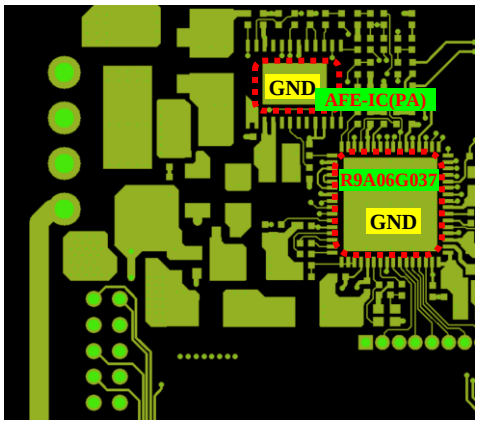
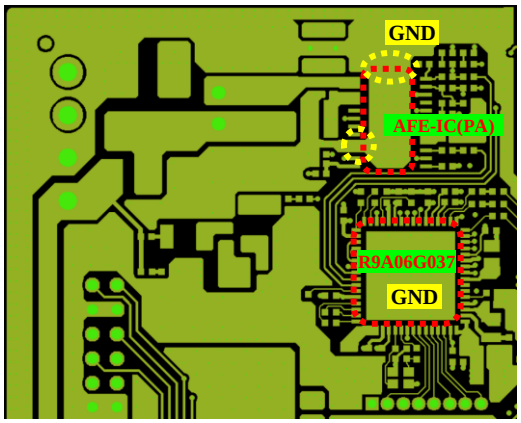


Figure 2-11 Example of PCB Substrate Configuration and GND pattern for the PLC Board



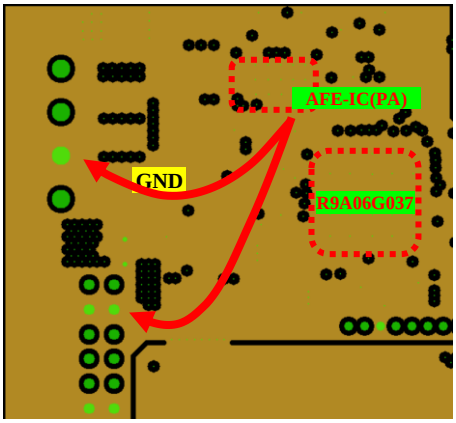
(a) 1st layer pattern before improvement

- The GND pattern is not filled in the empty part of the 1st layer.
- The Exposed die pad of the AFE-IC for which heat dissipation characteristics should be considered is not connected to the GND plane of the 1st layer.



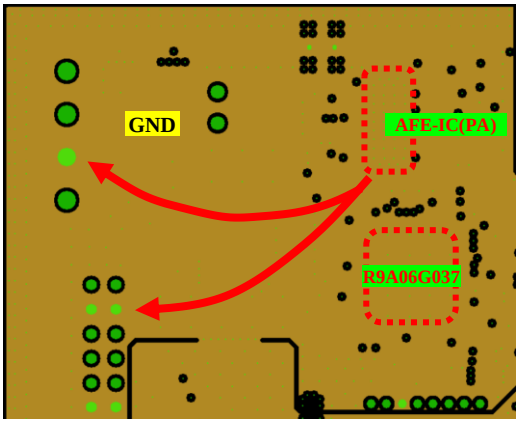
(b) 1st layer pattern after improvement

- The GND pattern is filled in the empty part of the 1st layer.
- The Exposed die pad of the AFE-IC for which heat dissipation characteristics should be considered is connected to the GND plane of the 1st layer. (Yellow circle part)



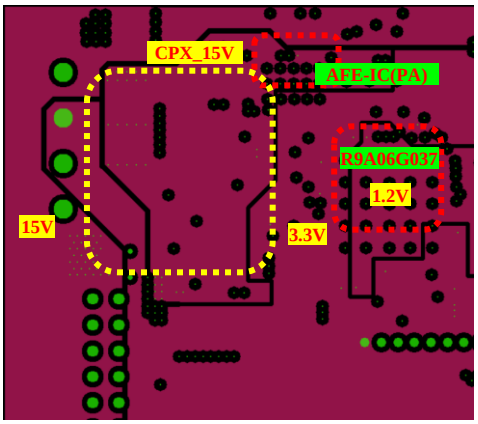
(c) 2nd layer pattern before improvement

- It is not smoothly connected because there is a Via hole in the path from the Exposed die pad of AFE-IC to the GND supply terminal on the PCB where the heat dissipation characteristics should be considered.



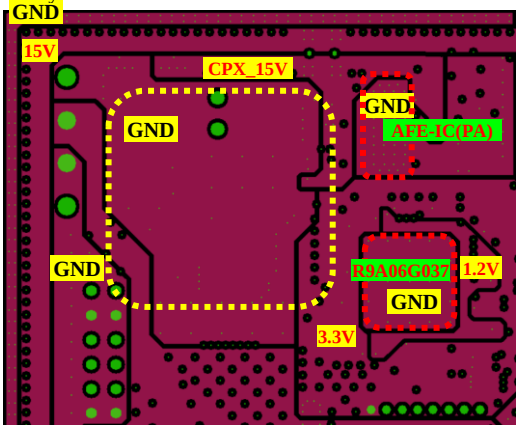
(d) 2nd layer pattern after improvement

- The GND pattern of the path from the Exposed die pad of the AFE-IC to the GND supply terminal on the PCB that should be considered for heat dissipation characteristics is smoothly connected.



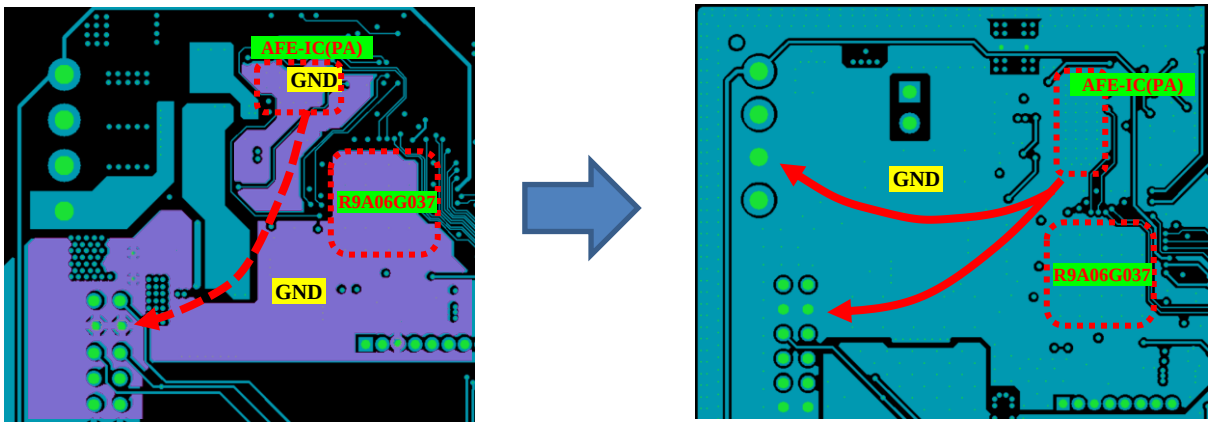
(e) 3rd layer pattern before improvement

- No GND pattern is placed on the 3rd layer
- The PLC TX signal output / RX signal input wiring area intersects the noisy CPX_15V pattern. (Yellow circle part)



(f) 3rd layer pattern after improvement

- The GND pattern is embedded in the part connected to the exposed die pad on the back of R9A06G037 and AFE-IC on the 3rd layer.
- The GND pattern is placed at the intersection of the PLC TX signal output / RX signal input wiring area and the noisy CPX_15V pattern. (Yellow circle part)



(g) 4th layer pattern before improvement

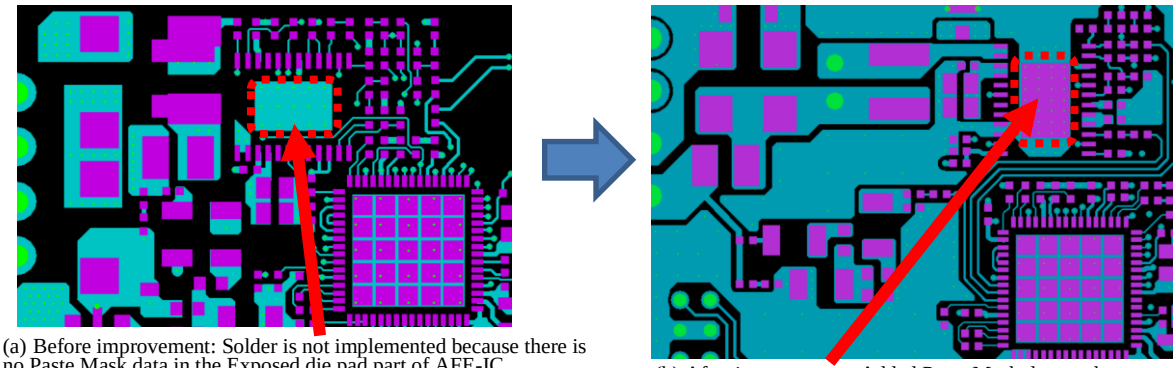
- The GND pattern is not filled in the empty part of the 4th layer
- The GND pattern of the path that should consider the heat dissipation characteristics from the Exposed die pad of the AFE-IC to the GND supply terminal on the PCB is divided.

(h) 4th layer pattern after improvement

- The GND pattern is filled in the empty part of the 4th layer
- The GND pattern of the path that should consider the heat dissipation characteristics from the Exposed die pad of the AFE-IC to the GND supply terminal on the PCB is not divided and is connected smoothly.

Figure 2-12 Example of connection between Exposed die pad of R9A06G037 and AFE-IC and GND pattern

Cyan: 1st layer / Magenta: Top Paste Mask / Yellow green: via hole



(a) Before improvement: Solder is not implemented because there is no Paste Mask data in the Exposed die pad part of AFE-IC.

(b) After improvement: Added Paste Mask data to the Exposed die pad part of AFE-IC.

- When checking the PCB artwork, it is recommended to check if the appropriate pattern is placed on the Exposed die pad part of R9A06G037 and AFE-IC in the paste mask (paste data) used for component mounting.
- If the paste mask does not have a pattern to connect to the Exposed die pad of R9A06G037 and AFE-IC, the operation will be unstable because R9A06G037 and AFE-IC will not be connected to GND. In addition, heat dissipation of the AFE-IC deteriorates, and the signal output stops intermittently due to the thermal shutdown function of the AFE-IC (Power Amp).
- Mask to check: Paste mask extension GTP, GBP, etc. (The mask used for assembling parts))
  - GTP : Top Paste Mask
  - GBP : Bottom Paste Mask
- The Gerber file provided by the board vendor may not contain the paste mask data. In that case, request the paste mask data from the board vendor.

- There is a solder mask as mask data for PCB that can be easily mistaken for a paste mask (sometimes called resist data, etc.). Solder masks are used only when manufacturing boards, and paste masks are used when assembling parts.
- Solder mask extension GBS, GBS, etc. (mask used when manufacturing the board)
  - GTS: Top Solder Mask
  - GBS: Bottom Solder Mask

Figure 2-13 Example of checking the paste mask (paste data) used for component mounting

2.7.2 Cautions on other GND Pattern

- When using the AC-DC power supply circuit, separate GND for the AC-DC power supply circuit and GND for low voltage circuit domain.
- For the low voltage circuit domain GND, it is recommended to use the GND solid pattern instead of separating GND for the digital circuit and GND for the analog circuit.
- Do not place a GND pattern under the inductance as shown in Figure 2-14 to avoid noise influences on the GND pattern. (e.g. the inductor to use for RX-BPF, a power supply circuit, and a filter for power supply line, etc.)

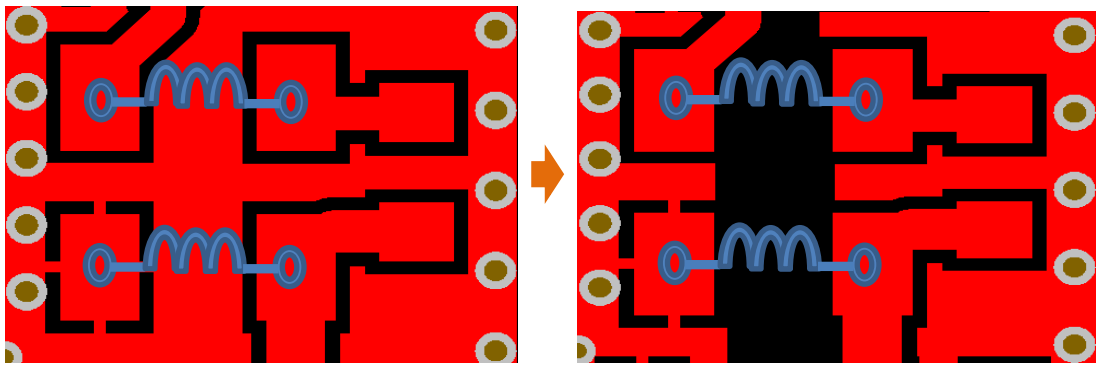


Figure 2-14 Cautions on GND patterns under the inductor

2.8 Cautions on the Power Supply Pattern

- It is recommended to configure the power supply layer with the PCB substrate configuration of the PLC board as shown in Figure 2-11.
- It is recommended to arrange 1.1V/3.3V/15V power regions used in the PLC board for the power supply layer, and arrange the GND pattern in the area where crossing with the power region should be avoided. Figure 2-12 (e)(f) and Figure 3-4 show examples of the power supply layer.

3. PCB Layout Design Example

This chapter shows PCB layout examples for the PLC board explained in Chapter 2. This material shows the PCB layout for the PLC board based on the configuration in Figure 3-1 as Renesas Electronics does not offer PLC boards with the AC-DC power supply circuit.

Figure 3-2 shows a parts layout example, Figure 3-3 shows a wiring example, and Figure 3-4 shows a power supply layer example. Note that these examples are not necessarily the most suitable PCB layout for all the PLC board patterns.

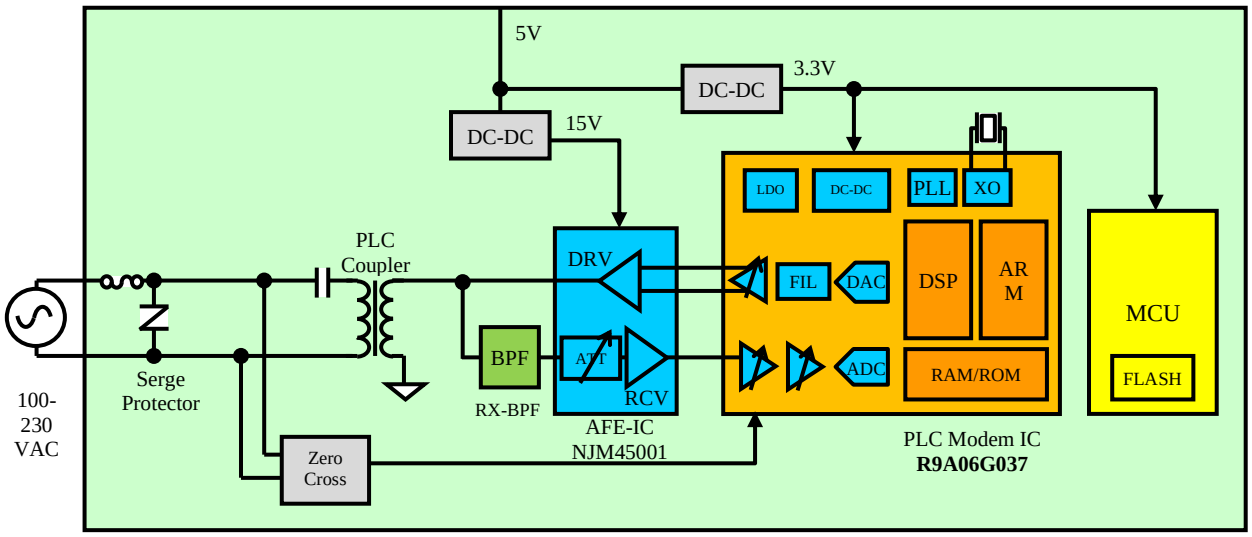


Figure 3-1 PLC Board Configuration Based on the PCB Layout Example in Chapter 3

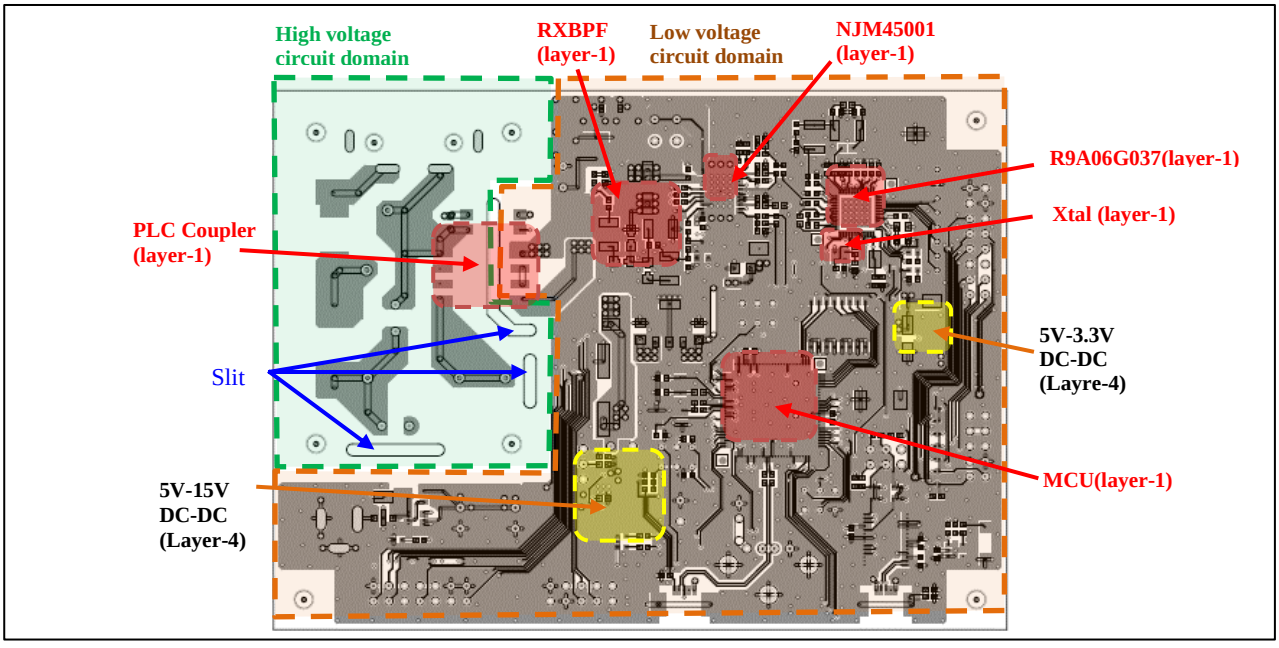


Figure 3-2 Example of PLC Board Parts Layout in Figure 3-1

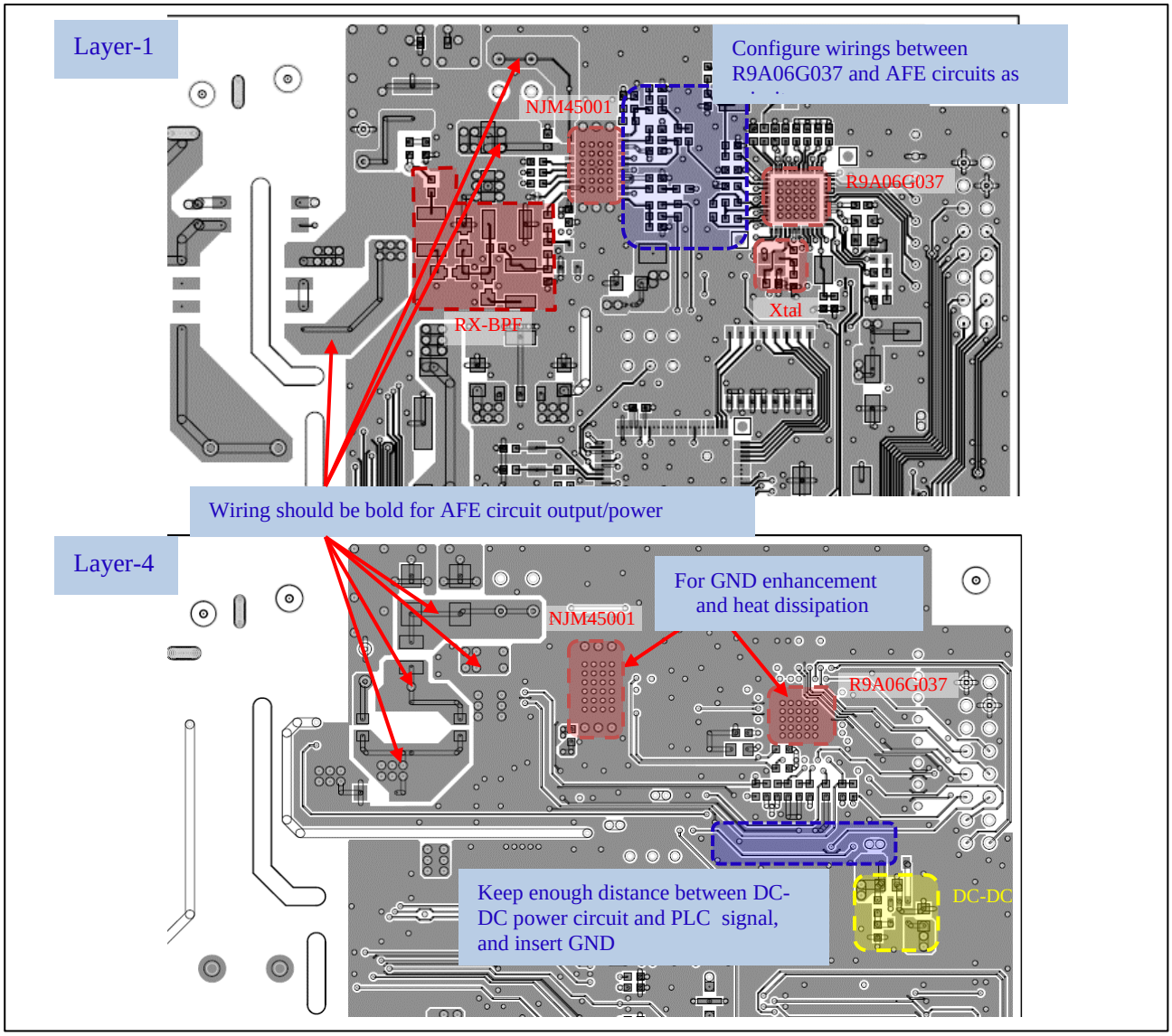


Figure 3-3 Example of PCB Layout Design for PLC Board in Figure 3-1

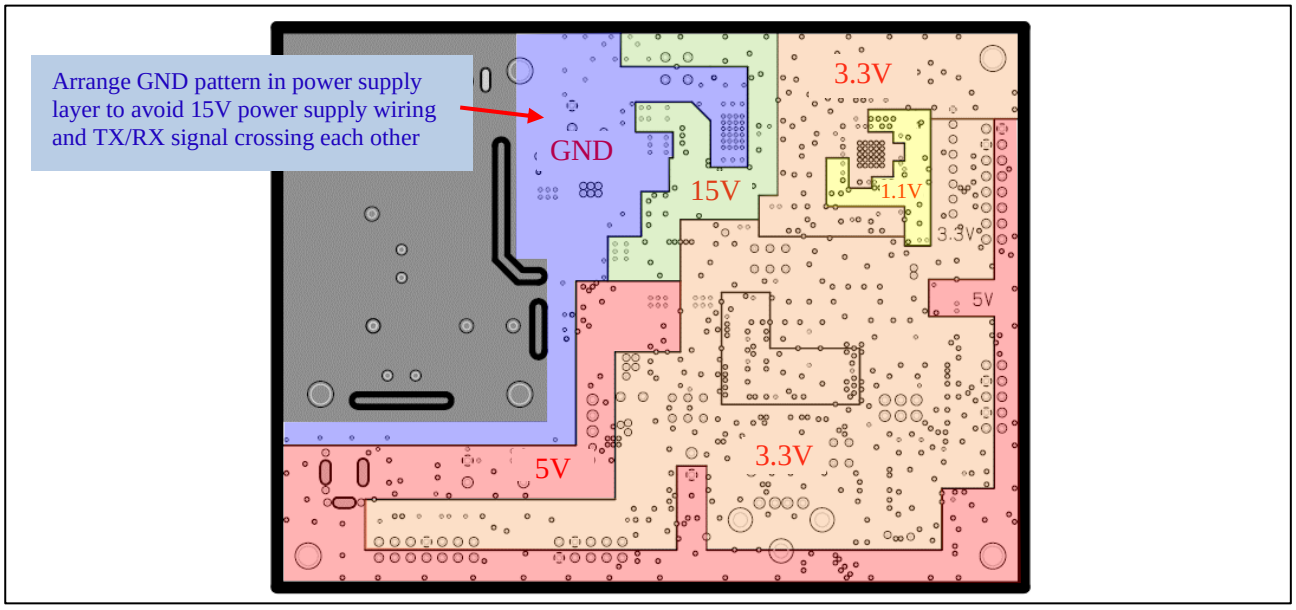


Figure 3-4 Example of Power Supply Layer in Figure 3-1

Website and Support

Renesas Electronics Website
https://www.renesas.com/jp/en

Inquiries
https://www.renesas.com/jp/en/contact-us

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2018.12.1		First Edition issued
2.00	2022.02.04	3~15	Added reference example Added and modified description
3.00	2022.07.01		Changed the title
4.00	2022.08.01	9,10	Deleted the description related to circuit design (RX-BPF, DC-DC/AC-DC Power Supply Circuit)

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