placehold of spliting the input caps before and after RS1
reduce the chatter for reverse mode

All NFETs and PFETs are 3x3 size

Split the output caps before and after RS2, to reduce the chatter for forward mode

Minimum effective capacitance guidline for DCIN, VDD, VDDP, BOOT1 and BOOT2 pins:

BOOT1 and BOOT2 capacitance: At least 0.25uF at 5V and x50 high side FET effective gate capacitance

VDD and VDDP capacitance: At least 0.4uF at 5V and x1.6 effective gate capacitance at boot pin

DCIN capacitance: At least 0.4uF at 20V

For C30, use MLCC with at least 0.25uF effective capacitance at 5V

For C31, use MLCC with at least 0.4uF effective capacitance at 20V

For C32, C33, use MLCC with at least 0.4uF effective capacitance at 5V

DNP Q3 for 2 FETs configuration

Short to GND for 2FETs
DNP R109 for 2FETs

For C36, use MLCC with at least 0.25uF effective capacitance at 5V

Short to VDDP for 2FETs
DNP R11 and C36 for 2FETs

CSOP1
A
Short for 2FETs
Open for 4FETs

Refer to PROG table in DS

SDA, SCL, FRWPG, RVSPG, FRWEN, RVSEN all have 3V3 or VDD pull up options

Title	RTKA489800DE00000BU_REVA		
Size C	Document Number <Doc>		Rev
Date: Wednesday, July 10, 2019	Sheet 1 of 1		