To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8/300H Tiny Series

24-Bit Timer Generation Using Timers V and W

Introduction

Applies the functions of timer V and timer W to implement a 24-bit timer.

Target Device

H8/3664

Contents

1. Specifications

1. This sample task generates pulses by alternately setting an output high for one second and then low for one second (figure 1.1).
2. The clock source of timer W is provided by connecting the compare-match output pin of timer V to the clock input pin of timer W.
3. A 24-bit timer is implemented through combined use of the 8-bit counter of timer V and the 16-bit counter of timer W.

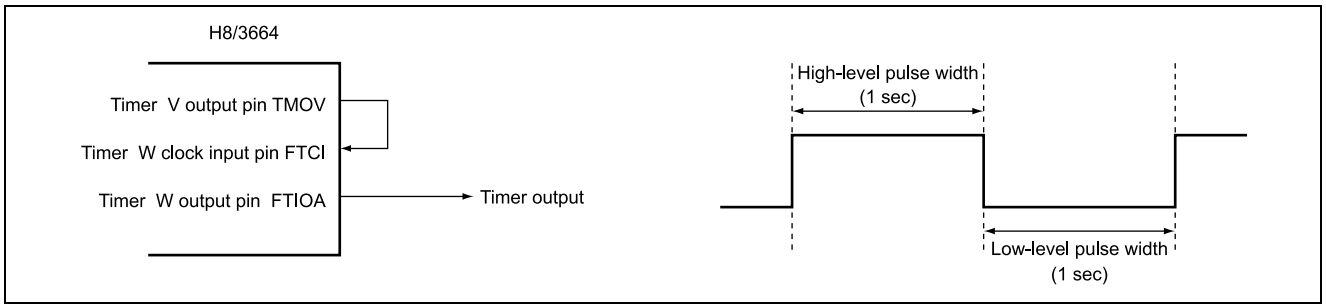


Figure 1.1 24-Bit Timer Using the Functions of Timers V and W

2. Description of Functions

1. In this sample task, the 8-bit timer V and 16-bit timer W are used together to form a 24-bit timer. Figure 2.1 is a block diagram of the timers used in this sample application. The following is a description of the items in the diagram.

- Timer counter V (TCNTV) is an 8-bit up-counter. The input clock signal is selectable from among nine sources, namely the system clock frequency-divided by 4, 8, 16, 32, 64 or 128, and clock signals generated from the rising edge, falling edge, or both edges of an external clock.
- Timer control register V0 (TCRV0) is an 8-bit readable/writable register which selects the TCNTV input clock and the condition for clearing of TCNTV, and enables or disables timer V compare-match interrupt requests.
- The timer control/status register V (TCSRV) is an 8-bit readable/writable register which has status flags that indicate the state of compare-match functions A and B and timer overflow, and controls output for the compare-match functions.
- The timer control register V1 (TCRV1) is an 8-bit readable/writable register that selects the driving edge on the TRGV pin, enables TRGV input, and selects the input clock for TCNT.
- Time constant register A (TCORA) is an 8-bit readable/writable register which holds the value (compare–match value) that is constantly compared with the value of the timer counter, TCNTV. When the values match, the CMFA bit of TCSRV is set to 1. If this happens while CMIEA in TCRV0 is 1, an interrupt request is sent to the CPU.
- TCORA of timer V is used as an output-compare register.
- A 125-kHz (= 8-µs period) clock source drives timer V, i.e., the selected signal is ϕ (= 16 MHz)/128.
- Upon a compare-match of timer V, timer V toggles the output on the TMOV pin and the timer counter TCNTV is cleared.
- The timer-output pin of timer V, TMOV, is connected to pin FCTI, the clock input for timer W.
- The toggled output on timer V's output pin is thus the clock source for timer W.
- GRA of timer W is used as an output-compare register.
- Timer W's timer counter (TCNT) is incremented on each rising edge of the signal on the timer input pin, FCTI; when the value in GRA matches TCNT, an interrupt signal is generated and an interrupt request is sent to the CPU if this is enabled.
- Timer counter TCNTV is a 16-bit up-counter which is incremented on either an internal or external clock input. Any of the following four signals is selectable as the input-clock signal for TCNT: signals obtained by dividing the system clock by 2, 4 or 8, and an external clock signal. In this sample task, an external clock signal is selected.

- Timer control register W (TCRW) is an 8-bit readable/writable register which is used to select the input clock signal for TCNT.
- Timer status register W (TSRW) is an 8-bit register used to set conditions for the clearing of the timer W counter, and control the timer W interrupt-request signals.
- The timer interrupt enable register W (TIERW) is an 8-bit readable/writable register which controls enabling/disabling of the individual interrupt requests.
- Counting by TCNT is started by the timer mode register W (TMRW).
- The timer I/O control register 0 (TIOR0) is an 8-bit readable/writable register used to select the output-compare register and output-comparison output.
- General register A (GRA) is a 16-bit readable/writable register. The value in GRA is constantly compared with TCNT; when the values match, IMFA in TSRW is set to 1
- (If IMIEA in TIERW is 1, an interrupt request is then sent to the CPU; however, this interrupt is not used in this sample task).

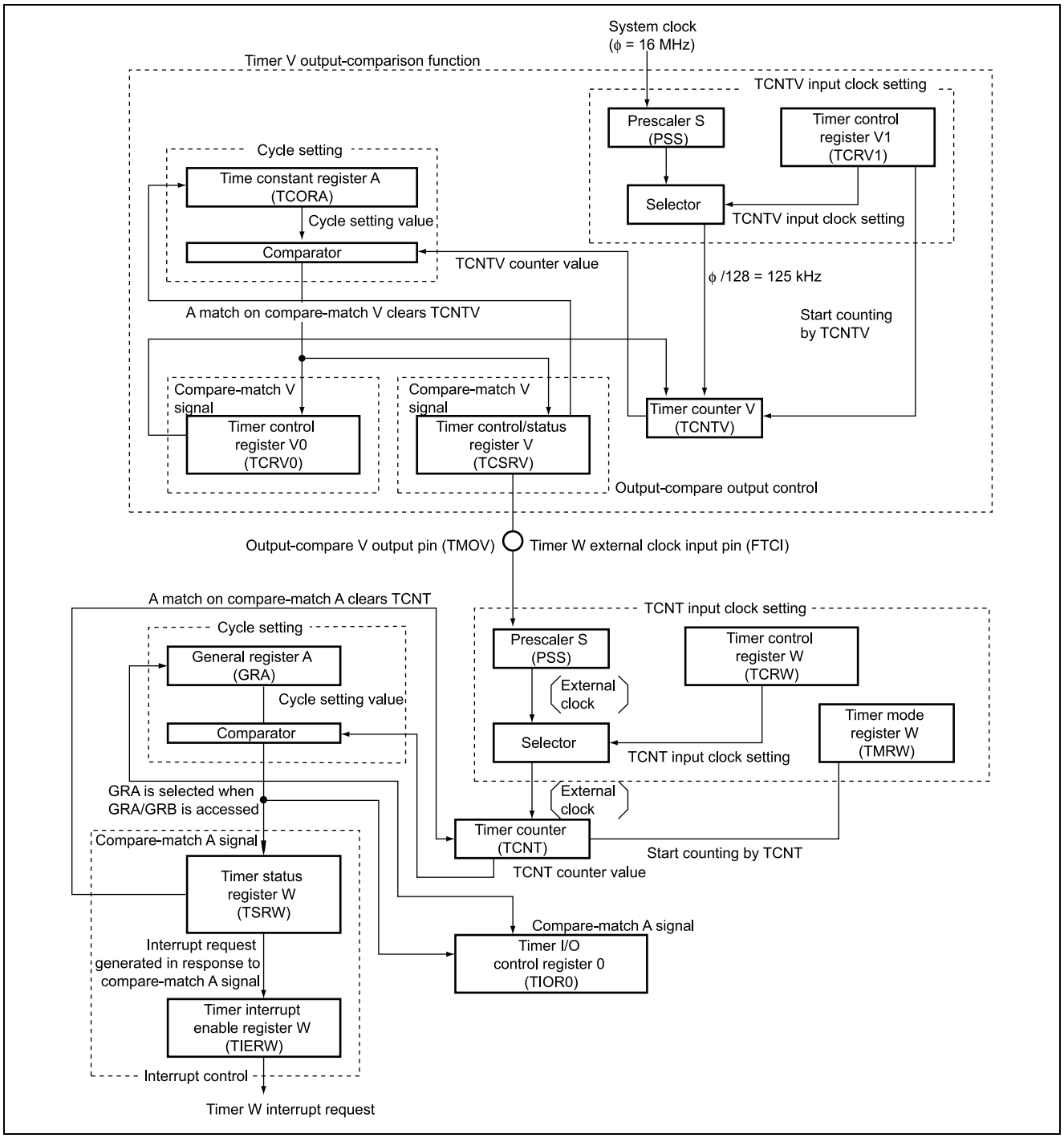


Figure 2.1 The Output-Comparison Functions of Timers V and W

2. Table 2.1 lists the function assignments of this sample task. A 24-bit timer function is implemented through the combination of timers V and W as shown in table 2.1.

Table 2.1 Function Assignment

Function	Function Assignment
TCRV0	Controls generation of interrupt-request signals by compare-match function A, enables clearing of TCNTV when the result of compare-match A is a match, and selects the TCNTV input clock and conditions for counting.
TCRV	Controls the generation of interrupt-request signals by compare-match A.
TCORA	The compare-match register for the lower-order 8 bits of the 24-bit timer counter
TCNTV	An 8-bit up-counter driven by the system clock frequency-divided by 8; provides the 8 lower-order bits of the 24-bit timer counter.
TCRV1	Selects the TCNTV input clock; starts counting by TCNTV.
TMRW	Starts counting by TCNT.
TCRW	Selects the input clock, counter-clearing condition, and timer output level for TCNT.
TIERW	Enables interrupt generation by compare-match A.
TSRW	Controls interrupt-request signal generation by compare-match function A and enables clearing of TCNT upon compare-match A.
TIOR0	Sets up the output-comparison function, i.e. specifies the output-compare register and selects output-comparison output
TCNT	A 16-bit up-counter set up to take the rising edge of an external input as its input clock; provides the higher-order 16 bits of the 24-bit timer counter
GRA	The compare-match register for the higher-order 16 bits of the 24-bit timer counter

3. Operation

The operation of this sample task is described in figure 3.1. A 24-bit timer is implemented by using timer W to count overflows of timer V's TCNTV through the hardware and software processing shown in figure 3.1.

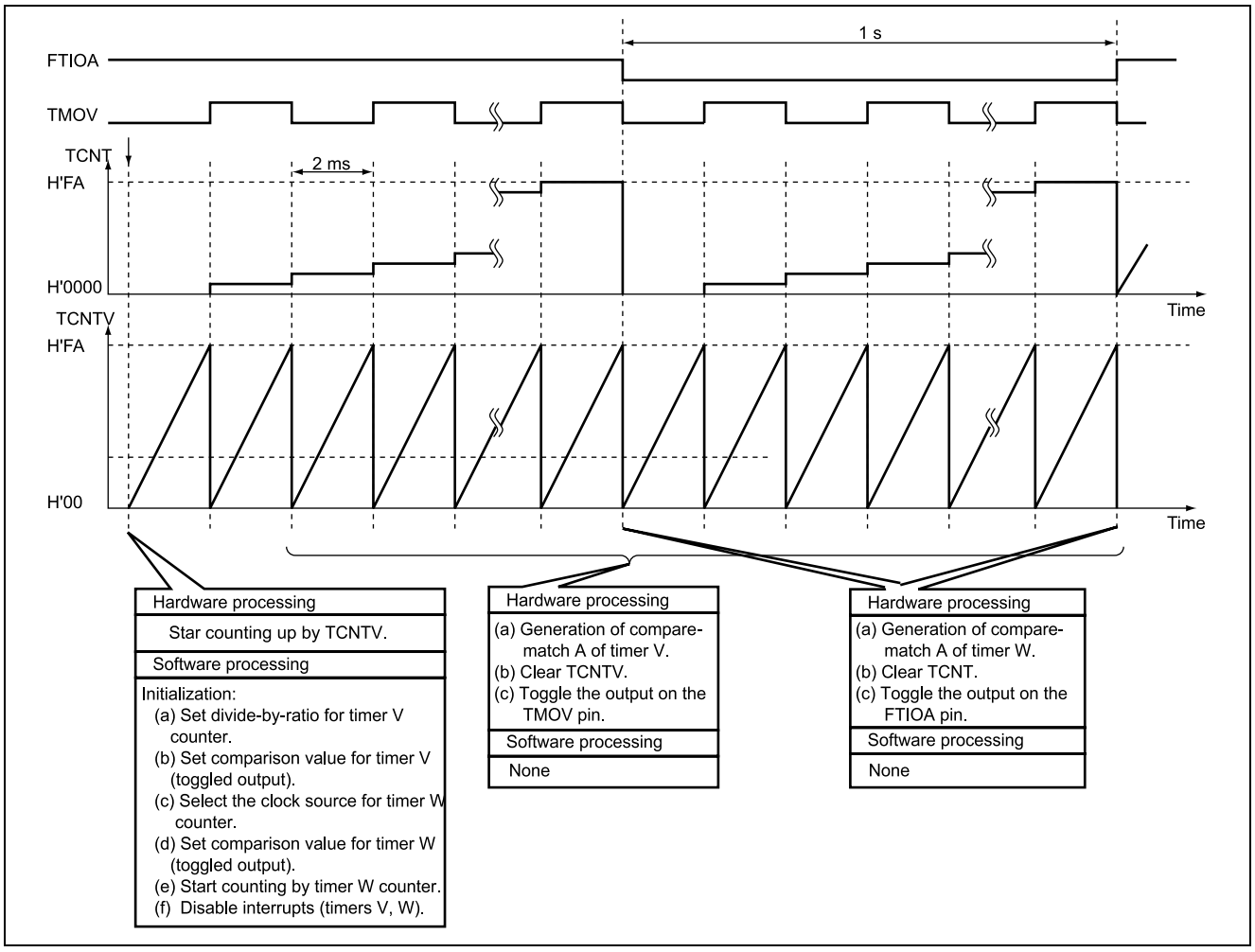


Figure 3.1 Using Timers V and W to Implement a 24-Bit Count-Up Timer: Principle of Operation

4. Description of the Software

4.1 Modules

Table 4.1 lists the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets up the interval timer and 8-bit counter, and enables interrupts.
Timer interrupt	TWINT	Clears interrupt flags.

4.2 Arguments

No arguments are used by this sample task.

4.3 Internal Register Usage

Table 4.2 lists the internal registers used in this sample task.

Table 4.2 Internal Registers Used

- TCRV0 Timer Control Register V0 Address: H'FFA0

Register Name		Function	Setting
TCRV0	CMIEA	Compare-match Interrupt Enable A: When CMIERAW = "1", interrupt-generation according to the value of the CMFA bit in TCSRV is enabled.	0
	CCLR1, CCLR0	Counter Clear 1,0: Setting CCLR1 = "0" and CCLR0 = "1" enables clearing of TCNTV in response to a match for compare-match A.	CCLR1 = 0, CCLR0 = 1
	CKS2, CKS1, CKS0	Clock Select 2 to 0: When these bits are CKS2 = "0", CKS1 = "1", CKS0 = "1", and ICKS0 in TCRV1 = "1", timer V is incremented on the falling edge of the internal clock ϕ/128.	CKS2 = 0, CKS1 = 1, CKS0 = 1

- TCSRV Timer Control Status Register V Address: H'FFA1

Register Name		Function	Setting
TCSRV	OS1, OS0	Output Select 1, 0: When OS1 = "1" and OS0 = "1", the output on the TMOV pin toggles on a match between TCNTV and TCORA.	OS1 = 1, OS0 = 1

- TCORA Time Constant Register A Address: H'FFA2

Register Name	Function	Setting
TCORA	A compare-match A signal is generated when the value in this register and the value of the counter TCNTV match.	H'FA

- TCNTV Timer counter V Address: H'FFA4

Register Name	Function	Setting
TCNTV	An 8-bit up-counter which receives the system clock frequency-divided by 128 as a clock signal.	H'00

- TCRV1 imer Control Register V1 Address: H'FFA5

Register Name		Function	Setting
TCRV1	ICKS0	Internal Clock Select: When ICKS0 = "1" and the bits in TCRV0 are CSK2 = "0", CSK1 = "1", and CSK0 = "1", timer V is incremented on the falling edge of the internal clock ϕ/128.	1

- TMRW imer Mode Register W Address: H'FF80

Register Name		Function	Setting
TMRW	CTS	Timer Counter Start CTS = "1" indicates that counting by TCNT has started. CTS = "0" indicates that counting by TCNT is stopped.	1

- TCRW Timer Control Register W Address: H'FF81

Register Name		Function	Setting
TCRW	CCLR	Counter Clearance: When CCLR = "1", enables clearing of TCNT on compare-match A.	1
	CKS2, CKS1, CKS0	Clock Select 1,0: When these bits are CKS2 = "1", CKS1 = "X", and CKS0 = "X", selects driving of TCNT by the rising edge of the external clock.	CKS2 = 1, CKS1 = X, CKS0 = X
	TOB	Timer Output Level Setting B: When TOB = "1", the level on the FTIOB pin remains high until the compare-match B signal is generated. When TOB = "0", the level on the FTIOB pin remains low until the compare-match B signal is generated.	0
	TOA	Timer Output Level Setting A: When TOA = "1", the level on the FTIOA pin remains high until the compare-match A signal is generated. When TOA = "0", the level on the FTIOA pin remains low until the compare-match A signal is generated.	0

- TIERW Timer Interrupt Enable Register W Address: H'FF82

Register Name		Function	Setting
TIERW	IMIEB	Output Compare Interrupt B Enable: When IMIEB = "0", IMFB interrupts are disabled.	0
	IMIEA	Output Compare Interrupt A Enable: When IMIEA = "1", IMFA interrupts are enabled.	1

- TSRW Timer Status Register W Address: H'FF83

Register Name		Function	Setting
TSRW	IMFB	Output Compare Flag B: IMFB ="0" indicates that the values in TCNT and GRB have not matched yet. IMFB = "1" indicates that the values in TCNT and GRB have matched.	0
	IMFA	Output Compare Flag A: IMFA = "0" indicates that the values in TCNT and GRA have not matched yet. IMFA = "1" indicates that the values in TCNT and GRA have matched.	0

- TIOR0 Timer I/O Control Register 0 Address: H'FF84

Register Name		Function	Setting
TIOR0	IOA2, IOA1, IOA0	I/O Control A2 to A0: When IOA2 = "0", IOA1 = "1", and IOA0 = "1", the output signal on the FTIOA pin is toggled on a compare-match with GRA.	IOA2 = 0, IOA1 = 1, IOA0 = 1

- TCNT Timer Counter Address: H'FF86

Register Name	Function	Setting
TCNT	A 16-bit up-counter which receives the signal from the TMOV pin as an input clock signal.	H'0000

- GRA General Register A Address: H'FF88

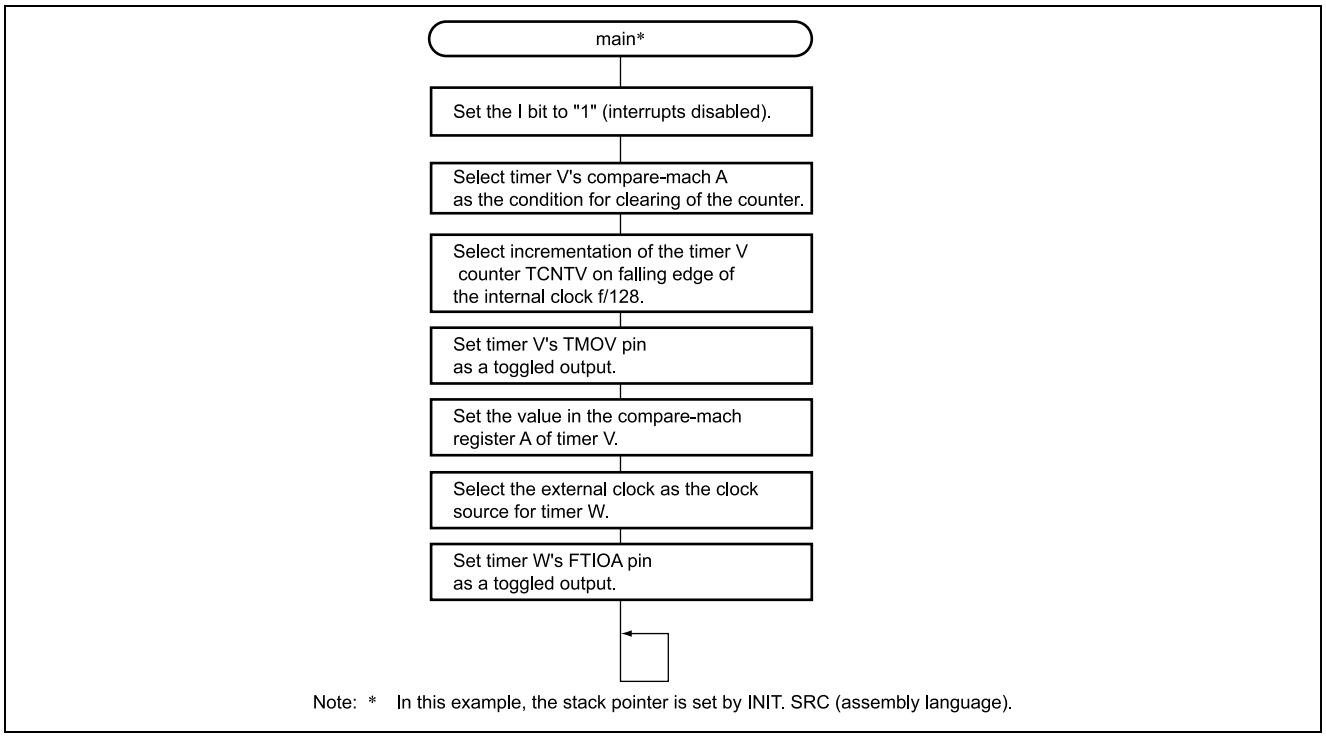
Register Name	Function	Setting
GRA	A compare-match A signal is generated when the value in this register and the value of counter TCNT match.	H'00FA

4.4 RAM Usage

No RAM is used by this sample task.

5. Flowchart

Main routine



Note: * In this example, the stack pointer is set by INIT. SRC (assembly language).

6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300H Tiny Series -H8/3664-                                                                                      */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   24bit Timer using Timer W, Timer V                                                                                 */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer W, Timer V                                                                                                 */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <C:\ch38\include\machine.h>

/************************************************************************************************************************/
/*   Symbol Defnition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
     unsigned char    b7:1;        /* bit7 */
     unsigned char    b6:1;        /* bit6 */
     unsigned char    b5:1;        /* bit5 */
     unsigned char    b4:1;        /* bit4 */
     unsigned char    b3:1;        /* bit3 */
     unsigned char    b2:1;        /* bit2 */
     unsigned char    b1:1;        /* bit1 */
     unsigned char    b0:1;        /* bit0 */
};

#define        TMRW           *(volatile unsigned char *)0xFF80              /* Timer Mode Register W                    */
#define        TMRW_BIT       (*(struct BIT *)0xFF80)                        /* Timer Mode Register W                    */
#define        CTS            TMRW_BIT.b                                     /* Counter Start Bit                        */
#define        TCRW           *(volatile unsigned char *)0xFF81              /* Timer Control Register W                 */
#define        TCRW_BIT       (*(struct BIT *)0xFF81)                        /* Timer Control Register W                 */
#define        WCCLR          TCRW_BIT.b7                                    /* Counter Clear                            */
#define        WCKS2          TCRW_BIT.b6                                    /* Clock Select 2                           */
#define        WCKS1          TCRW_BIT.b5                                    /* Clock Select 1                           */
#define        WCKS0          TCRW_BIT.b4                                    /* Clock Select 0                           */
#define        TIERW          *(volatile unsigned char *)0xFF82              /* Timer Interrupt Enable Register          */
#define        TIERW_BIT      (*(struct BIT *)0xFF82)                        /* Timer Interrupt Enable Register          */
#define        IMIEA          TIERW_BIT.b0                                   /* Input Caputure/Output Compaire           */
#define        TSRW           *(volatile unsigned char *)0xFF83              /* Timer Status Register W                  */
#define        TSRW_BIT       (*(struct BIT *)0xFF83)                        /* Timer Status Register W                  */
#define        IMFA           TSRW_BIT.b0                                    /* Input Caputure/Output Compaire Flag      */
#define        TIOR0          *(volatile unsigned char *)0xFF84              /* Timer Status Register W                  */
#define        TIOR0_BIT      (*(struct BIT *)0xFF84)                        /* Timer Status Register W                  */
#define        IOA2           TIOR0_BIT.b2                                   /* I/O Control A2                           */
#define        IOA1           TIOR0_BIT.b1                                   /* I/O Control A1                           */
#define        IOA0           TIOR0_BIT.b0                                   /* I/O Control A0                           */
#define        TCNT           *(volatile unsigned int *)0xFF86               /* Time Counter H & L                       */
#define        GRA            *(volatile unsigned int *)0xFF88               /* General Register A                       */
#define        TCRV0          *(volatile unsigned char *)0xFFA0              /* Time Constant Register V0                */
#define        TCRV0_BIT      (*(struct BIT *)0xFFA0)                        /* Timer Control Register V0                */
```

```
#define        CMIEB          TCRV0_BIT.b7                          /* Compare Match Interrupt Enable B           */
#define        CMIEA          TCRV0_BIT.b6                          /* Compare Match Interrupt Enable A           */
#define        VCCLR1         TCRV0_BIT.b4                          /* Counter Clear 1                            */
#define        VCCLR0         TCRV0_BIT.b3                          /* Counter Clear 0                            */
#define        VCKS2          TCRV0_BIT.b2                          /* Clock Select 2                             */
#define        VCKS1          TCRV0_BIT.b1                          /* Clock Select 1                             */
#define        VCKS0          TCRV0_BIT.b0                          /* Clock Select 0                             */
#define        TCSRV          *(volatile unsigned char *)0xFFA1     /* Timer Control/Status Register V            */
#define        TCSRV_BIT      (*(struct BIT *)0xFFA1)               /* Timer Control/Status Register V            */
#define        CMFB           TCSRV_BIT.b7                          /* Compare Match Flag B                       */
#define        CMFA           TCSRV_BIT.b6                          /* Compare Match Flag A                       */
#define        OS3            TCSRV_BIT.b3                          /* Output Select 3                            */
#define        OS2            TCSRV_BIT.b2                          /* Output Select 2                            */
#define        OS1            TCSRV_BIT.b1                          /* Output Select 1                            */
#define        OS0            TCSRV_BIT.b0                          /* Output Select 0                            */
#define        TCORA          *(volatile unsigned char *)0xFFA2     /* Time Constant Register A                   */
#define        TCORB          *(volatile unsigned char *)0xFFA3     /* Time Constant Reguster B                   */
#define        TCNTV          *(volatile unsigned char *)0xFFA4     /* Timer Counter V                            */
#define        TCRV1_BIT      (*(struct BIT *)0xFFA5                /* Timer Control Register V1                  */
#define        TVEG1          TCRV1_BIT.b4                          /* TRGV Input Edge Select 1                   */
#define        TVEG0          TCRV1_BIT.b3                          /* TRGV Input Edge Select 0                   */
#define        TRGE           TCRV1_BIT.b2                          /* TRGV Input Enable                          */
#define        ICKS0          TCRV1_BIT.b0                          /* Internal Clock Select 0                    */

#pragma        interrupt    (TWINT)

/************************************************************************************************************************/
/*   Function definition                                                                                                */
/************************************************************************************************************************/
extern  void    INIT( void );                                       /* SP Set                                     */
void    main      ( void );
void    TWINT     ( void );

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma    section        V1                                        /* VECTOR SECTOIN SET                         */
void (*const VEC_TBL1[])(void) = {                                  /* 0x00 - 0x0f                                */
     INIT                                                           /* 00 Reset                                   */
};

#pragma    section                                                  /* P                                          */

/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     _INITSCT();

     VCCLR0 = 1;                                                    /* Compare Match A Clear                      */
     VCCLR1 = 0;
     VCKS0 = 1;                                                     /* Internal Clock φ/128 Falling Edge Count Up  */
     VCKS1 = 1;
     VCKS2 = 0;
     ICKS0 = 1;
     OS0 = 1;                                                       /* Toggle Output Every Compare Match A        */
     OS1 = 1;
```

```
    TCORA = 0xFA;                                   /* Timer V Compare Register Set              */

    WCCLR = 1;                                      /* Timer W Clock Source External Input       */
    WCKS2 = 1;
    WCKS1 = 1;
    WCKS0 = 1;
    IOA0 = 1;                                       /* Output Compare Match Output enable        */
    IOA1 = 1;
    IOA2 = 0;

    GRA = 0xFA;

    CTS = 1;                                        /* Timer W Start                             */

    while(1){
        ;
        }
}
```

Link address specification

Section Name	Address
CV1	H'0000
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.