

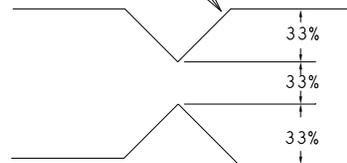
NOTES: UNLESS OTHERWISE SPECIFIED

1. COMPLIANCE.
  - A. THE PCB SHALL MEET ROHS (LEAD FREE) STANDARDS.
  - B. THE PCB SHALL MEET IPC-6012B CLASS 2 REQUIREMENTS.
2. MATERIAL.
  - A. BASE LAMINATE. ISOLA 370HR OR EQUIVALENT WITH A THERMAL RESISTANCE OF 260 DEGREES C OR HIGER FOR ROHS COMPLINANCE.
  - B. BONDING MATERIAL. PRE-IMPREGNATED PER IPC-4101/24 (TYPE GFG) WITH MINIMUM Tg 150 AND Td 325.
3. FINISH.
  - A. ELECTROLESS NICKEL / IMMERSION GOLD (ENIG).
  - B. NICKEL SHALL BE A MINIMUM OF 118 MICRO INCHES.
  - C. GOLD SHALL BE A MINIMUM OF 2 MICRO INCHES.
4. HOLE DRILLING:
 

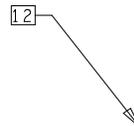
ALL HOLES TO BE WITHIN .003" OF TRUE POSTIO.
5. PLATING:
 

ALL PLATED HOLDS SHALL HAVE A MINIMUM WALL THICKNESS OF .0007" COPPER. ALL HOLE DIAMETERS ARE AFTER PLATING. ALL ANNULAR RINGS SHALL BE .002" OR GREATER.
6. SOLDERMASK- LIQUID PHOTO IMAGEABLE OVER BARE COPPER  
 COLOR BLACK MATTE TO BE APPLIED TO BOTH SIDES ACCORDING TO IPC-SM-840C..
7. SILKSCEEN - SHALL BE WHITE BASE EPOXY PAINT TO BE APPLIED TO BOTHE SIDES THERE SHALL BE NO SILKSCREEN ON ANY EXPOSED PADS.
8. THIEVING - THIEVING MAY BE ADDED TO COMPENSATEFOR LOW COPPER DENSITY  
 THIEVING SHALL NOT BE ADDED TO WITHIN 3.8mm MINIMUM DISTANCE TO ANY EXISTING FEATURE. THERE SHALL BE NO EXPOSED THIEVING.
9. PCB VENDOR SHALL PROVIDE, CERTIFICATE OF CONFORMANCE.
10. PCB VENDOR IDENTIFICATION, DATE CODE, UL CODE (94V-0) AND UR SYMBOL TO BE MARKED USING SILKSCREEN ON THE TOP SIDE. (OR BOTTOM SIDE IF NEED BE)
11. ELECTRICAL TEST - BOARDS SHALL BE ELECTICALLY TESTED FOR CONTINUITY AND ISOLATION IN ACCORRDACE WITH IPC-6012. AN IPC-365 NETLIST FILE IS PROVIDED. EXCEPTIONS TO THE INTEGRITY OF THE ELECTRICAL TEST ARE AS FOLLOWS:  
 INTERTIONAL SHORTS: NONE  
 INTERTIONAL OPENS: NONE
12. CONTROLLED DIELECTRIC- THE DIELECTRIC THICKNESS FOR EACH LAYER. SHALL BE AS PRESCRIBED IN THE LAYERRING DETAIL SHOWN BELOW.
13. EXPOSED COPPER - THER SHAL BE NO EXPOSED COPPER.
14. PCB manufacturing and assembly to be according to data files shown in Gerber file table listed in bare board drawing.
15. V-GROOVE BOARD AT X=0mm and X=24mm  
 AND DO NOT CUT OR BREAK AT GROOVE.

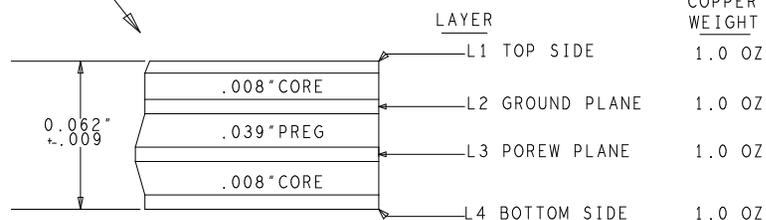
V\_GROOVE DETAILS [16]



CONTROLLED DIELECTRIC [12]



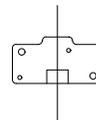
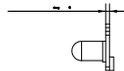
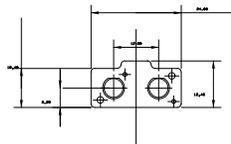
LAYERING DETAIL  
SCALE=NONE



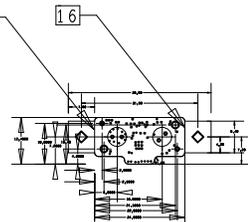
FINISHED  
COPPER  
WEIGHT

| LAYER           | FINISHED COPPER WEIGHT |
|-----------------|------------------------|
| L1 TOP SIDE     | 1.0 OZ                 |
| L2 GROUND PLANE | 1.0 OZ                 |
| L3 POREW PLANE  | 1.0 OZ                 |
| L4 BOTTOM SIDE  | 1.0 OZ                 |

| DRILL CHART: TOP to BOTTOM   |        |             |        |     |
|------------------------------|--------|-------------|--------|-----|
| ALL UNITS ARE IN MILLIMETERS |        |             |        |     |
| FIGURE                       | SIZE   | TOLERANCE   | PLATED | QTY |
| •                            | 0.254  | +0.03/-0.03 | PLATED | 24  |
| •                            | 0.254  | +0.03/-0.03 | PLATED | 44  |
| •                            | 0.8128 | +0.03/-0.03 | PLATED | 4   |
| •                            | 1.1    | +0.03/-0.03 | PLATED | 2   |
| o                            | 1.8    | +0.03/-0.03 | PLATED | 2   |
| ◇                            | 3.0    | +0.3/-0.3   | PLATED | 2   |



V\_GROOVE [16]



|                                |                               |   |          |           |
|--------------------------------|-------------------------------|---|----------|-----------|
| ENGINEER:<br>Scott Jenney      | DRAWN BY:<br>Scott Jenney     | BOARD NUMBER:<br><br>ISL29501-CS1Z                                |          |           |
| RELEASED BY:                   | DATE DRAWN:<br>April 27, 2016 | Intersil Corporation<br>1001 MURPHY RANCH RD<br>MILPITAS CA 95035 |          |           |
| UPDATED BY:<br>Scott Jenney    | DATE RELEASES:                | MASK  | HOWR ID: | REV:<br>A |
| DATE UPDATED:<br>April 7, 2016 |                               | FILENAME<br>ISL29501 CAT SHARK<br>FABRICATION DRAWING             |          |           |
| intersil                       |                               |   |          |           |