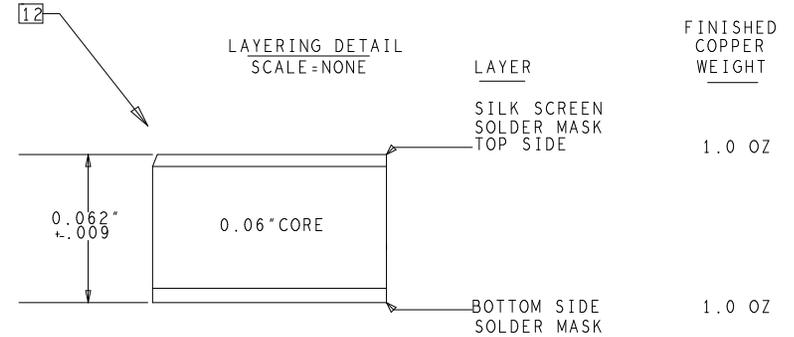


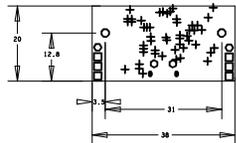
NOTES: UNLESS OTHERWISE SPECIFIED

1. COMPLIANCE.
 - A. THE PCB SHALL MEET ROHS (LEAD FREE) STANDARDS.
 - B. THE PCB SHALL MEET IPC-6012 CLASS 2 REQUIREMENTS.
2. MATERIAL.
 - A. BASE LAMINATE. ISOLA 370HR OR EQUIVALENT WITH A THERMAL RESISTANCE OF 260 DEGREES C OR HIGHER FOR ROHS COMPLIANCE.
 - B. BONDING MATERIAL. PRE-IMPREGNATED PER IPC-4101/24 (TYPE GFG) WITH MINIMUM Tg 150 AND Td 325.
3. FINISH.
 - A. ELECTROLESS NICKEL / IMMERSION GOLD (ENIG).
 - B. NICKEL SHALL BE A MINIMUM OF 118 MICRO INCHES.
 - C. GOLD SHALL BE A MINIMUM OF 2 MICRO INCHES.
4. HOLE DRILLING:
 - A. ALL HOLES TO BE WITHIN .003" OF TRUE POSTIO.
5. PLATING:
 - A. ALL PLATED HOLDS SHALL HAVE A MINIMUM WALL THICKNESS OF .0007" COPPER. ALL HOLE DIAMETERS ARE AFTER PLATING.
 - B. ALL ANNULAR RINGS SHALL BE .002" OR GREATER.
6. SOLDERMASK- LIQUID PHOTO IMAGEABLE OVER BARE COPPER COLOR BLACK MATTE TO BE APPLIED TO BOTH SIDES ACCORDING TO IPC-SM-840C.
7. SILKSCREEN - SHALL BE WHITE BASE EPOXY PAINT TO BE APPLIED TO BOTH SIDES. THERE SHALL BE NO SILKSCREEN ON ANY EXPOSED PADS.
8. THIEVING - THIEVING MAY BE ADDED TO COMPENSATE FOR LOW COPPER DENSITY THIEVING SHALL NOT BE ADDED TO WITHIN 3.8mm MINIMUM DISTANCE TO ANY EXISTING FEATURE. THERE SHALL BE NO EXPOSED THIEVING.
9. PCB VENDOR SHALL PROVIDE, CERTIFICATE OF CONFORMANCE.
10. PCB VENDOR IDENTIFICATION, DATE CODE, UL CODE (94V-0) AND UR SYMBOL TO BE MARKED USING SILKSCREEN ON THE TOP SIDE. (OR BOTTOM SIDE IF NEED BE)
11. ELECTRICAL TEST - BOARDS SHALL BE ELECTRICALLY TESTED FOR CONTINUITY AND ISOLATION IN ACCORDANCE WITH IPC-6012. AN IPC-365 NETLIST FILE IS PROVIDED. EXCEPTIONS TO THE INTEGRITY OF THE ELECTRICAL TEST ARE AS FOLLOWS:
 - INTENTIONAL SHORTS: NONE
 - INTENTIONAL OPENS: NONE
12. CONTROLLED DIELECTRIC- THE DIELECTRIC THICKNESS FOR EACH LAYER. SHALL BE AS PRESCRIBED IN THE LAYERING DETAIL SHOWN BELOW.
13. EXPOSED COPPER - THERE SHALL BE NO EXPOSED COPPER.
14. PCB manufacturing and assembly to be according to data files shown in Gerber file table listed in bare board drawing.

CONTROLLED DIELECTRIC



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
+	0.254	+0.03/-0.03	PLATED	50
□	0.9144	+0.03/-0.03	PLATED	6
○	0.9144	+0.03/-0.03	PLATED	2
○	1.016	+0.03/-0.03	PLATED	2
○	3.0	+0.03/-0.03	PLATED	2
•	1.3208x0.762	+0.03/-0.03	PLATED	2



Design History

- REV A - Initial Release
- Rev B - Add pullup to U1-11, move R8, Move FB3 and R9 Silk.

ENGINEER: Scott Jenney	DRAWN BY: Scott Jenney	BOARD NUMBER: ISLI2UEV1Z Intersil Corporation 1001 MURPHY RANCH RD MILPITAS CA 95035		
RELEASED BY:	DATE DRAWN: Apr 11 16, 2016	MASK#	DDR ID:	REV: B
UPDATED BY:	DATE RELEASED:	FILENAME Microcontroller Interface Board		