

ISLA214S50IR48EV1Z

- Title
- Device Under Test
- Analog Inputs & Sampling Clock
- Vita57 Interface, ID and Config EEPROM
- Power Regulator

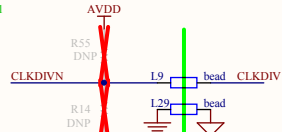
Assembly Variant: ISLA214S50IR48EV1Z

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Title		Title	
Size	Number	Revision	
B	1	B	
Date:	1/5/2012	Sheet 1 of	5
File:	H:\Work\Title.SchDoc	Drawn By:	

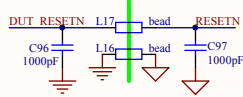
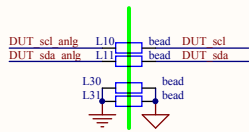
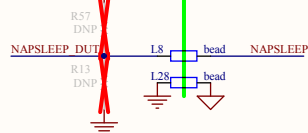
Clock Division

HI= clk_div1
LO clk_div2

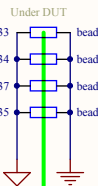
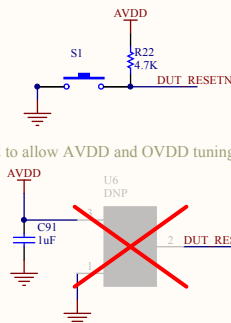


Nap/Sleep

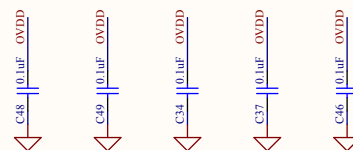
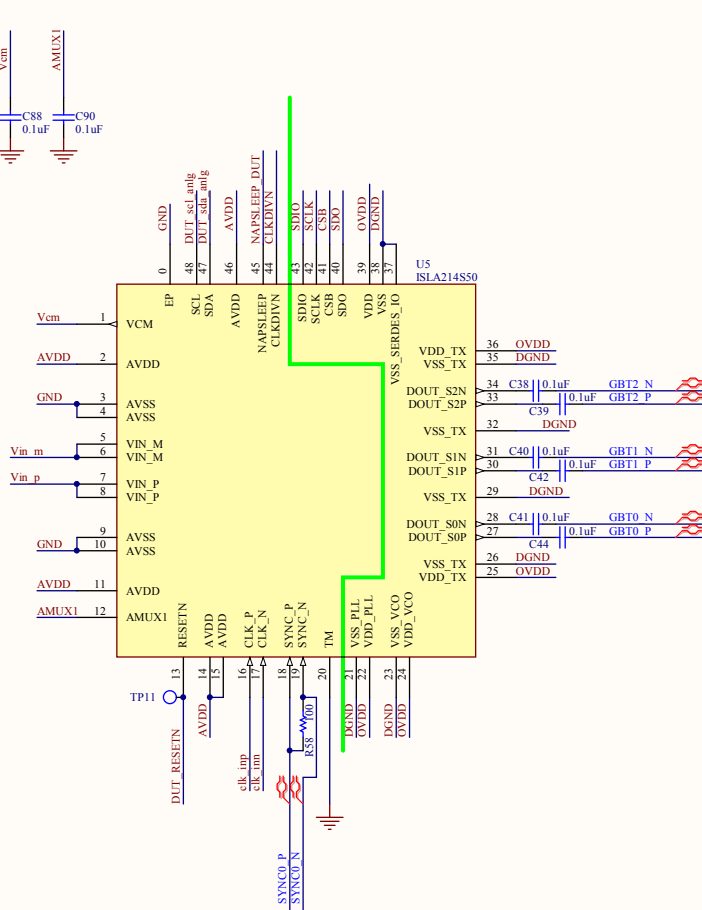
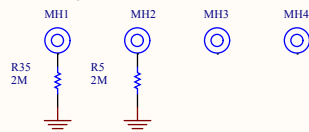
HI= Sleep
FI= Nap
LO = Normal



DNP U2 to allow AVDD and OVDD tuning below 1.7V



Plated tooling holes
Adjacent to J4



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A

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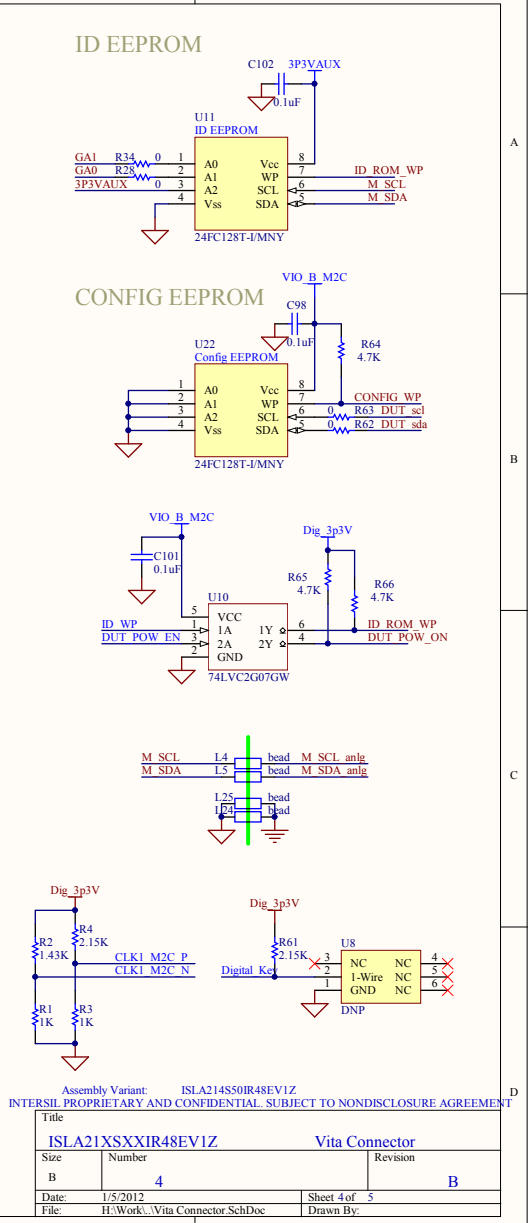
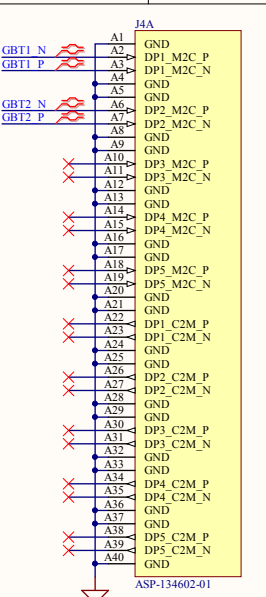
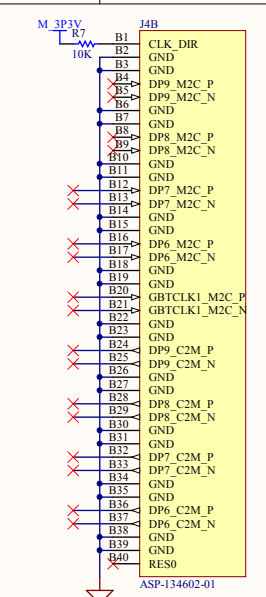
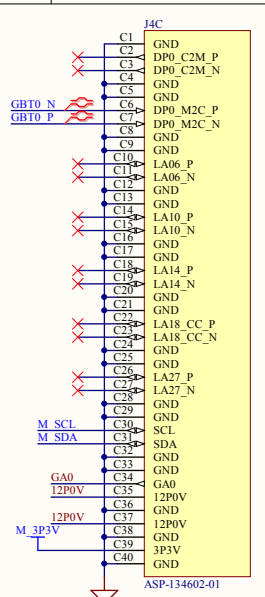
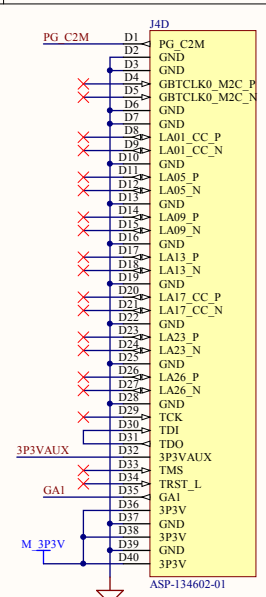
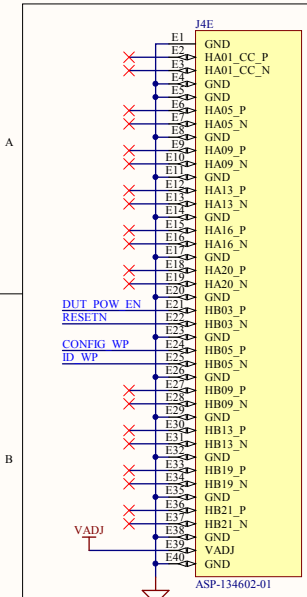
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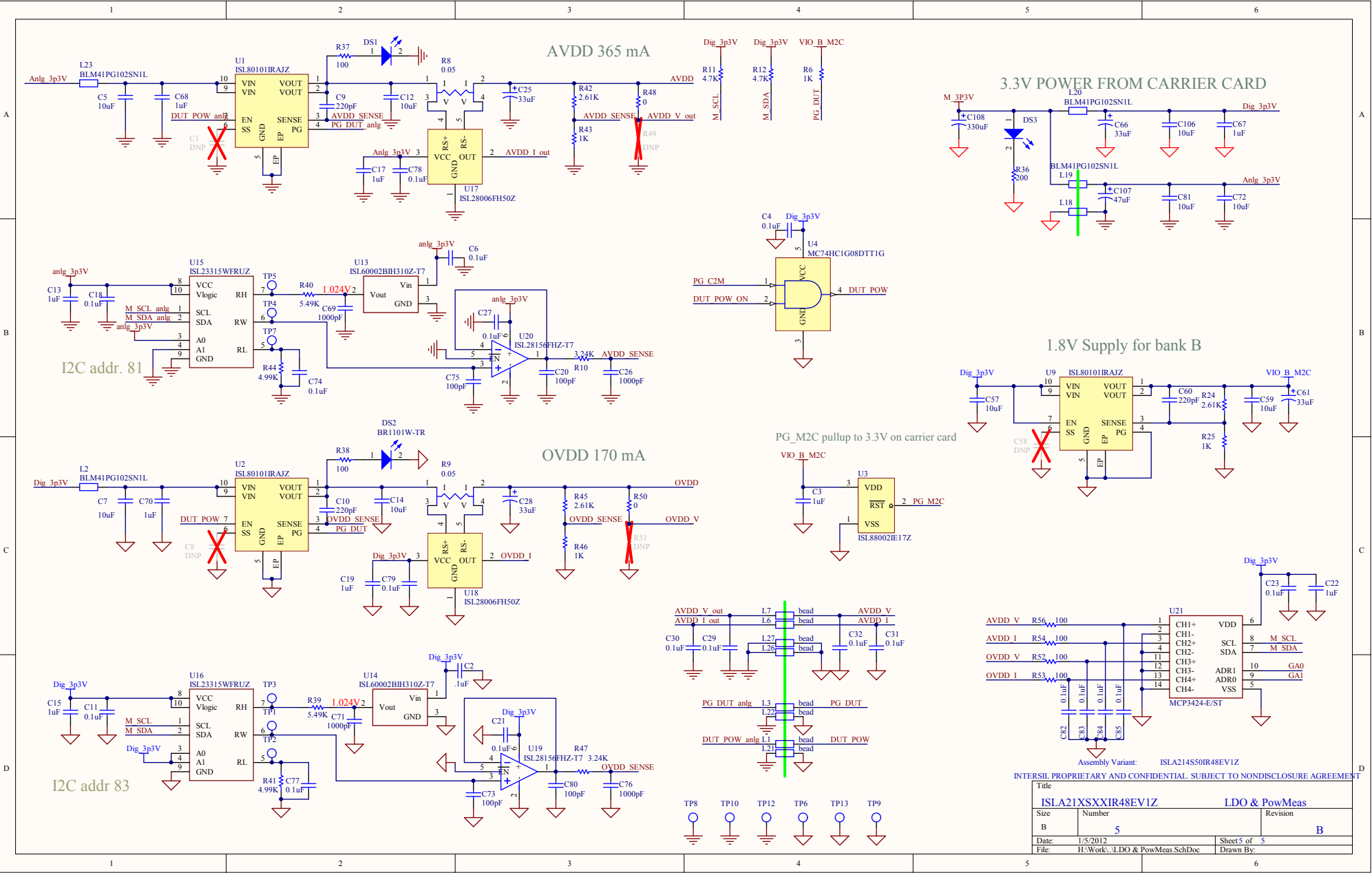
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D





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