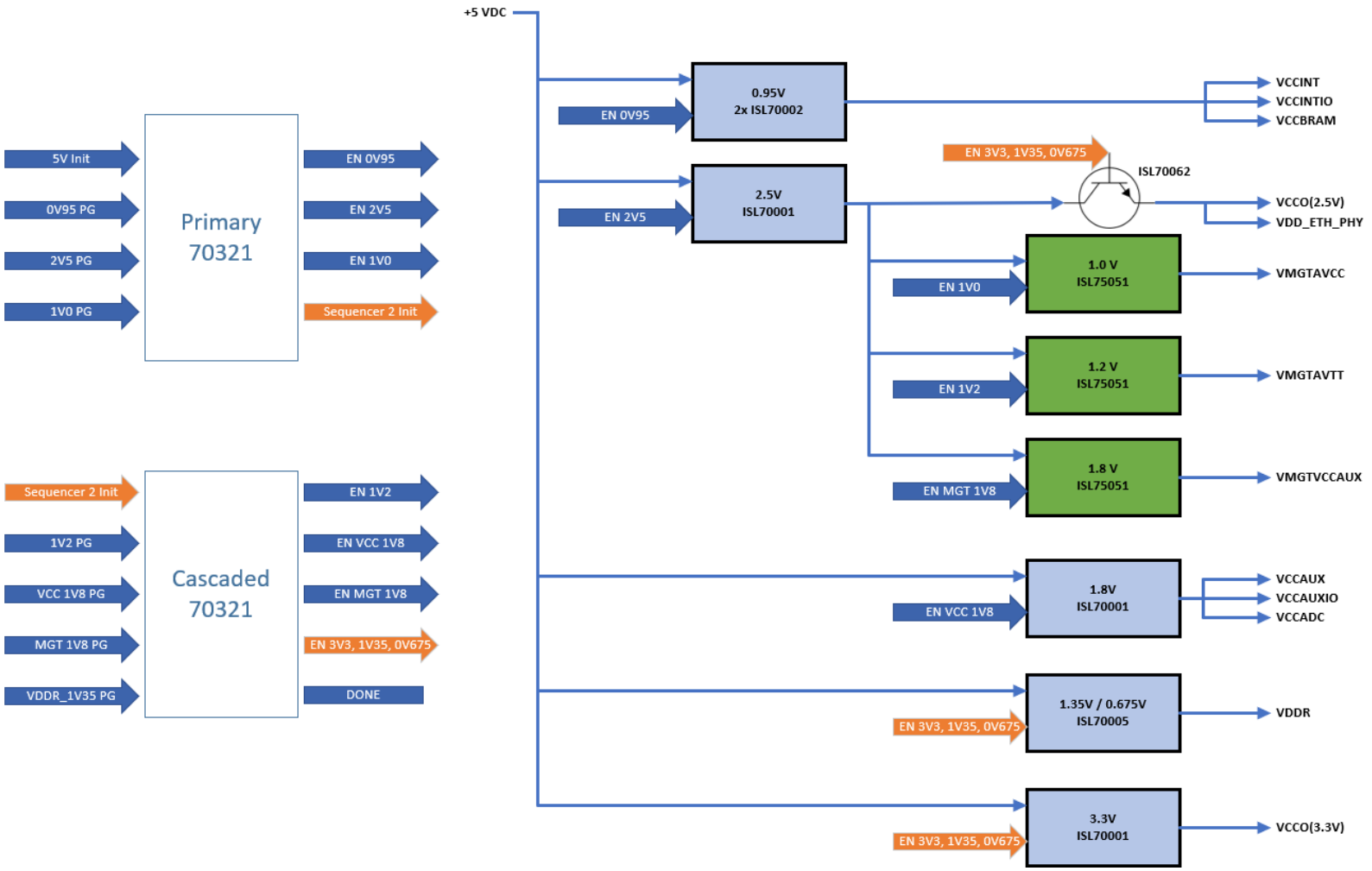
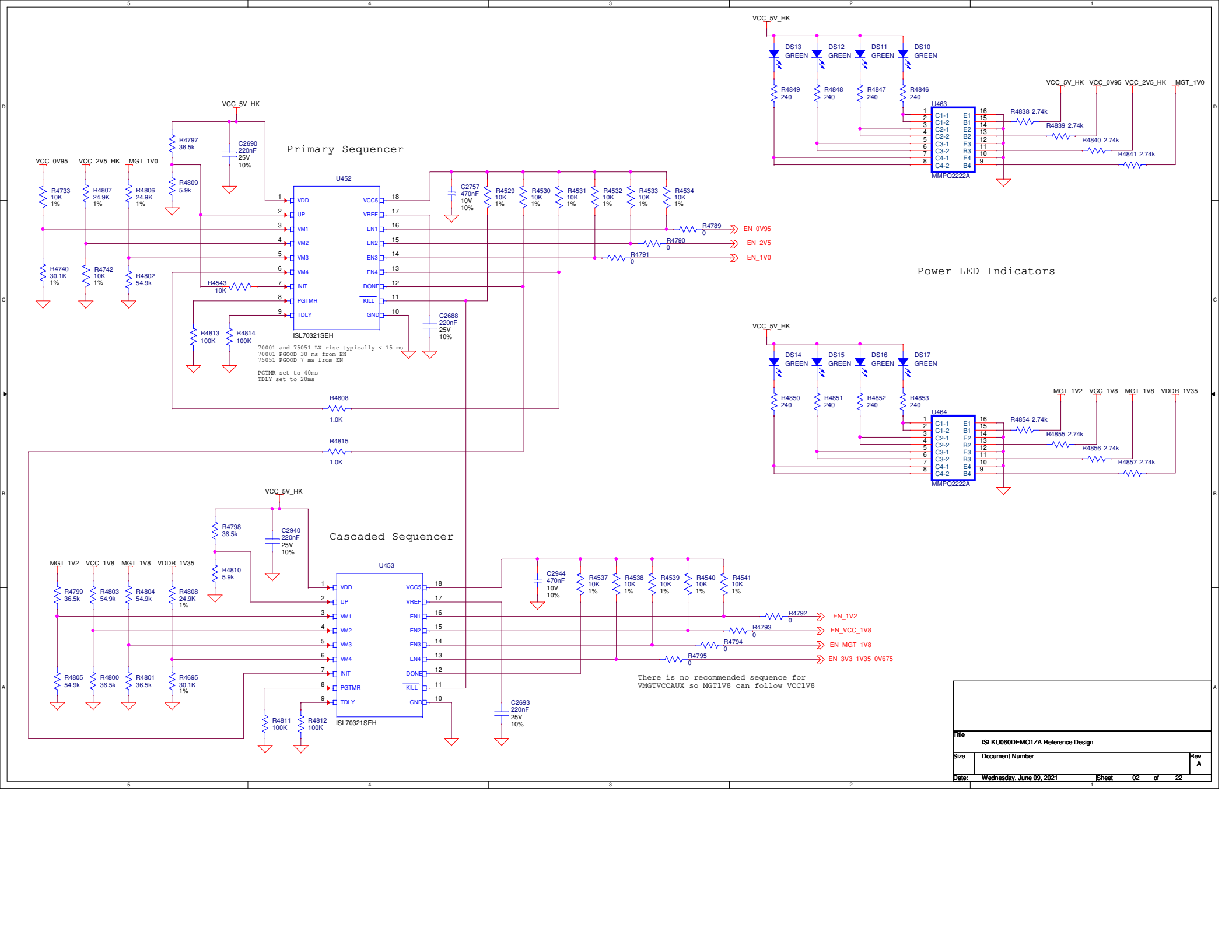
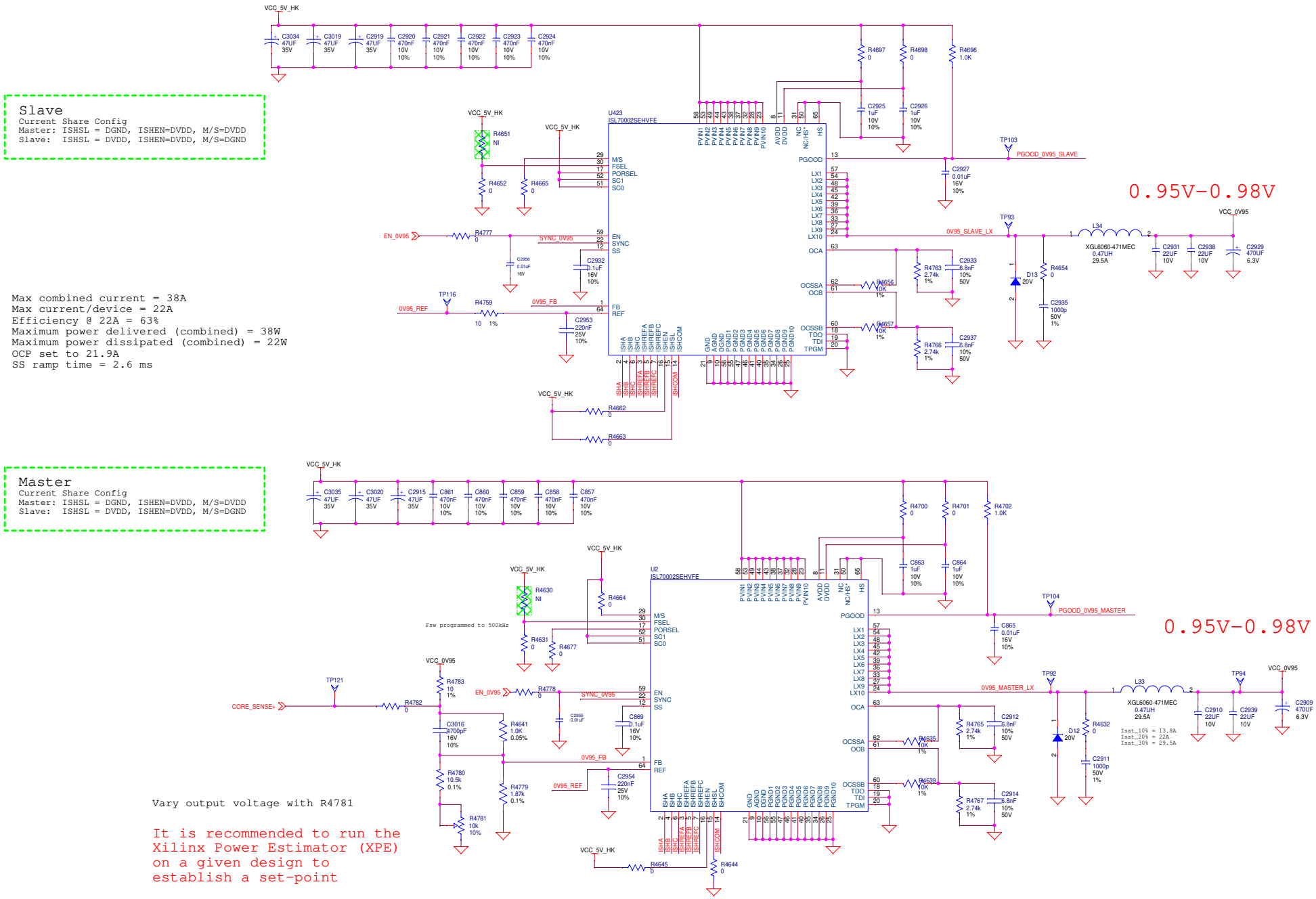
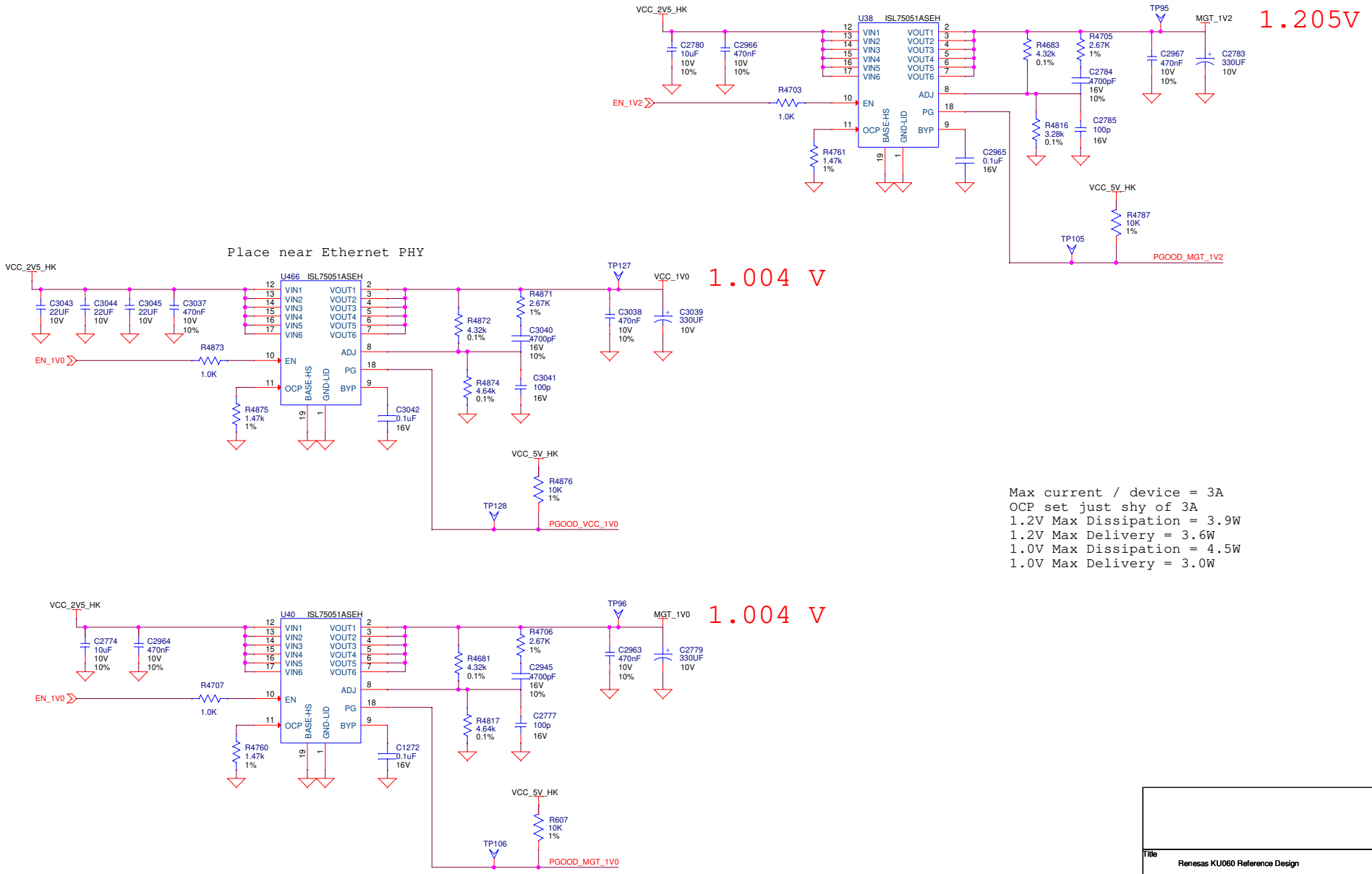
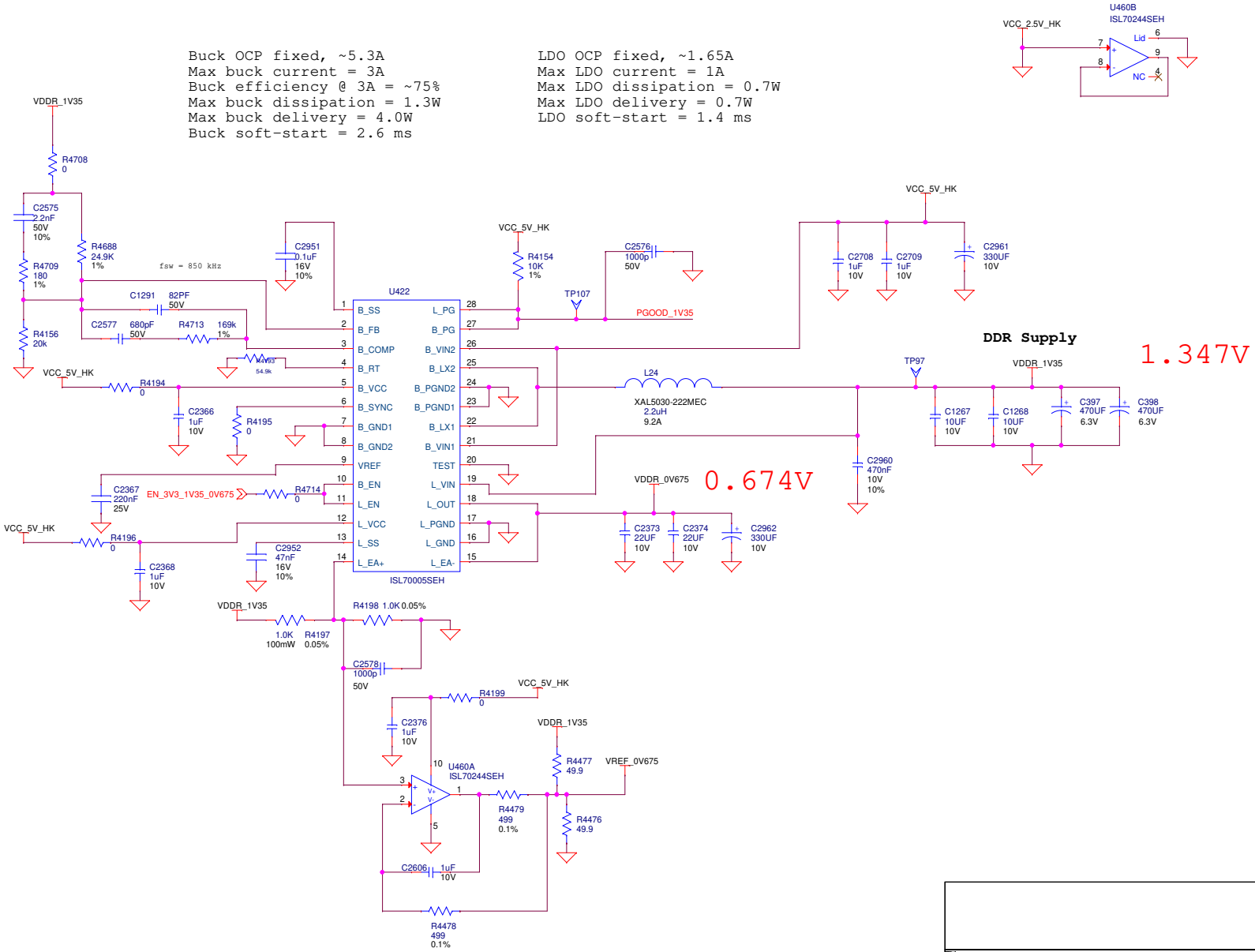


Title	ISLKU060DEMO1ZA Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 01 of 22	


Primary Sequencer
Cascaded Sequencer
Power LED Indicators
U452
U453
U463
U464
ISL70321SEH
MMPQ2222A
VCC_5V_HK
VCC_0V95
VCC_2V5_HK
MGT_1V0
MGT_1V2
VCC_1V8
MGT_1V8
VDDR_1V35
EN_0V95
EN_2V5
EN_1V0
EN_1V2
EN_VCC_1V8
EN_MGT_1V8
EN_3V3_1V35_0V675
70001 and 75051 LX rise typically < 15 ms
70001 PGOOD 30 ms from EN
75051 PGOOD 7 ms from EN
PGTMR set to 40ms
TDLY set to 20ms
There is no recommended sequence for
VMGTVCCAUX so MGT1V8 can follow VCC1V8
Title
ISLKU060DEMO1ZA Reference Design
Size
Document Number
Rev
A
Date:
Wednesday, June 09, 2021
Sheet
02
of
22

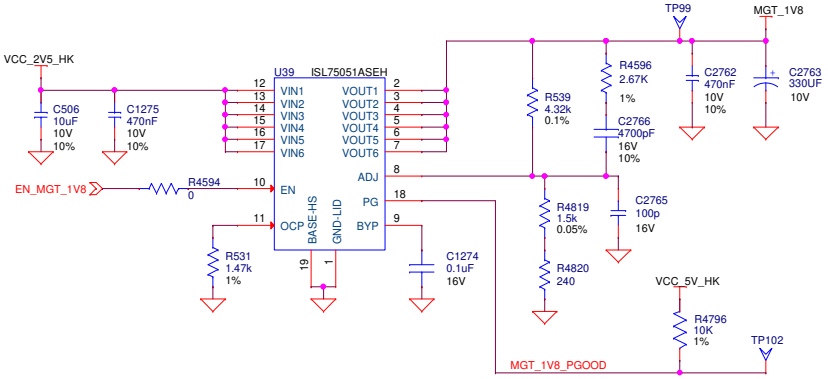

Slave
Current Share Config
Master: ISHSL = DGND, ISHEN=DVDD, M/S=DVDD
Slave: ISHSL = DVDD, ISHEN=DVDD, M/S=DGND
Max combined current = 38A
Max current/device = 22A
Efficiency @ 22A = 63%
Maximum power delivered (combined) = 38W
Maximum power dissipated (combined) = 22W
OCP set to 21.9A
SS ramp time = 2.6 ms
0.95V-0.98V
Master
Current Share Config
Master: ISHSL = DGND, ISHEN=DVDD, M/S=DVDD
Slave: ISHSL = DVDD, ISHEN=DVDD, M/S=DGND
Fsw programmed to 500kHz
0.95V-0.98V
Vary output voltage with R4781
It is recommended to run the Xilinx Power Estimator (XPE) on a given design to establish a set-point
ISLKU060DEMO1ZA Reference Design
Document Number
Wednesday, June 09, 2021
Sheet 03 of 22


VCC_2V5_HK
C2780 10uF 10V 10%
C2966 470nF 10V 10%
U38 ISL75051ASEH
VIN1 VIN2 VIN3 VIN4 VIN5 VIN6
VOUT1 VOUT2 VOUT3 VOUT4 VOUT5 VOUT6
EN
ADJ
PG
OCP
BYP
BASE-HS
GND-LID
EN_1V2
R4703 1.0K
R4761 1.47k 1%
C2965 0.1uF 16V
R4683 4.32k 0.1%
R4705 2.67K 1%
C2784 4700pF 16V 10%
R4816 3.28k 0.1%
C2785 100p 16V
TP95
MGT_1V2
C2967 470nF 10V 10%
C2783 330UF 10V
1.205V
VCC_5V_HK
R4787 10K 1%
TP105
PGOOD_MGT_1V2
Place near Ethernet PHY
VCC_2V5_HK
C3043 22UF 10V
C3044 22UF 10V
C3045 22UF 10V
C3037 470nF 10V 10%
U466 ISL75051ASEH
EN_1V0
R4873 1.0K
R4875 1.47k 1%
C3042 0.1uF 16V
R4872 4.32k 0.1%
R4874 4.64k 0.1%
R4871 2.67K 1%
C3040 4700pF 16V 10%
C3041 100p 16V
TP127
VCC_1V0
C3038 470nF 10V 10%
C3039 330UF 10V
1.004 V
VCC_5V_HK
R4876 10K 1%
TP128
PGOOD_VCC_1V0
Max current / device = 3A
OCP set just shy of 3A
1.2V Max Dissipation = 3.9W
1.2V Max Delivery = 3.6W
1.0V Max Dissipation = 4.5W
1.0V Max Delivery = 3.0W
VCC_2V5_HK
C2774 10uF 10V 10%
C2964 470nF 10V 10%
U40 ISL75051ASEH
EN_1V0
R4707 1.0K
R4760 1.47k 1%
C1272 0.1uF 16V
R4681 4.32k 0.1%
R4817 4.64k 0.1%
R4706 2.67K 1%
C2945 4700pF 16V 10%
C2777 100p 16V
TP96
MGT_1V0
C2963 470nF 10V 10%
C2779 330UF 10V
1.004 V
VCC_5V_HK
R607 10K 1%
TP106
PGOOD_MGT_1V0
Title
Renesas KU060 Reference Design
Size
Document Number
Rev A
Date: Wednesday, June 09, 2021
Sheet 04 of 22

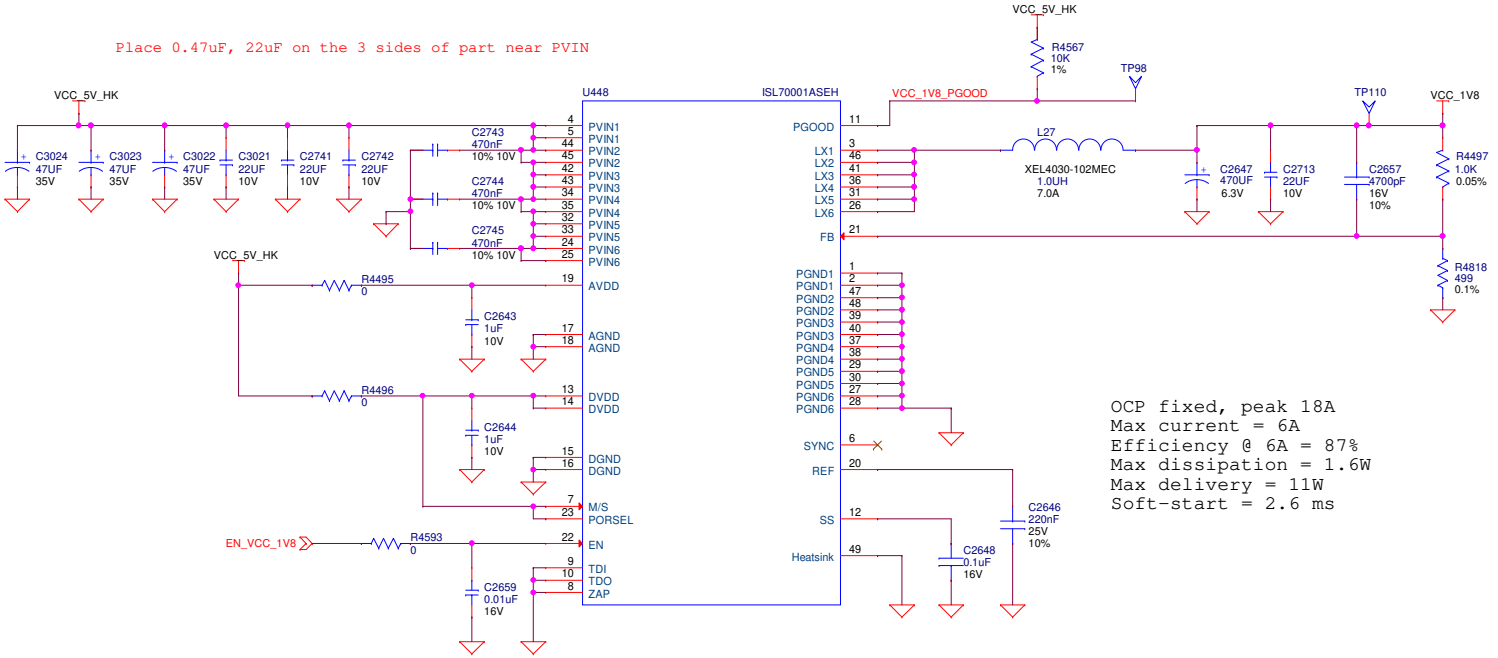


Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 05 of 22	

Max LDO current = 3A
Max LDO dissipation = 2.1W
Max LDO delivery = 5.4W
OCP set just shy of 3A



Place 0.47uF, 22uF on the 3 sides of part near PVIN

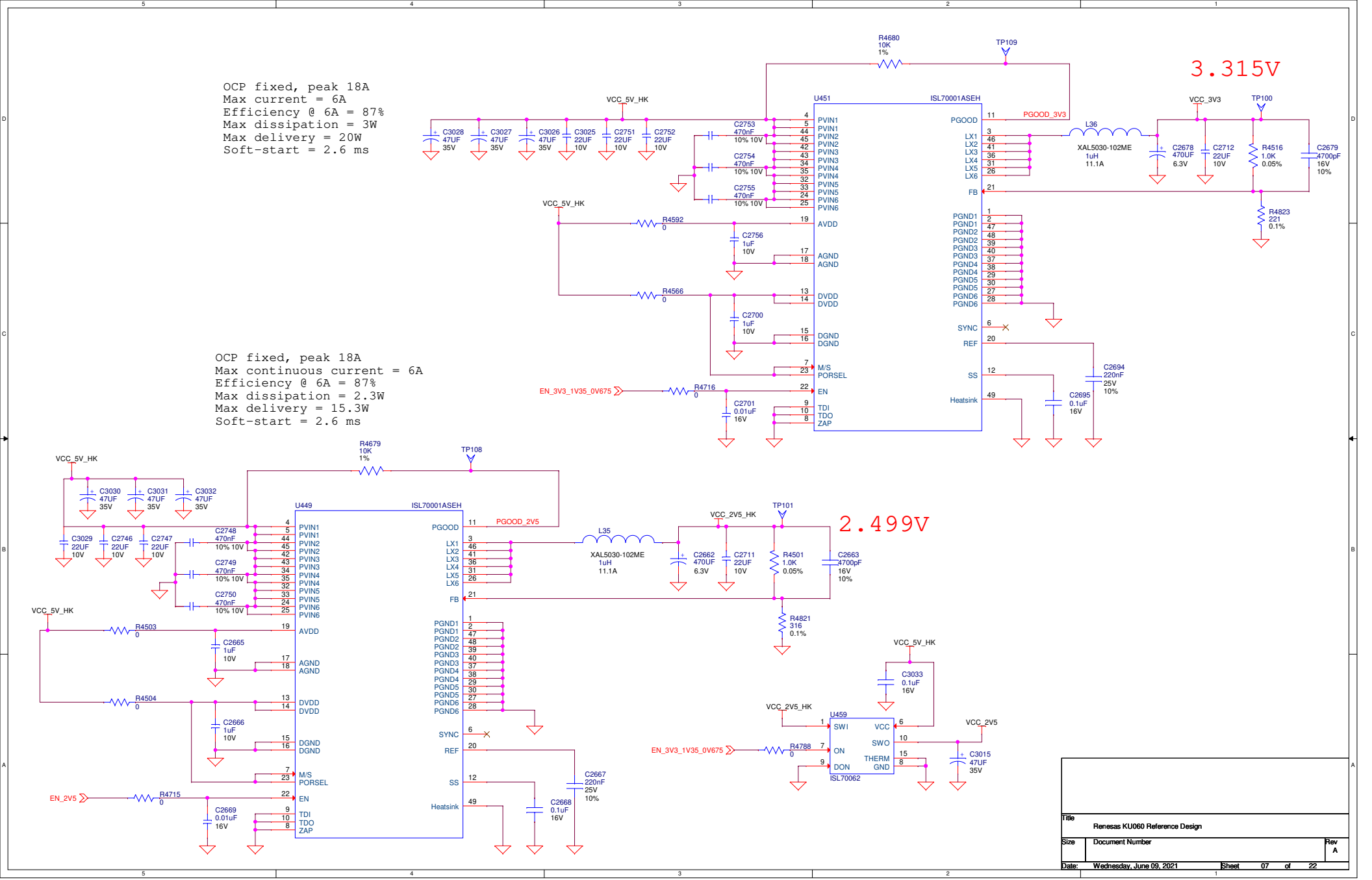


OCP fixed, peak 18A
Max current = 6A
Efficiency @ 6A = 87%
Max dissipation = 1.6W
Max delivery = 11W
Soft-start = 2.6 ms

Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 06 of 22	

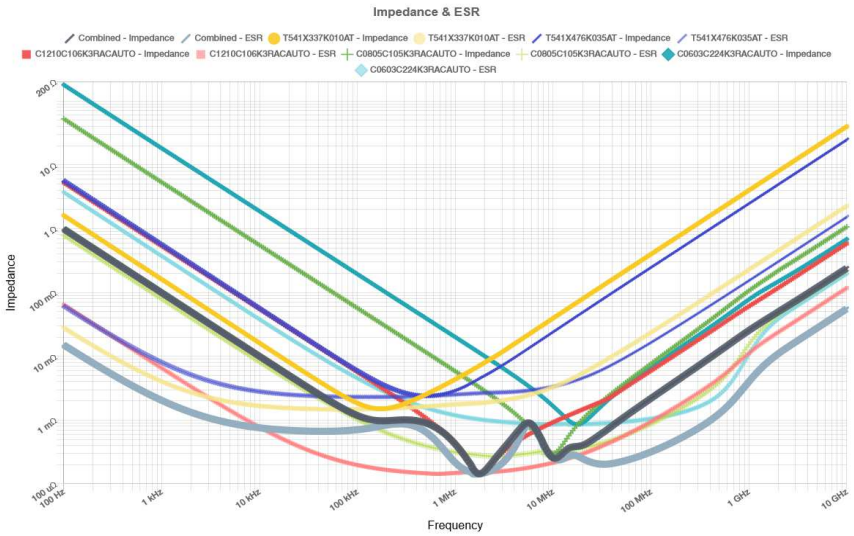
OCP fixed, peak 18A
Max current = 6A
Efficiency @ 6A = 87%
Max dissipation = 3W
Max delivery = 20W
Soft-start = 2.6 ms

OCP fixed, peak 18A
Max continuous current = 6A
Efficiency @ 6A = 87%
Max dissipation = 2.3W
Max delivery = 15.3W
Soft-start = 2.6 ms

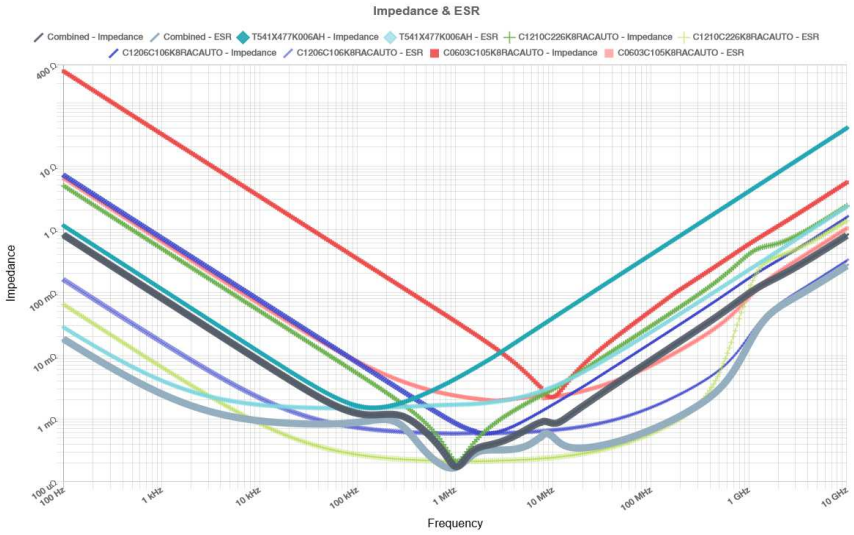


Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 07 of 22	

Xilinx Reference Decoupling Network Impedance:



BOM-Optimized Decoupling Network Impedance:



Decoupling designed to a 6A load step

Recommended PCB Capacitors per Device

Example decoupling capacitor quantities for the XQRKU060-CNA1509 device are listed in Table 77 to Table 81. The optimized quantities of PCB decoupling capacitors assume that the voltage regulators have stable output voltages and meet the regulator manufacturer's minimum output capacitance requirements. These recommendations assume a regulator (DC) tolerance of ±2% and an AC tolerance of ±1%, except for V_{CCINT} which assumes an AC tolerance of ±2%. The total of the DC and AC tolerances must be within the recommended operating conditions specified in Table 9.

Table 77: **Decoupling Capacitor Quantities for V_{CCINT} with Sample Step Currents**

VCCINT/VCCBRAM/VCCINT_IO Combined or VCCINT/VCCINT_IO Combined[1]					
Step current (A)	**330 µF**	**47 µF**	**10 µF**	**1.0 µF**	**0.22 µF**
6	3	6	30	30	40
5	2	5	19	21	25
4	1	4	16	16	16
3	1	2	8	8	8
2	1	1	3	3	3

Notes:
1. VCCINT_IO is tied internally in the CNA1509 package to VCCINT.
2. Step current is typically a fraction of dynamic current; roughly 15–33%.

Table 78: **Decoupling Capacitor Quantities for V_{CCBRAM}**

V_{CCBRAM}	
47 µF	**10 µF**
1	1

Table 79: **Decoupling Capacitor Quantities for V_{CCAUX}/V_{CCAUX_IO}**

V_{CCAUX}/V_{CCAUX_IO} (combined)	
47 µF	**10 µF**
1	1

Notes:
1. Based on 2.0A of I_{CCAUX} + I_{CCAUX_IO} dynamic current.

Table 80: **Decoupling Capacitor Quantities for V_{CCO} per Bank**

V_{CCO_HP} (per bank) or V_{CCO_HR} (per bank)	
47 µF	**10 µF**
1	1

Notes:
1. When combining banks, one 47 µF can power up to four connected banks.

Table 81: **Decoupling Capacitor Specifications and Sample Part Numbers**

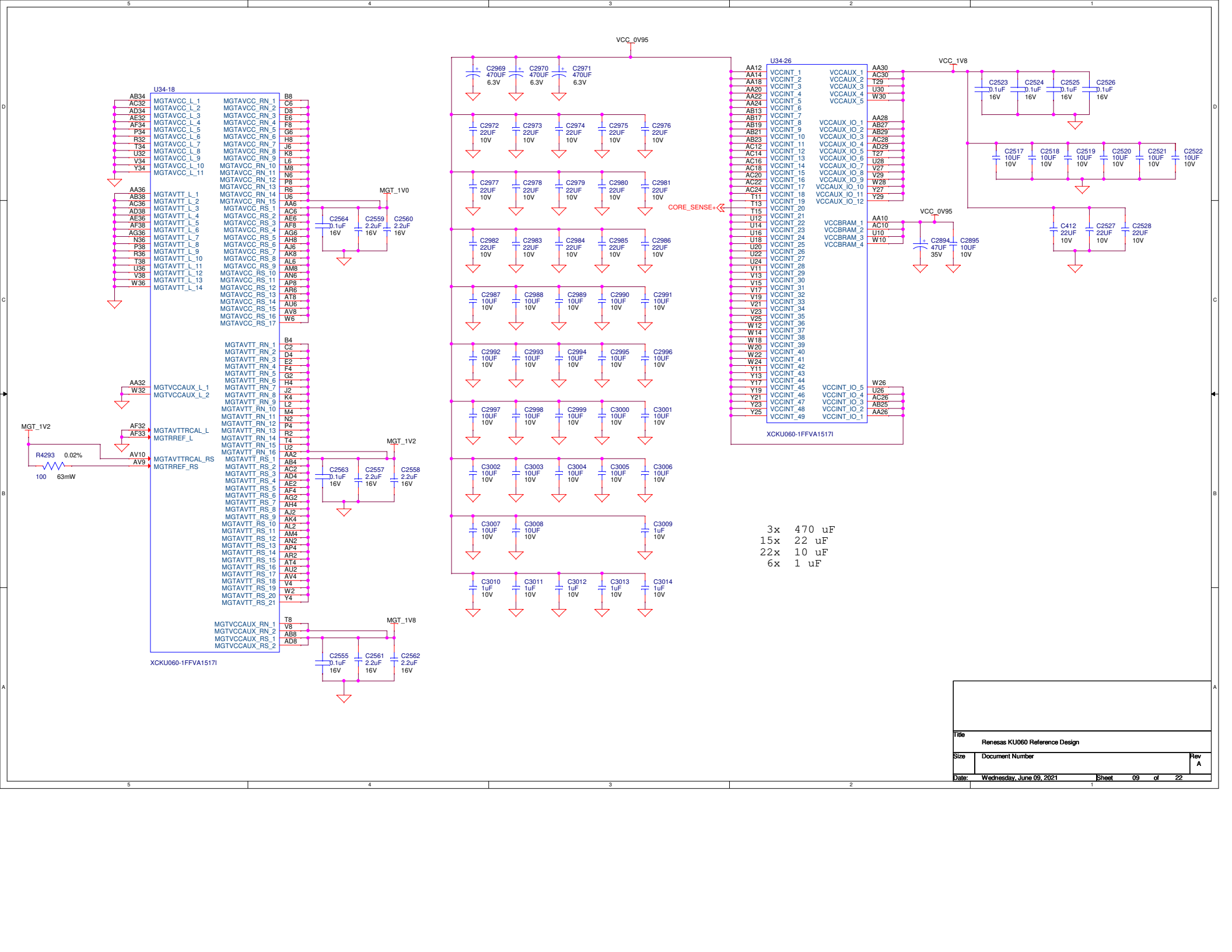
Value (µF)	Case	Type	ESR (mΩ)	ESL (nH)	Sample Part Number
330	D	Tant Poly	5.84	1.90	Kemet T541X337M010ATE
47	D	Tant Poly	15.22	1.90	Kemet T541D476M3.5ATE
10	1210	X7R	20	1.62	
1.0	0805	X7R	19	2.50	
0.22	0603	X7R	12	2.50	

Decoupling methods other than those presented in these tables can be used, but the decoupling network should be designed to meet or exceed the performance of the simple decoupling networks presented here. The impedance of the alternate network is recommended to be less than or equal to that of the recommended network across frequencies from 100 kHz to approximately 10 MHz.

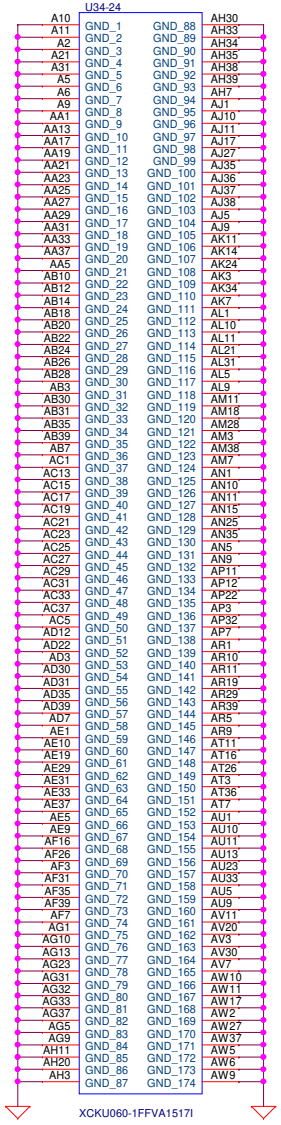
Using KEMET's K-SIM capacitor simulation software we find that the Xilinx design has peak impedance of about 1.5 mOhm over frequency. Iterating in the same tool we derive a network with a similar figure, but fewer components. This reduces the BOM and simplifies PCB layout.

Both designs are under Ztarget = 3mOhm.

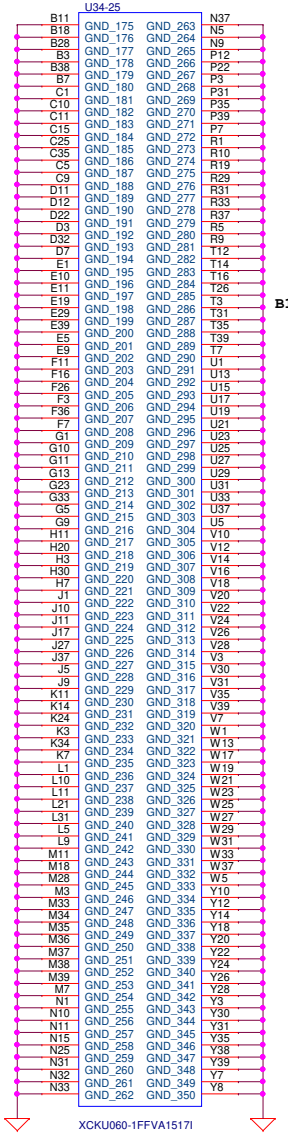
Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date:	Wednesday, June 09, 2021	Sheet 08 of 22


U34-18
XCKU060-1FFVA1517I
MGTAVCC_L_1
MGTAVCC_L_2
MGTAVCC_L_3
MGTAVCC_L_4
MGTAVCC_L_5
MGTAVCC_L_6
MGTAVCC_L_7
MGTAVCC_L_8
MGTAVCC_L_9
MGTAVCC_L_10
MGTAVCC_L_11
MGTAVTT_L_1
MGTAVTT_L_2
MGTAVTT_L_3
MGTAVTT_L_4
MGTAVTT_L_5
MGTAVTT_L_6
MGTAVTT_L_7
MGTAVTT_L_8
MGTAVTT_L_9
MGTAVTT_L_10
MGTAVTT_L_11
MGTAVTT_L_12
MGTAVTT_L_13
MGTAVTT_L_14
MGTVCCAUX_L_1
MGTVCCAUX_L_2
MGTAVTTRCAL_L
MGTRREF_L
MGTAVTTRCAL_RS
MGTRREF_RS
MGTAVCC_RN_1
MGTAVCC_RN_2
MGTAVCC_RN_3
MGTAVCC_RN_4
MGTAVCC_RN_5
MGTAVCC_RN_6
MGTAVCC_RN_7
MGTAVCC_RN_8
MGTAVCC_RN_9
MGTAVCC_RN_10
MGTAVCC_RN_11
MGTAVCC_RN_12
MGTAVCC_RN_13
MGTAVCC_RN_14
MGTAVCC_RN_15
MGTAVCC_RS_1
MGTAVCC_RS_2
MGTAVCC_RS_3
MGTAVCC_RS_4
MGTAVCC_RS_5
MGTAVCC_RS_6
MGTAVCC_RS_7
MGTAVCC_RS_8
MGTAVCC_RS_9
MGTAVCC_RS_10
MGTAVCC_RS_11
MGTAVCC_RS_12
MGTAVCC_RS_13
MGTAVCC_RS_14
MGTAVCC_RS_15
MGTAVCC_RS_16
MGTAVCC_RS_17
MGTAVTT_RN_1
MGTAVTT_RN_2
MGTAVTT_RN_3
MGTAVTT_RN_4
MGTAVTT_RN_5
MGTAVTT_RN_6
MGTAVTT_RN_7
MGTAVTT_RN_8
MGTAVTT_RN_9
MGTAVTT_RN_10
MGTAVTT_RN_11
MGTAVTT_RN_12
MGTAVTT_RN_13
MGTAVTT_RN_14
MGTAVTT_RN_15
MGTAVTT_RN_16
MGTAVTT_RS_1
MGTAVTT_RS_2
MGTAVTT_RS_3
MGTAVTT_RS_4
MGTAVTT_RS_5
MGTAVTT_RS_6
MGTAVTT_RS_7
MGTAVTT_RS_8
MGTAVTT_RS_9
MGTAVTT_RS_10
MGTAVTT_RS_11
MGTAVTT_RS_12
MGTAVTT_RS_13
MGTAVTT_RS_14
MGTAVTT_RS_15
MGTAVTT_RS_16
MGTAVTT_RS_17
MGTAVTT_RS_18
MGTAVTT_RS_19
MGTAVTT_RS_20
MGTAVTT_RS_21
MGTVCCAUX_RN_1
MGTVCCAUX_RN_2
MGTVCCAUX_RS_1
MGTVCCAUX_RS_2
MGT_1V0
MGT_1V2
MGT_1V8
C2564 0.1uF 16V
C2559 2.2uF 16V
C2560 2.2uF 16V
C2563 0.1uF 16V
C2557 2.2uF 16V
C2558 2.2uF 16V
C2555 0.1uF 16V
C2561 2.2uF 16V
C2562 2.2uF 16V
R4293 0.02%
100 63mW
VCC_0V95
C2969 470UF 6.3V
C2970 470UF 6.3V
C2971 470UF 6.3V
C2972 22UF 10V
C2973 22UF 10V
C2974 22UF 10V
C2975 22UF 10V
C2976 22UF 10V
C2977 22UF 10V
C2978 22UF 10V
C2979 22UF 10V
C2980 22UF 10V
C2981 22UF 10V
C2982 22UF 10V
C2983 22UF 10V
C2984 22UF 10V
C2985 22UF 10V
C2986 22UF 10V
C2987 10UF 10V
C2988 10UF 10V
C2989 10UF 10V
C2990 10UF 10V
C2991 10UF 10V
C2992 10UF 10V
C2993 10UF 10V
C2994 10UF 10V
C2995 10UF 10V
C2996 10UF 10V
C2997 10UF 10V
C2998 10UF 10V
C2999 10UF 10V
C3000 10UF 10V
C3001 10UF 10V
C3002 10UF 10V
C3003 10UF 10V
C3004 10UF 10V
C3005 10UF 10V
C3006 10UF 10V
C3007 10UF 10V
C3008 10UF 10V
C3009 1uF 10V
C3010 1uF 10V
C3011 1uF 10V
C3012 1uF 10V
C3013 1uF 10V
C3014 1uF 10V
CORE_SENSE+
U34-26
XCKU060-1FFVA1517I
VCCINT_1
VCCINT_2
VCCINT_3
VCCINT_4
VCCINT_5
VCCINT_6
VCCINT_7
VCCINT_8
VCCINT_9
VCCINT_10
VCCINT_11
VCCINT_12
VCCINT_13
VCCINT_14
VCCINT_15
VCCINT_16
VCCINT_17
VCCINT_18
VCCINT_19
VCCINT_20
VCCINT_21
VCCINT_22
VCCINT_23
VCCINT_24
VCCINT_25
VCCINT_26
VCCINT_27
VCCINT_28
VCCINT_29
VCCINT_30
VCCINT_31
VCCINT_32
VCCINT_33
VCCINT_34
VCCINT_35
VCCINT_36
VCCINT_37
VCCINT_38
VCCINT_39
VCCINT_40
VCCINT_41
VCCINT_42
VCCINT_43
VCCINT_44
VCCINT_45
VCCINT_46
VCCINT_47
VCCINT_48
VCCINT_49
VCCAUX_1
VCCAUX_2
VCCAUX_3
VCCAUX_4
VCCAUX_5
VCCAUX_IO_1
VCCAUX_IO_2
VCCAUX_IO_3
VCCAUX_IO_4
VCCAUX_IO_5
VCCAUX_IO_6
VCCAUX_IO_7
VCCAUX_IO_8
VCCAUX_IO_9
VCCAUX_IO_10
VCCAUX_IO_11
VCCAUX_IO_12
VCCBRAM_1
VCCBRAM_2
VCCBRAM_3
VCCBRAM_4
VCCINT_IO_5
VCCINT_IO_4
VCCINT_IO_3
VCCINT_IO_2
VCCINT_IO_1
VCC_1V8
VCC_0V95
C2523 0.1uF 16V
C2524 0.1uF 16V
C2525 0.1uF 16V
C2526 0.1uF 16V
C2517 10UF 10V
C2518 10UF 10V
C2519 10UF 10V
C2520 10UF 10V
C2521 10UF 10V
C2522 10UF 10V
C412 22UF 10V
C2527 22UF 10V
C2528 22UF 10V
C2894 47UF 35V
C2895 10UF 10V
3x 470 uF
15x 22 uF
22x 10 uF
6x 1 uF
Title
Renesas KU060 Reference Design
Size
Document Number
Rev A
Date: Wednesday, June 09, 2021
Sheet 09 of 22

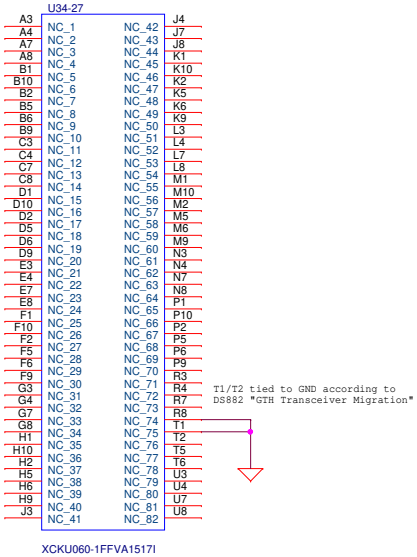
A2 is NC on A1517 (CGA) Pinout



AW2 is NC on A1517 (CGA) Pinout

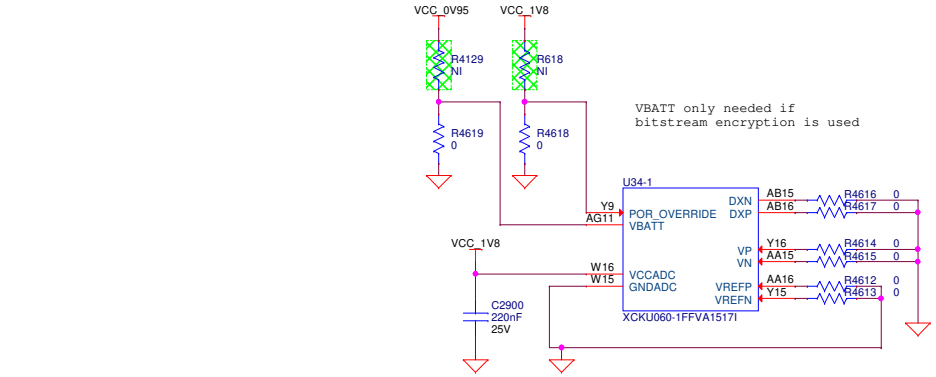


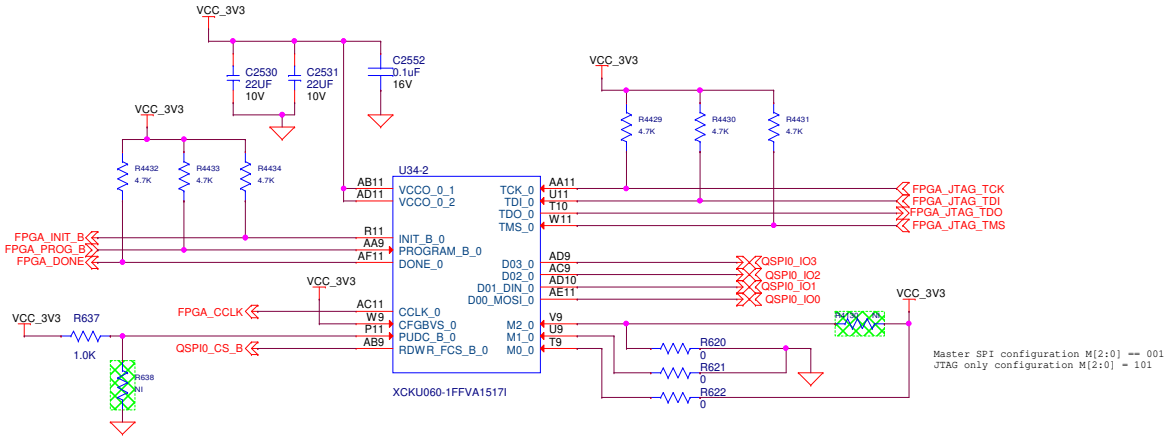
B1 is NC on A1517 (CGA) Pinout



Bank 224 corner transceiver moved to pins T1,T2 on XQRK060 Package

Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 10 of 22	





Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 11 of 22	

HP Voltage = 0.950 V to 1.890 V
Maximum clamp-current per pin = 10mA
Maximum clamp-current per 52-pin bank = 200mA

U34-4

AK39 VCCO_25_1
AL36 VCCO_25_2
AP37 VCCO_25_3
AR34 VCCO_25_4
AU38 VCCO_25_5
AV35 VCCO_25_6
AJ34 VREF_25

IO_L10N_T1U_N7_QBC_AD4N_25 AU39
IO_L10P_T1U_N6_QBC_AD4P_25 AT39
IO_L11N_T1U_N9_GC_25 AT37
IO_L11P_T1U_N8_GC_25 AR37
IO_L12N_T1U_N11_GC_25 AT38
IO_L12P_T1U_N10_GC_25 AR38
IO_L13N_T2L_N1_GC_QBC_25 AR36
IO_L13P_T2L_N0_GC_QBC_25 AP36
IO_L14N_T2L_N3_GC_25 AN37
IO_L14P_T2L_N2_GC_25 AN36
IO_L15N_T2L_N5_AD11N_25 AP34
IO_L15P_T2L_N4_AD11P_25 AN34
IO_L16N_T2U_N7_QBC_AD3N_25 AP38
IO_L16P_T2U_N6_QBC_AD3P_25 AN38
IO_L17N_T2U_N9_AD10N_25 AM35
IO_L17P_T2U_N8_AD10P_25 AM34
IO_L18N_T2U_N11_AD2N_25 AP39
IO_L18P_T2U_N10_AD2P_25 AN39
IO_L19N_T3L_N1_DBC_AD9N_25 AM37
IO_L19P_T3L_N0_DBC_AD9P_25 AM36
IO_L1N_T0L_N1_DBC_25 AW34
IO_L1P_T0L_N0_DBC_25 AW33
IO_L20N_T3L_N3_AD1N_25 AL38
IO_L20P_T3L_N2_AD1P_25 AL37
IO_L21N_T3L_N5_AD8N_25 AL35
IO_L21P_T3L_N4_AD8P_25 AL34
IO_L22N_T3U_N7_DBC_AD0N_25 AK38
IO_L22P_T3U_N6_DBC_AD0P_25 AK37
IO_L23N_T3U_N9_25 AK36
IO_L23P_T3U_N8_25 AK35
IO_L24N_T3U_N11_25 AM39
IO_L24P_T3U_N10_25 AL39
IO_L2N_T0L_N3_25 AV34
IO_L2P_T0L_N2_25 AV33
IO_L3N_T0L_N5_AD15N_25 AU34
IO_L3P_T0L_N4_AD15P_25 AT34
IO_L4N_T0U_N7_DBC_AD7N_25 AW36
IO_L4P_T0U_N6_DBC_AD7P_25 AW35
IO_L5N_T0U_N9_AD14N_25 AT33
IO_L5P_T0U_N8_AD14P_25 AR33
IO_L6N_T0U_N11_AD6N_25 AU35
IO_L6P_T0U_N10_AD6P_25 AT35
IO_L7N_T1L_N1_QBC_AD13N_25 AV36
IO_L7P_T1L_N0_QBC_AD13P_25 AU36
IO_L8N_T1L_N3_AD5N_25 AV39
IO_L8P_T1L_N2_AD5P_25 AV38
IO_L9N_T1L_N5_AD12N_25 AV37
IO_L9P_T1L_N4_AD12P_25 AU37
IO_T0U_N12_VRP_25 AR35
IO_T1U_N12_25 AW38
IO_T2U_N12_25 AP35
IO_T3U_N12_25 AJ39

HP
XCKU060-1FFVA1517I

AR# 72582 Space-Grade XQRKU060 will prohibit you from placing memory (DDR) interfaces in bank 25 and/or bank 46 due to corner pads not being bonded out to package

AV39 is NC on CA1509 (CGA) Pinout
AV38 NC by association
AW38 is NC on CA1509 (CGA) Pinout

U34-6

AD27 VCCO_45_1
AE24 VCCO_45_2
AH25 VCCO_45_3
AL26 VCCO_45_4
AP27 VCCO_45_5
AU28 VCCO_45_6
AV25 VCCO_45_7
AD24 VREF_45

IO_L10N_T1U_N7_QBC_AD4N_45 AR25
IO_L10P_T1U_N6_QBC_AD4P_45 AP25
IO_L11N_T1U_N9_GC_45 AN27
IO_L11P_T1U_N8_GC_45 AM27
IO_L12N_T1U_N11_GC_45 AN26
IO_L12P_T1U_N10_GC_45 AM26
IO_L13N_T2L_N1_GC_QBC_45 AK28
IO_L13P_T2L_N0_GC_QBC_45 AK27
IO_L14N_T2L_N3_GC_45 AL28
IO_L14P_T2L_N2_GC_45 AL27
IO_L15N_T2L_N5_AD11N_45 AK25
IO_L15P_T2L_N4_AD11P_45 AJ25
IO_L16N_T2U_N7_QBC_AD3N_45 AL25
IO_L16P_T2U_N6_QBC_AD3P_45 AL24
IO_L17N_T2U_N9_AD10N_45 AJ26
IO_L17P_T2U_N8_AD10P_45 AH26
IO_L18N_T2U_N11_AD2N_45 AJ24
IO_L18P_T2U_N10_AD2P_45 AH24
IO_L19N_T3L_N1_DBC_AD9N_45 AE25
IO_L19P_T3L_N0_DBC_AD9P_45 AD25
IO_L1N_T0L_N1_DBC_45 AW28
IO_L1P_T0L_N0_DBC_45 AV28
IO_L20N_T3L_N3_AD1N_45 AG25
IO_L20P_T3L_N2_AD1P_45 AF25
IO_L21N_T3L_N5_AD8N_45 AE26
IO_L21P_T3L_N4_AD8P_45 AD26
IO_L22N_T3U_N7_DBC_AD0N_45 AG24
IO_L22P_T3U_N6_DBC_AD0P_45 AF24
IO_L23N_T3U_N9_45 AF27
IO_L23P_T3U_N8_45 AE27
IO_L24N_T3U_N11_45 AG27
IO_L24P_T3U_N10_45 AG26
IO_L2N_T0L_N3_45 AW26
IO_L2P_T0L_N2_45 AW25
IO_L3N_T0L_N5_AD15N_45 AU27
IO_L3P_T0L_N4_AD15P_45 AT27
IO_L4N_T0U_N7_DBC_AD7N_45 AU26
IO_L4P_T0U_N6_DBC_AD7P_45 AU25
IO_L5N_T0U_N9_AD14N_45 AT28
IO_L5P_T0U_N8_AD14P_45 AR28
IO_L6N_T0U_N11_AD6N_45 AV27
IO_L6P_T0U_N10_AD6P_45 AV26
IO_L7N_T1L_N1_QBC_AD13N_45 AR27
IO_L7P_T1L_N0_QBC_AD13P_45 AR26
IO_L8N_T1L_N3_AD5N_45 AM25
IO_L8P_T1L_N2_AD5P_45 AM24
IO_L9N_T1L_N5_AD12N_45 AP28
IO_L9P_T1L_N4_AD12P_45 AN28
IO_T0U_N12_VRP_45 AT25
IO_T1U_N12_45 AP26
IO_T2U_N12_45 AK26
IO_T3U_N12_45 AH27

HP
XCKU060-1FFVA1517I

U34-3

AG28 VCCO_24_1
AJ32 VCCO_24_2
AK29 VCCO_24_3
AM33 VCCO_24_4
AN30 VCCO_24_5
AT31 VCCO_24_6
AW32 VCCO_24_7
AD28 VREF_24

IO_L10N_T1U_N7_QBC_AD4N_24 AR30
IO_L10P_T1U_N6_QBC_AD4P_24 AP29
IO_L11N_T1U_N9_GC_24 AN32
IO_L11P_T1U_N8_GC_24 AN31
IO_L12N_T1U_N11_GC_24 AM31
IO_L12P_T1U_N10_GC_24 AM30
IO_L13N_T2L_N1_GC_QBC_24 AL30
IO_L13P_T2L_N0_GC_QBC_24 AM29
IO_L14N_T2L_N3_GC_24 AL29
IO_L14P_T2L_N2_GC_24 AK30
IO_L15N_T2L_N5_AD11N_24 AJ30
IO_L15P_T2L_N4_AD11P_24 AL32
IO_L16N_T2U_N7_QBC_AD3N_24 AK32
IO_L16P_T2U_N6_QBC_AD3P_24 AK31
IO_L17N_T2U_N9_AD10N_24 AJ31
IO_L17P_T2U_N8_AD10P_24 AK33
IO_L18N_T2U_N11_AD2N_24 AJ33
IO_L18P_T2U_N10_AD2P_24 AJ29
IO_L19N_T3L_N1_DBC_AD9N_24 AH29
IO_L19P_T3L_N0_DBC_AD9P_24 AV32
IO_L1N_T0L_N1_DBC_24 AU32
IO_L1P_T0L_N0_DBC_24 AH32
IO_L20N_T3L_N3_AD1N_24 AH31
IO_L20P_T3L_N2_AD1P_24 AF30
IO_L21N_T3L_N5_AD8N_24 AE30
IO_L21P_T3L_N4_AD8P_24 AJ28
IO_L22N_T3U_N7_DBC_AD0N_24 AH28
IO_L22P_T3U_N6_DBC_AD0P_24 AG29
IO_L23N_T3U_N9_24 AF29
IO_L23P_T3U_N8_24 AF28
IO_L24N_T3U_N11_24 AE28
IO_L24P_T3U_N10_24 AW29
IO_L2N_T0L_N3_24 AV29
IO_L2P_T0L_N2_24 AW31
IO_L3N_T0L_N5_AD15N_24 AW30
IO_L3P_T0L_N4_AD15P_24 AU30
IO_L4N_T0U_N7_DBC_AD7N_24 AU29
IO_L4P_T0U_N6_DBC_AD7P_24 AV31
IO_L5N_T0U_N9_AD14N_24 AU31
IO_L5P_T0U_N8_AD14P_24 AT30
IO_L6N_T0U_N11_AD6N_24 AT29
IO_L6P_T0U_N10_AD6P_24 AP33
IO_L7N_T1L_N1_QBC_AD13N_24 AN33
IO_L7P_T1L_N0_QBC_AD13P_24 AP31
IO_L8N_T1L_N3_AD5N_24 AP30
IO_L8P_T1L_N2_AD5P_24 AR32
IO_L9N_T1L_N5_AD12N_24 AR31
IO_L9P_T1L_N4_AD12P_24 AT32
IO_T0U_N12_VRP_24 AN29
IO_T1U_N12_24 AL33
IO_T2U_N12_24 AG30
IO_T3U_N12_24

HP
XCKU060-1FFVA1517I

VCC_1V8

C2600 0.1uF 16V
C2599 0.1uF 16V
C2597 22UF 10V
C2598 22UF 10V

AD23
R4464 1.0K

HSTL_DIFF and LVDS do not have input vref requirements

In banks where the I/O standard does not have an input reference voltage requirement, connect the dedicated VREF pin to GND (with a 500 or 1k resistor), or leave it floating.

VCC_1V8

R4471 1.0K
R4472 1.0K
SGMIICLK_P
C2603 0.1uF 16V SGMIICLK_C_P
SGMIICLK_N
C2604 0.1uF 16V SGMIICLK_C_N
R4473 1.0K
R4474 1.0K

U34-5

AF21 VCCO_44_1
AJ22 VCCO_44_2
AM23 VCCO_44_3
AN20 VCCO_44_4
AR24 VCCO_44_5
AT21 VCCO_44_6
AW22 VCCO_44_7
AD23 VREF_44

IO_L10N_T1U_N7_QBC_AD4N_44 AR21
IO_L10P_T1U_N6_QBC_AD4P_44 AP21
IO_L11N_T1U_N9_GC_44 AN22
IO_L11P_T1U_N8_GC_44 AM22
IO_L12N_T1U_N11_GC_44 AN21
IO_L12P_T1U_N10_GC_44 AM21
IO_L13N_T2L_N1_GC_QBC_44 AL23
IO_L13P_T2L_N0_GC_QBC_44 AK23
IO_L14N_T2L_N3_GC_44 AL22
IO_L14P_T2L_N2_GC_44 AK22
IO_L15N_T2L_N5_AD11N_44 AM20
IO_L15P_T2L_N4_AD11P_44 AL20
IO_L16N_T2U_N7_QBC_AD3N_44 AJ21
IO_L16P_T2U_N6_QBC_AD3P_44 AJ20
IO_L17N_T2U_N9_AD10N_44 AK21
IO_L17P_T2U_N8_AD10P_44 AK20
IO_L18N_T2U_N11_AD2N_44 AH23
IO_L18P_T2U_N10_AD2P_44 AH22
IO_L19N_T3L_N1_DBC_AD9N_44 AG22
IO_L19P_T3L_N0_DBC_AD9P_44 AG21
IO_L1N_T0L_N1_DBC_44 AW24
IO_L1P_T0L_N0_DBC_44 AV24
IO_L20N_T3L_N3_AD1N_44 AG20
IO_L20P_T3L_N2_AD1P_44 AF20
IO_L21N_T3L_N5_AD8N_44 AF22
IO_L21P_T3L_N4_AD8P_44 AE22
IO_L22N_T3U_N7_DBC_AD0N_44 AE21
IO_L22P_T3U_N6_DBC_AD0P_44 AE20
IO_L23N_T3U_N9_44 AF23
IO_L23P_T3U_N8_44 AE23
IO_L24N_T3U_N11_44 AD21
IO_L24P_T3U_N10_44 AD20
IO_L2N_T0L_N3_44 AW21
IO_L2P_T0L_N2_44 AV21
IO_L3N_T0L_N5_AD15N_44 AW23
IO_L3P_T0L_N4_AD15P_44 AV23
IO_L4N_T0U_N7_DBC_AD7N_44 AV22
IO_L4P_T0U_N6_DBC_AD7P_44 AU21
IO_L5N_T0U_N9_AD14N_44 AT24
IO_L5P_T0U_N8_AD14P_44 AT23
IO_L6N_T0U_N11_AD6N_44 AU22
IO_L6P_T0U_N10_AD6P_44 AT22
IO_L7N_T1L_N1_QBC_AD13N_44 AP24
IO_L7P_T1L_N0_QBC_AD13P_44 AN24
IO_L8N_T1L_N3_AD5N_44 AR23
IO_L8P_T1L_N2_AD5P_44 AR22
IO_L9N_T1L_N5_AD12N_44 AP23
IO_L9P_T1L_N4_AD12P_44 AN23
IO_T0U_N12_VRP_44 AU24
IO_T1U_N12_44 AP20
IO_T2U_N12_44 AJ23
IO_T3U_N12_44 AH21

HP
XCKU060-1FFVA1517I

We put these signals in the HP bank because the vivado design file listed the SGMII_TX and SGMII_RX signals as HSTL logic I/O (HSTL is not available in 2.5V banks, so it requires different VCCO from the GMII signals)

SGMII_TX_N
SGMII_TX_P
SGMIICLK_N
SGMIICLK_P
SGMII_RX_N
SGMII_RX_P

Place resistors as close to pins of FPGA as possible

SGMIICLK_P
R4465 100 63mW 0.02%
SGMIICLK_N
SGMII_RX_P
R4466 100 63mW 0.02%
SGMII_RX_N

VRP_44
R4463 240

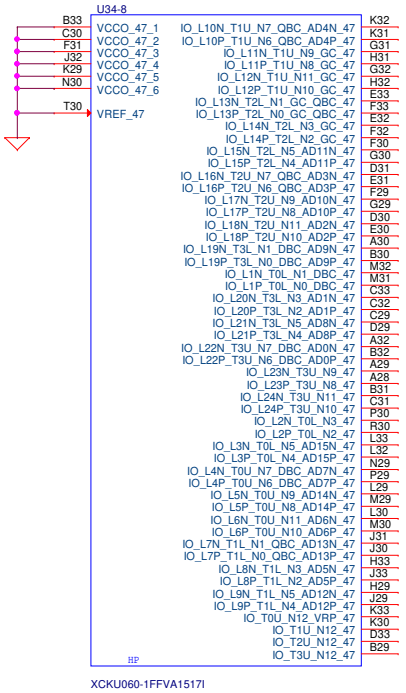
VCC_1V8

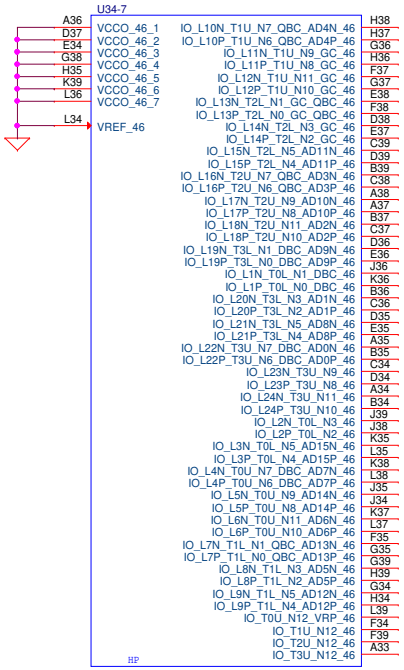
R4467 1.0K
R4468 1.0K
SGMII_RX_P
C2601 0.1uF 16V SGMII_RX_C_P
SGMII_RX_N
C2602 0.1uF 16V SGMII_RX_C_N
R4469 1.0K
R4470 1.0K

Levelshifting to adjust 1.4V common-mode to 0.9V common-mode of 1.8V DIFF_HSTL_I_18 and LVDS

Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 12 of 22	

HP Voltage = 0.950 V to 1.890 V
Maximum clamp-current per pin = 10mA
Maximum clamp-current per 52-pin bank = 200mA

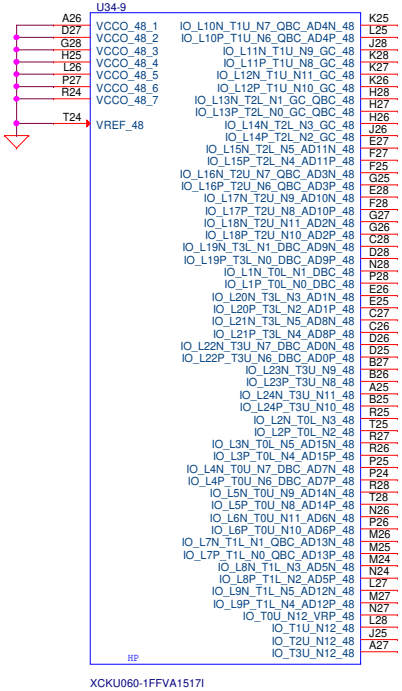




B39 is NC on CA1509 (CGA) Pinout
C38 NC by association

A38 is NC on A1509 (CGA) Pinout
A37 NC by association

AR# 72582 Space-Grade XQRKU060 will prohibit you from placing memory (DDR) interfaces in bank 25 and/or bank 46 Due to corner-pads not being bonded out to package



Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 13 of 22	

HP Voltage = 0.950 V to 1.890 V
Maximum clamp-current per pin = 10mA
Maximum clamp-current per 52-pin bank = 200mA

Max memory interfaces speed is 1600Mb/s according to table 26 in DS892 (-1L speed grade, 0.95V core, FF package)

U34-11 — XCKU060-1FFVA1517I

U34-10 — XCKU060-1FFVA1517I

U34-12 — XCKU060-1FFVA1517I

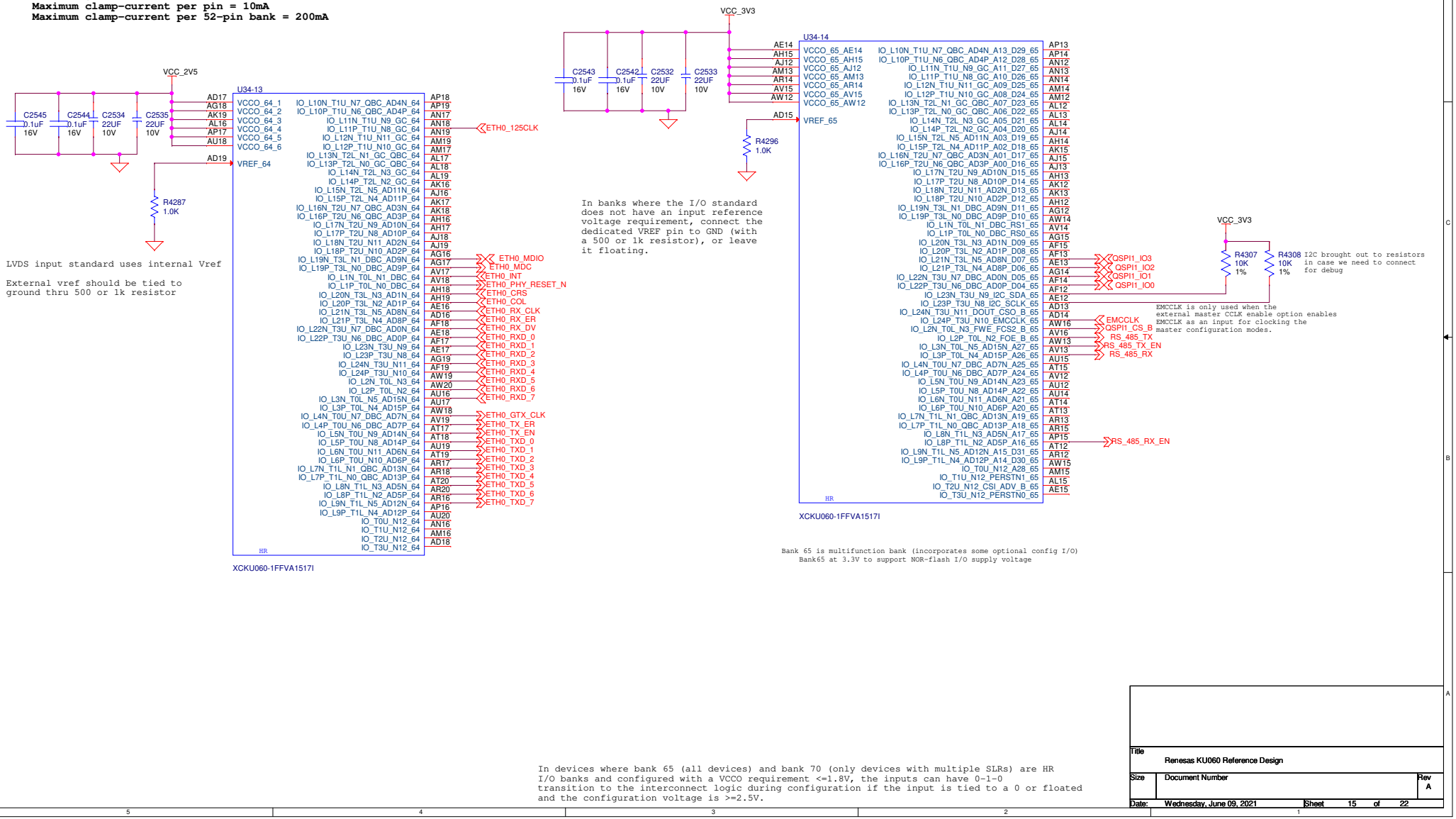
Place termination near pins of FPGA

VRP to 240 ohm 1% resistor

DQS_BIAS would place common-mode at 0.675V

Title	Renesas KU060 Reference Design
Size	Document Number — Rev A
Date:	Wednesday, June 09, 2021 — Sheet 14 of 22

HR Voltage = 1.140 V to 3.400 V
Maximum clamp-current per pin = 10mA
Maximum clamp-current per 52-pin bank = 200mA



LVDS input standard uses internal Vref

External vref should be tied to ground thru 500 or 1k resistor

In banks where the I/O standard does not have an input reference voltage requirement, connect the dedicated VREF pin to GND (with a 500 or 1k resistor), or leave it floating.

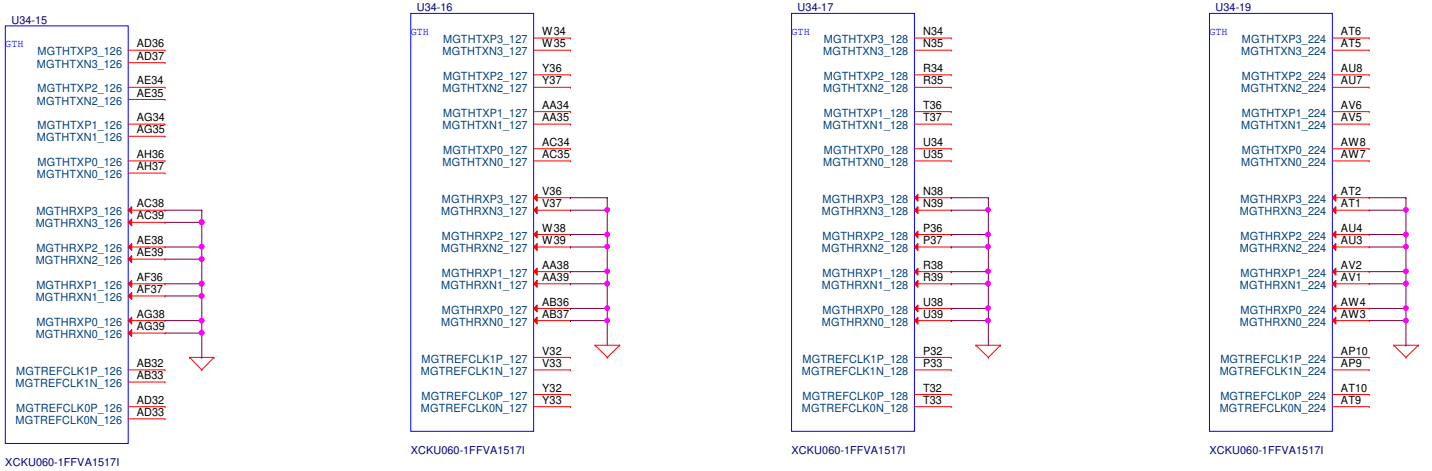
I2C brought out to resistors in case we need to connect for debug

EMCCLK is only used when the external master CCLK enable option enables EMCCLK as an input for clocking the master configuration modes.

Bank 65 is multifunction bank (incorporates some optional config I/O)
Bank65 at 3.3V to support NOR-flash I/O supply voltage

In devices where bank 65 (all devices) and bank 70 (only devices with multiple SLRs) are HR I/O banks and configured with a VCCO requirement <=1.8V, the inputs can have 0-1-0 transition to the interconnect logic during configuration if the input is tied to a 0 or floated and the configuration voltage is >=2.5V.

Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 15 of 22	


U34-15
GTH
MGTHTXP3_126
MGTHTXN3_126
MGTHTXP2_126
MGTHTXN2_126
MGTHTXP1_126
MGTHTXN1_126
MGTHTXP0_126
MGTHTXN0_126
MGTHRXP3_126
MGTHRXN3_126
MGTHRXP2_126
MGTHRXN2_126
MGTHRXP1_126
MGTHRXN1_126
MGTHRXP0_126
MGTHRXN0_126
MGTREFCLK1P_126
MGTREFCLK1N_126
MGTREFCLK0P_126
MGTREFCLK0N_126
AD36
AD37
AE34
AE35
AG34
AG35
AH36
AH37
AC38
AC39
AE38
AE39
AF36
AF37
AG38
AG39
AB32
AB33
AD32
AD33
XCKU060-1FFVA1517I
U34-16
GTH
MGTHTXP3_127
MGTHTXN3_127
MGTHTXP2_127
MGTHTXN2_127
MGTHTXP1_127
MGTHTXN1_127
MGTHTXP0_127
MGTHTXN0_127
MGTHRXP3_127
MGTHRXN3_127
MGTHRXP2_127
MGTHRXN2_127
MGTHRXP1_127
MGTHRXN1_127
MGTHRXP0_127
MGTHRXN0_127
MGTREFCLK1P_127
MGTREFCLK1N_127
MGTREFCLK0P_127
MGTREFCLK0N_127
W34
W35
Y36
Y37
AA34
AA35
AC34
AC35
V36
V37
W38
W39
AA38
AA39
AB36
AB37
V32
V33
Y32
Y33
XCKU060-1FFVA1517I
U34-17
GTH
MGTHTXP3_128
MGTHTXN3_128
MGTHTXP2_128
MGTHTXN2_128
MGTHTXP1_128
MGTHTXN1_128
MGTHTXP0_128
MGTHTXN0_128
MGTHRXP3_128
MGTHRXN3_128
MGTHRXP2_128
MGTHRXN2_128
MGTHRXP1_128
MGTHRXN1_128
MGTHRXP0_128
MGTHRXN0_128
MGTREFCLK1P_128
MGTREFCLK1N_128
MGTREFCLK0P_128
MGTREFCLK0N_128
N34
N35
R34
R35
T36
T37
U34
U35
N38
N39
P36
P37
R38
R39
U38
U39
P32
P33
T32
T33
XCKU060-1FFVA1517I
U34-19
GTH
MGTHTXP3_224
MGTHTXN3_224
MGTHTXP2_224
MGTHTXN2_224
MGTHTXP1_224
MGTHTXN1_224
MGTHTXP0_224
MGTHTXN0_224
MGTHRXP3_224
MGTHRXN3_224
MGTHRXP2_224
MGTHRXN2_224
MGTHRXP1_224
MGTHRXN1_224
MGTHRXP0_224
MGTHRXN0_224
MGTREFCLK1P_224
MGTREFCLK1N_224
MGTREFCLK0P_224
MGTREFCLK0N_224
AT6
AT5
AU8
AU7
AV6
AV5
AW8
AW7
AT2
AT1
AU4
AU3
AV2
AV1
AW4
AW3
AP10
AP9
AT10
AT9
XCKU060-1FFVA1517I
U34-20
GTH
MGTHTXP3_225
MGTHTXN3_225
MGTHTXP2_225
MGTHTXN2_225
MGTHTXP1_225
MGTHTXN1_225
MGTHTXP0_225
MGTHTXN0_225
MGTHRXP3_225
MGTHRXN3_225
MGTHRXP2_225
MGTHRXN2_225
MGTHRXP1_225
MGTHRXN1_225
MGTHRXP0_225
MGTHRXN0_225
MGTREFCLK1P_225
MGTREFCLK1N_225
MGTREFCLK0P_225
MGTREFCLK0N_225
AM6
AM5
AN8
AN7
AP6
AP5
AR8
AR7
AM2
AM1
AN4
AN3
AP2
AP1
AR4
AR3
AK10
AK9
AM10
AM9
XCKU060-1FFVA1517I
U34-21
GTH
MGTHTXP3_226
MGTHTXN3_226
MGTHTXP2_226
MGTHTXN2_226
MGTHTXP1_226
MGTHTXN1_226
MGTHTXP0_226
MGTHTXN0_226
MGTHRXP3_226
MGTHRXN3_226
MGTHRXP2_226
MGTHRXN2_226
MGTHRXP1_226
MGTHRXN1_226
MGTHRXP0_226
MGTHRXN0_226
MGTREFCLK1P_226
MGTREFCLK1N_226
MGTREFCLK0P_226
MGTREFCLK0N_226
AH6
AH5
AJ8
AJ7
AK6
AK5
AL8
AL7
AH2
AH1
AJ4
AJ3
AK2
AK1
AL4
AL3
AF10
AF9
AH10
AH9
XCKU060-1FFVA1517I
U34-22
GTH
MGTHTXP3_227
MGTHTXN3_227
MGTHTXP2_227
MGTHTXN2_227
MGTHTXP1_227
MGTHTXN1_227
MGTHTXP0_227
MGTHTXN0_227
MGTHRXP3_227
MGTHRXN3_227
MGTHRXP2_227
MGTHRXN2_227
MGTHRXP1_227
MGTHRXN1_227
MGTHRXP0_227
MGTHRXN0_227
MGTREFCLK1P_227
MGTREFCLK1N_227
MGTREFCLK0P_227
MGTREFCLK0N_227
AD6
AD5
AE4
AE3
AF6
AF5
AG8
AG7
AC4
AC3
AD2
AD1
AF2
AF1
AG4
AG3
AC8
AC7
AE8
AE7
XCKU060-1FFVA1517I
U34-23
GTH
MGTHTXP3_228
MGTHTXN3_228
MGTHTXP2_228
MGTHTXN2_228
MGTHTXP1_228
MGTHTXN1_228
MGTHTXP0_228
MGTHTXN0_228
MGTHRXP3_228
MGTHRXN3_228
MGTHRXP2_228
MGTHRXN2_228
MGTHRXP1_228
MGTHRXN1_228
MGTHRXP0_228
MGTHRXN0_228
MGTREFCLK1P_228
MGTREFCLK1N_228
MGTREFCLK0P_228
MGTREFCLK0N_228
V6
V5
Y6
Y5
AA4
AA3
AB6
AB5
V2
V1
W4
W3
Y2
Y1
AB2
AB1
W8
W7
AA8
AA7
XCKU060-1FFVA1517I
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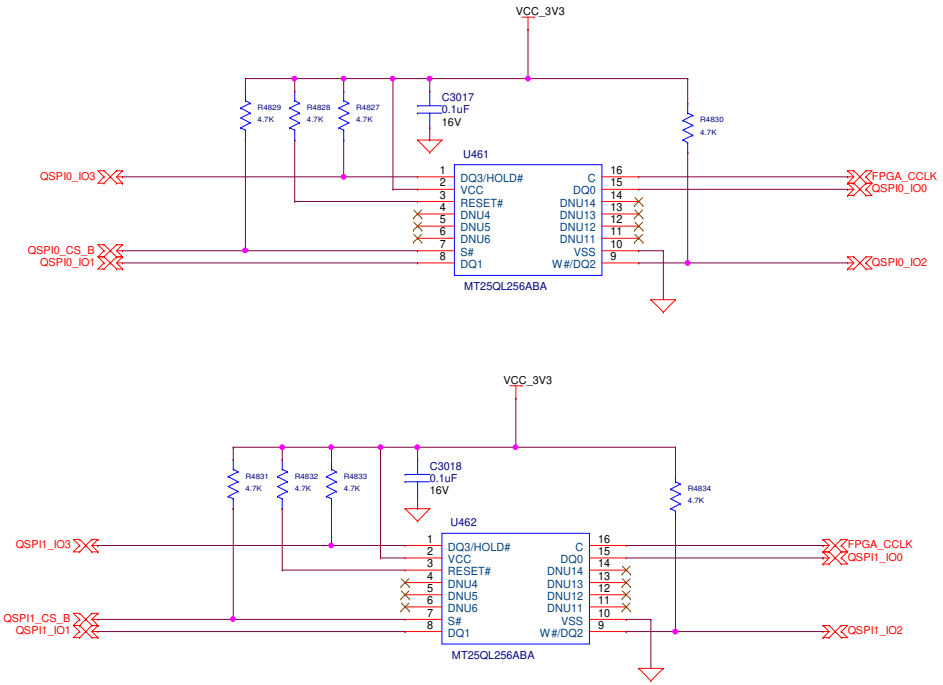
Renesas KU060 Reference Design
Size
Document Number
Rev
A
Date:
Wednesday, June 09, 2021
Sheet
16
of
22



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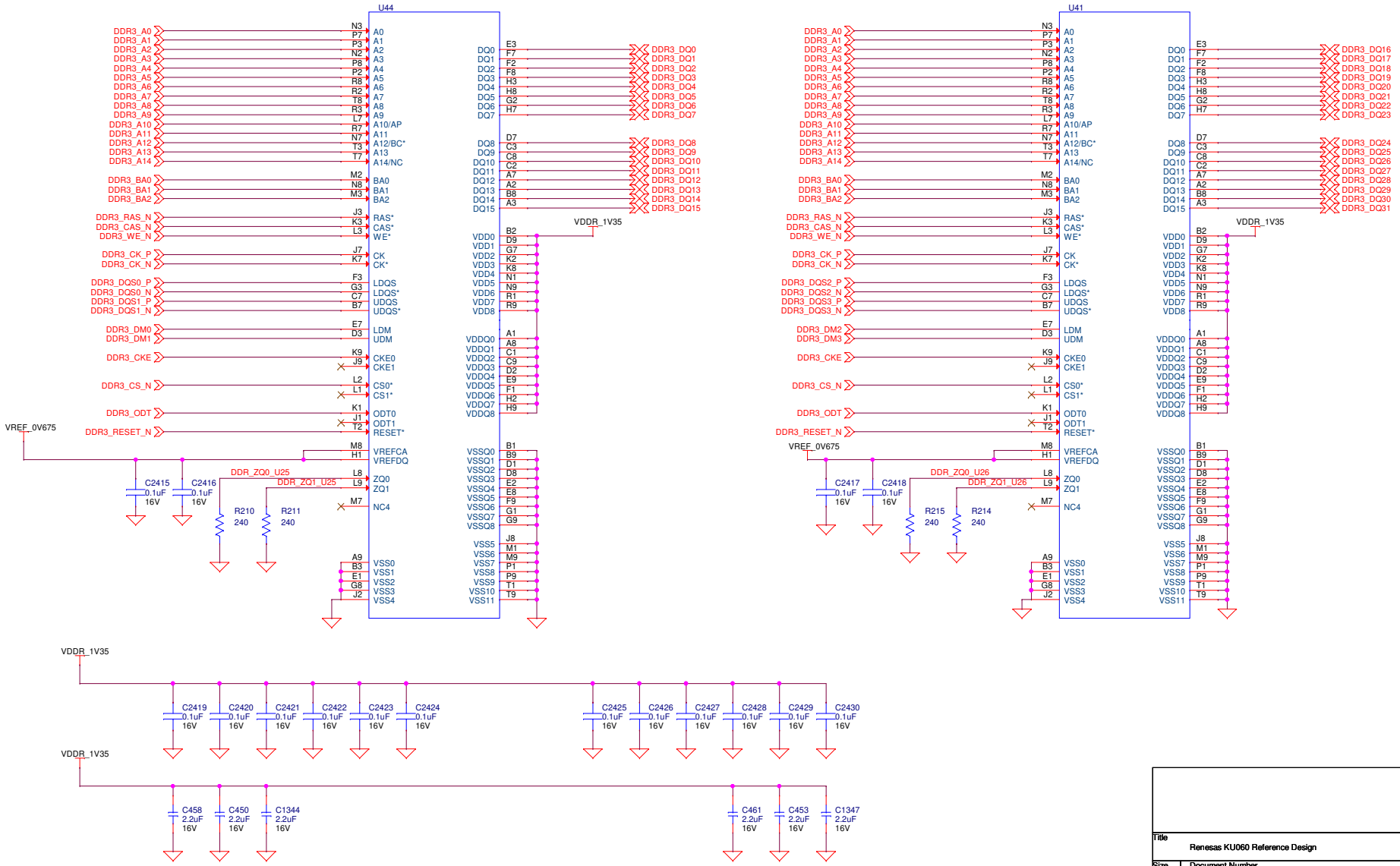
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 17 of 22	



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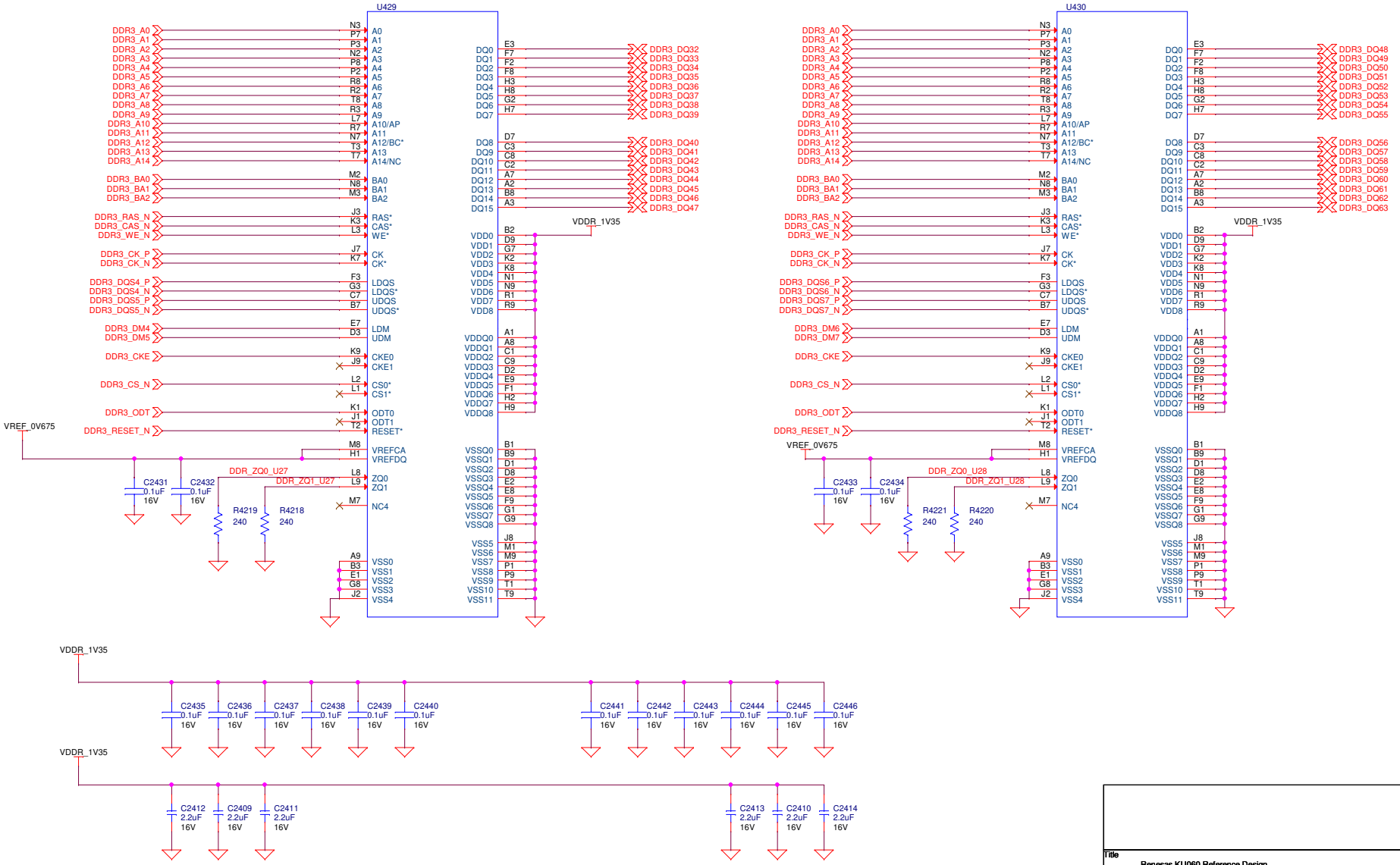
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 18 of 22	



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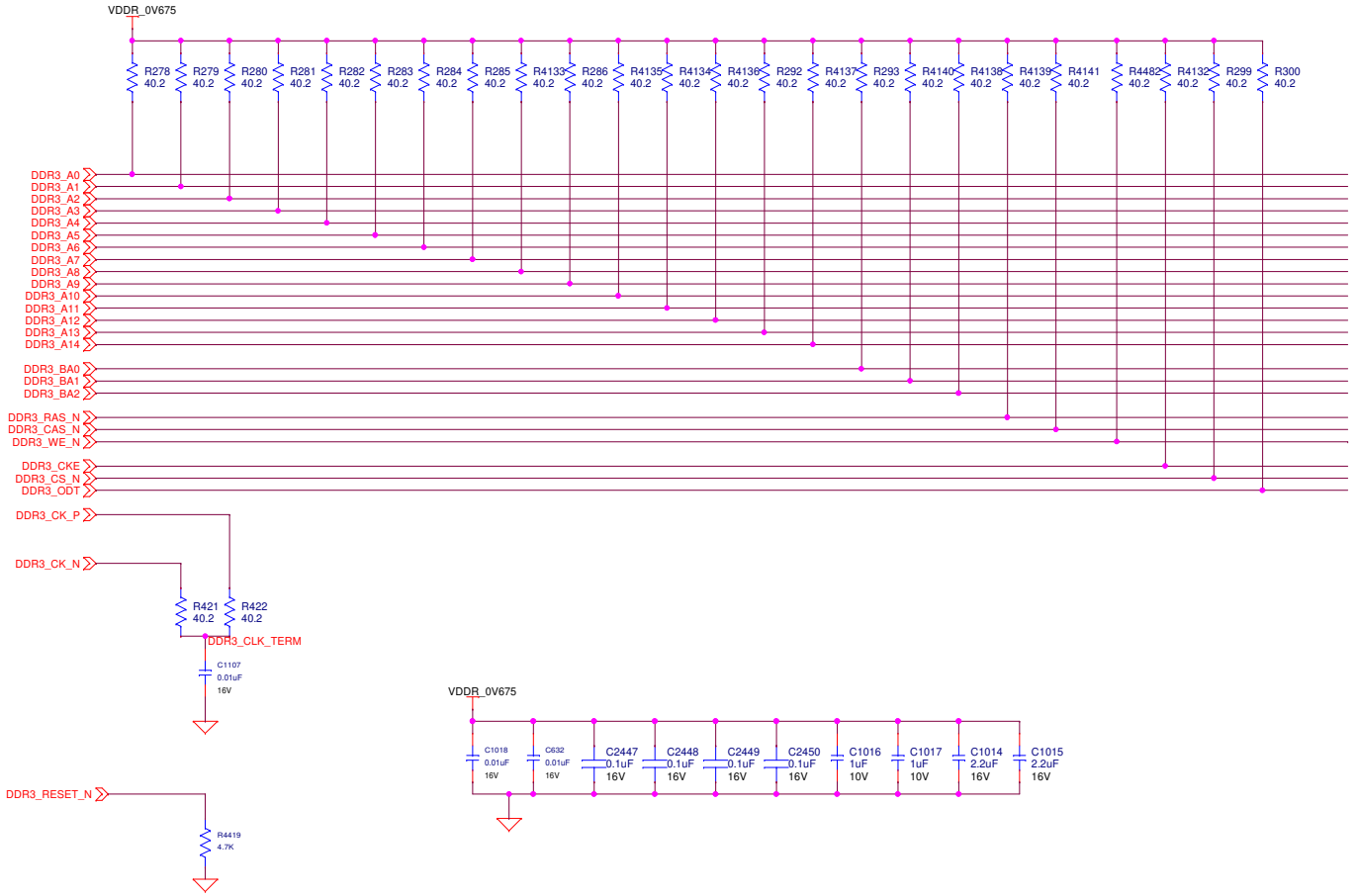
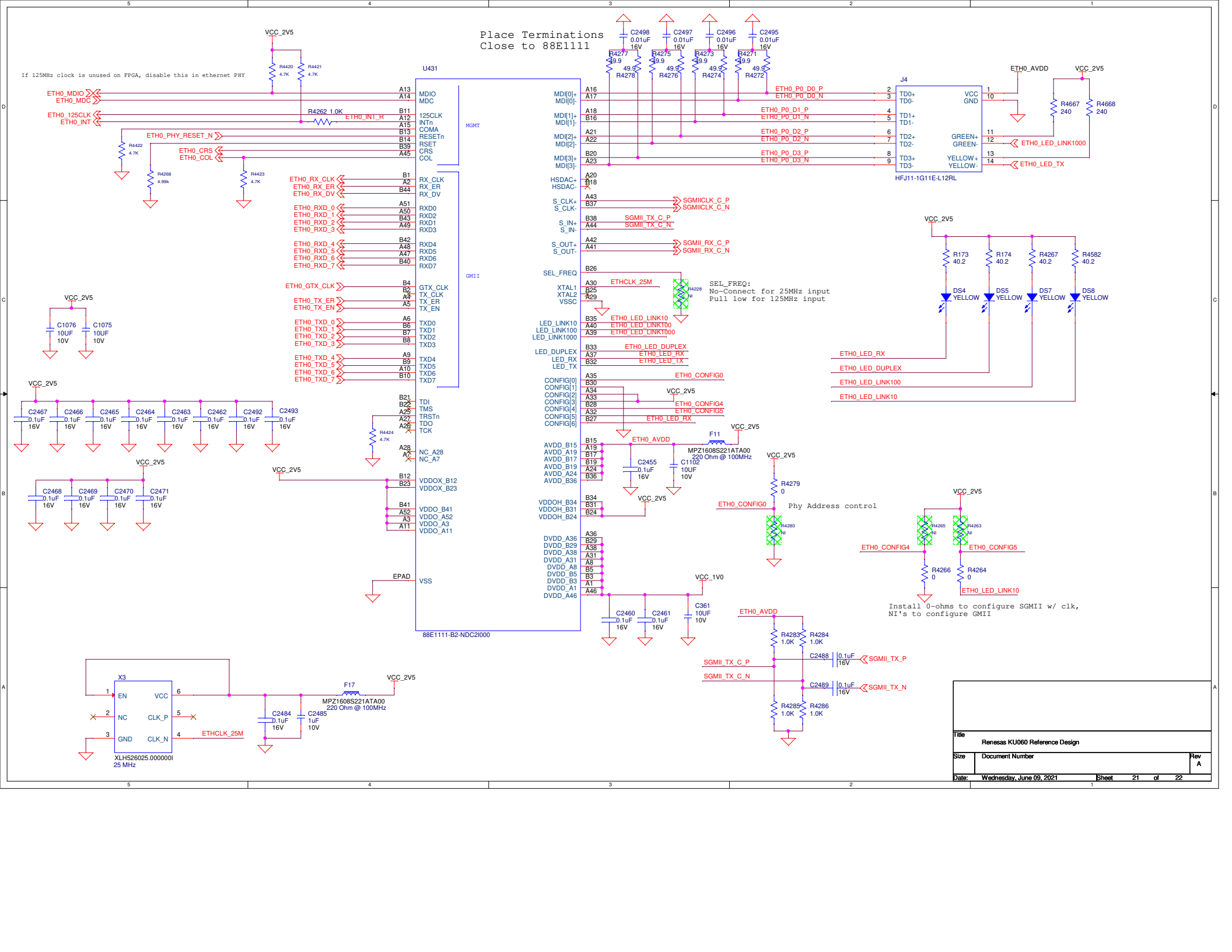
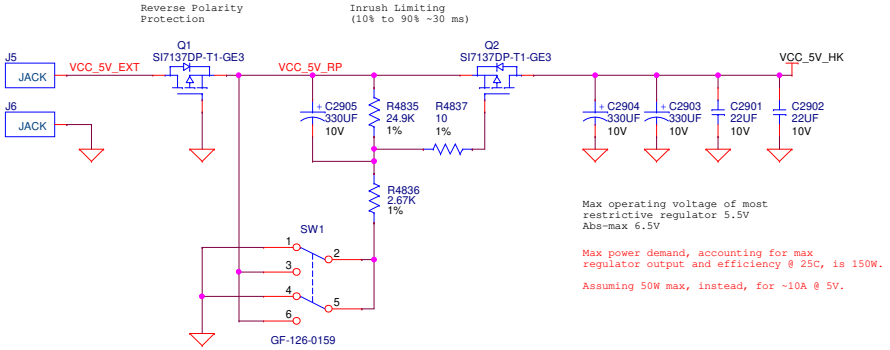
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 19 of 22	



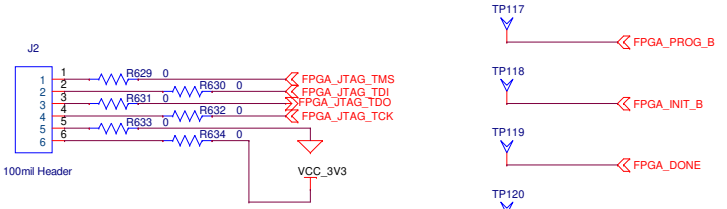
Title	Renesas KU060 Reference Design	
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 20 of 22	

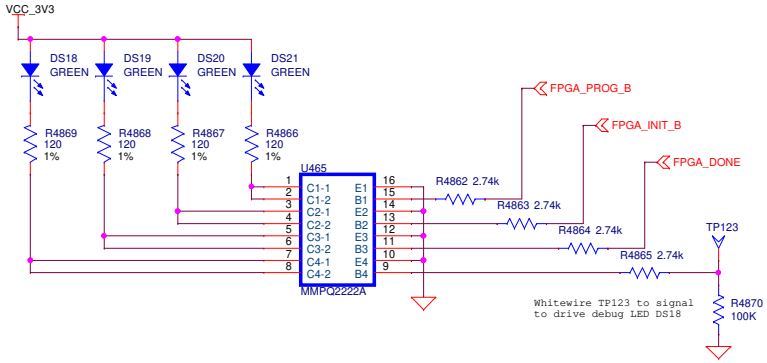

Place Terminations
Close to 88E1111
If 125MHz clock is unused on FPGA, disable this in ethernet PHY
U431
88E1111-B2-NDC2I000
MGMT
GMII
SEL_FREQ:
No-Connect for 25MHz input
Pull low for 125MHz input
Phy Address control
Install 0-ohms to configure SGMII w/ clk,
NI's to configure GMII
HFJ11-1G11E-L12RL
XLH526025.000000I
25 MHz
MPZ1608S221ATA00
220 Ohm @ 100MHz
Title
Renesas KU060 Reference Design
Size
Document Number
Rev
A
Date: Wednesday, June 09, 2021
Sheet 21 of 22

5V Power Input

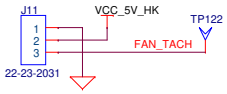


JTAG and FPGA Configuration

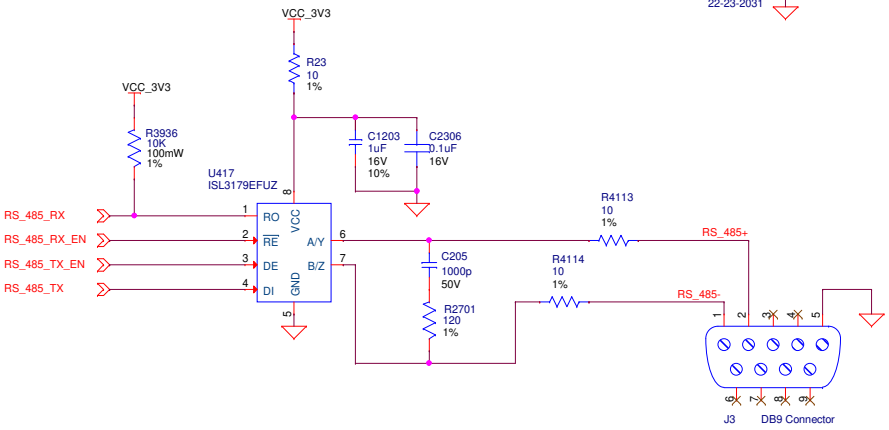


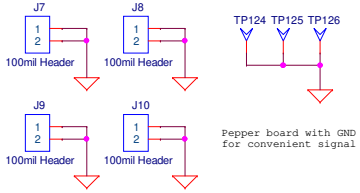


FPGA Fan



RS-485





Pepper board with GND test points for convenient signal probing

Title: Renesas KU060 Reference Design		
Size	Document Number	Rev A
Date: Wednesday, June 09, 2021	Sheet 22 of 22	