ISL73148SEH

Introduction

The intense proton and heavy-ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues such as disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the ISL73148SEH product. The ISL73148SEH is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

SEE Summary

The ISL73148SEH proved to be free of Destructive Single Event Effects (DSEE) including SEL at supply voltages up to AV_{CC} = 6.4V, DV_{CC} = 4.6V, and V_{REF} = 3.6V with a die temperature of 125°C when irradiated with normal incidence gold for a Linear Energy Transfer (LET) of 86MeV·cm^2/mg. **Note:** These voltages are above the operating condition maximum values to provide an additional margin for end applications.

The ISL73148SEH exhibited SET that primarily lasted for a single sample and recovered to normal operation thereafter without any user intervention required indicating the device had no SEFI. The number and magnitude of SET decreased as the LET decreased. No observed SET lasted for longer than two samples and out of all the observed SET during testing, 99.98% were single sample events and 81.92% were less than 100 codes in magnitude. Out of the total number of samples observed during testing, 0.0021% of samples exhibited a SET.

SEE testing was performed on two different test dates with a cumulative dose effect being observed on the first test date. This cumulative dose effect resulted in a reduction in the number of SETs as the effective total dose increased during testing. During all SET testing, the devices were exposed to a total fluence of $2x10^6$ion/cm^2 and a sufficient number of devices under test (DUTs) were used to keep the cumulative does to under 8.5krad.

Part Description

The ISL73148SEH is a radiation hardened 8-channel high precision14-bit SAR ADC (analog-to-digital converter) operating up to 900ksps with the integrated PGA bypassed and up to 480ksps with the integrated PGA enabled.

The ADC core is preceded by eight analog input channels followed by a buffered 8-to-1 multiplexer and a PGA (Programmable Gain Amplifier). The device features a peak SNR of 82dBFS when operating at 900ksps. With the PGA enabled, sampling rates up to 480ksps are supported. The PGA may be bypassed to allow the sample rate to be increased to 900ksps.

The product features 900/480ksps throughput with no data latency and features excellent linearity and dynamic accuracy. The ISL73148SEH offers a high-speed SPI-compatible serial interface that supports logic ranging from 2.2V to 3.6V using a separate digital I/O supply pin.

The ISL73148SEH offers a separate low power mode (LPM) pin that reduces power dissipation at lower sample rates. The analog input signal range is determined by an external reference applied to the V_{REF} pin with a supported input range of 2.4V to 2.6V.

The ISL73148SEH operates across the military temperature range from -55°C to +125°C and is available in a 28 Ld hermetically sealed Ceramic Dual Flat-Pack (CDFP) package.

The SEE testing of the ISL73148SEH was completed on two silicon versions. During the first two test sessions in June and August of 2021, Revision A silicon was used. Revision B silicon (released production silicon version)

was used during the third (final) test session in November 2021. Lot information for the first two test sessions was not logged, but in the final test session, three lots were tested: V6C750, V6C751, and V6C752.

Because the production silicon version is Revision B, the results from that silicon version serves as the focus of this report. However, the results from Revision A can be cited as well because the silicon design is similar between the two revisions and the results from the versions provide some information on manufacturing variability. In addition, the SEE results from Revision A were used to guide the test efforts for Revision B.

The samples were packaged without lids to allow irradiation, and only room temperature testing of the parts was done. No burn-in stressing was done on the parts.

Contents

1. SEE Testing

1.1 Objective

The testing was intended to find the limits for the supply voltages set by the onset of Destructive Single Event Effects (DSEE) at a LET of 86MeV·cm^2/mg (normal incidence gold). Additional testing was intended to identify and quantify SETs and SEFIs occurring in the output sample codes of the ISL73148SEH. The SET studies included irradiation with normal incidence gold (86MeV·cm^2/mg), silver (43MeV·cm^2/mg), argon (8.5MeV·cm^2/mg), and neon (2.7MeV·cm^2/mg).

1.2 Facility

SEE testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station Texas. This facility is coupled to a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The testing referred to in this report was performed on June 27, 2021, August 3, 2021, and November 17-18, 2021.

1.3 Setup

The ISL73148SEH was SEE evaluated using a general-purpose engineering evaluation board that allowed various application configurations to be used. The specific configurations changed with the type of testing. For destructive SEE testing (collectively called DSEE herein), the individual supply voltages and analog input were driven directly from an external power supply with currents monitored using an ammeter. For the SET testing, external power supplies supplied ±10V to the evaluation board and the ISL73148SEH supply voltages were generated by onboard LDOs while an onboard amplifier circuit connected to the analog input set the ADC input to midscale. The onboard LDOs kept noise to a minimum and allow for fine resolution of SET detection.

For the DSEE testing, the ADC input clock (CSB) was set to 483.092ksps sampling rate with the PGA enabled with a gain of 2, AV_{CC} varied up to 6.5V, DV_{CC} set to 4.6V, and V_{REF} set to 3.6V. The maximum sampling rate (with the PGA enabled) and the maximum voltages were used for AV_{CC}, DV_{CC}, and V_{REF} to achieve the worst-case conditions. The monitored parameters for the ADC are listed in Table 1.

Table 1. Monitored Parameters and Failure Criteria for the ISL73148SEH DSEE Testing

Parameter Monitored	Failure Criteria
AV_{CC} Supply Current	±10%
DV_{CC} Supply Current	±10%
V_{REF} Supply Current	±10%

For DSEE testing, the DV_{CC} (4.6V), and V_{REF} (3.6V) input voltages were held constant during both test dates. For all DSEE testing, the AV_{CC} voltage was started at 5.8V and increased in 0.1V steps until DSEE was observed or 6.5V was reached. During all test dates, the sample rate was set to 483.092ksps with the PGA enabled.

For SET testing, the ISL73148SEH was tested under five conditions as given in Table 5. The ISL73148SEH has a normal operation mode and a low power operation mode. In each operational mode, the PGA can be enabled or bypassed. For each mode of operation, the order of testing with the PGA enabled or bypassed was reversed from one DUT and/or LET to the next (for example, normal mode with the PGA bypassed followed by normal mode with the PGA enabled followed by normal mode with the PGA bypassed and so on). These configurations result in four possible test modes. The fifth test mode is achieved by enabling the SCAN function of the ISL73148SEH. The SCAN function sequences through the selection of the eight input channels beginning with channel 0 and ending with channel 7. As long as the ISL73148SEH SCAN function is enabled, it sequentially cycles through the selection of channels. When operating in the fifth test mode, the ISL73148SEH is in normal operation mode with the PGA bypassed to achieve the maximum sampling rate. Additional clocks on SDO were provided for the

information bits (info bits). For configurations where the PGA was bypassed, additional clocks were provided only for the channel info bits, but where the PGA was enabled, additional clocks were provided for the channel and gain info bits. For all test dates, the AV_{CC} supply was set to a voltage of 4.5V, the DV_{CC} supply was a voltage of 2.5V, and the V_{REF} input was set to a voltage of 2.5V. The AV_{CC} voltage corresponds to the minimum voltage for the ISL73148SEH. For each given mode, the ISL73148SEH was operated at the maximum sampling rate for that mode.

For all five test configurations, an onboard DAC (digital to analog converter) was used to drive channels 0 and 2 through 7 to independent values across the range of the ISL73148SEH. The onboard amplifier driver circuit was used to provide a DC input of $V_{REF}/2$ to channel 1. In the first four configurations where SCAN is not enabled, channel 1 is the observed channel. For the ISL73148SEH operating with bipolar data format, this means that the expected output code should be approximately 0 (zero scale). All other channels are driven to independent values different than which channel 1 is driven. The input conditions for all eight channels are summarized in Table 2 below.

Table 2. ISL73148SEH Channel Input Voltages and Input Sources for SET Testing

ADC Channel	Input Voltage (V)	Input Source
0	0.3	DAC
1	1.25	Amp Driver Circuit
2	0.6	DAC
3	0.9	DAC
4	1.5	DAC
5	1.8	DAC
6	2.1	DAC
7	2.4	DAC

Figure 1 shows the SET detection threshold that is configured inside the logic analyzer. The threshold window was widened slightly for the ISL73148SEH compared to the ISL73141SEH because of slight shifts observed in the offset during the initial test dates in June 2021. The slight shift in offset was explored and confirmed during the test session in August 2021 to set the appropriate threshold window for the testing that was completed in November 2021. Setting the ADC analog input to channel 1 to a mid-scale value enables the observation of positive and negative excursions in the output codes of the ISL73148SEH. A test run without a beam is performed to find the median output code on a per-part basis, and then a ±20 code threshold is applied around that value. If the output code of the ADC goes beyond this threshold it is counted as a SET. The ±20 code threshold was found by operating the ISL73148SEH and observing no output code excursion beyond the threshold with no beam at the TAMU facility. When the test run and calibration exercise are completed for channel 1 as previously described, the other seven channels are also observed to record the output code values. For each operating mode, the median code value for each of the eight channels is logged to a file. The median code for channel 1 is used to set the threshold window while the other seven channels are logged so that they can be used when post processing the SET data. When post processing the SET data for each test run, it can be determined if a SET occurred where the wrong channel was selected. Because the median code value is recorded for each channel, it can be determined if/when a channel was improperly selected. In addition, the channel information bits are monitored during the test and can be used to help determine the channel selection if/when a SET occurs. In the case that a SET occurs resulting in the wrong channel selection, the improperly selected channel can be identified by the value of the output code.

The ISL73148SEH evaluation board contains a CPLD, which takes the serial output data from the ADC and converts it to parallel. This data is input to a logic analyzer where it is observed for any SET. Figure 1 shows the SET detection threshold that is configured inside the logic analyzer (**Note:** the figure shows the threshold for channel 1 of the ISL73148SEH). The ADC input is set to approximately midscale using an amplifier circuit present

on the ISL73148SEH engineering evaluation board driving the ADC analog input. Setting the ADC analog input to a mid-scale value enables the observation of positive and negative excursions in the output codes of the ISL73148SEH. A test run without beam is performed to find the median output code on a per-part basis, and then a ±20 code threshold is applied around that value. During the calibration run, the median codes from all eight ADC channels are recorded. If the output code of the ADC goes beyond the specified threshold, it is counted as a SET. The ±20 code threshold was found by operating the ISL73148SEH and observing no output code excursion beyond the threshold with no beam at the TAMU facility. The threshold window was widened slightly for the ISL73148SEH compared to the ISL73141SEH because of slight shifts observed in the offset during the June 2021 and August 2021 test dates.

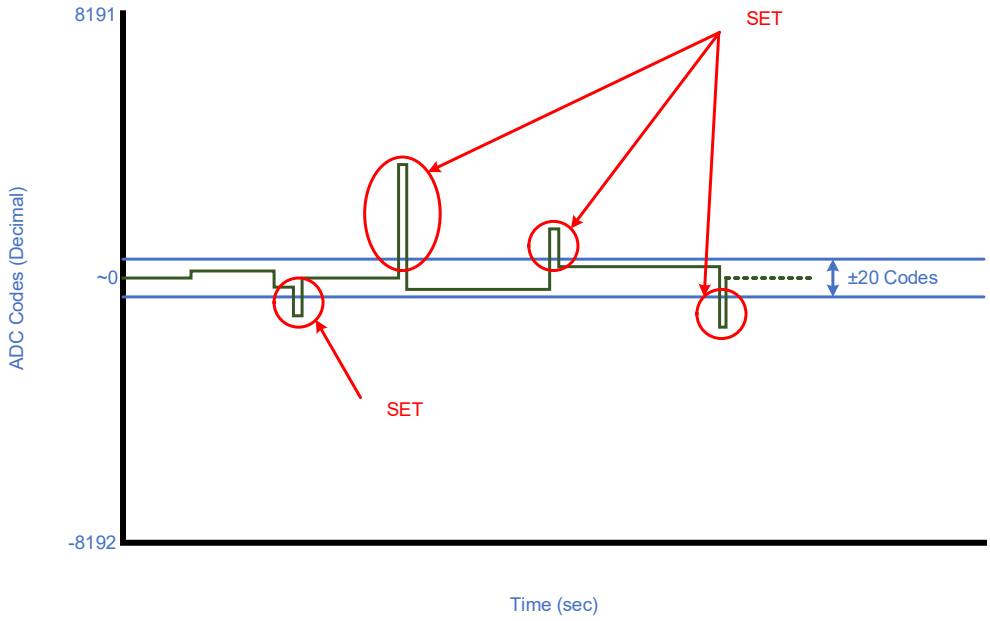

Figure 1. SET Detection Threshold

2. Results

2.1 DSEE Results

DSEE testing of the ISL73148SEH was performed on two parts from Revision A silicon on the June 2021 test date and on four parts from Revision B silicon during the November 2021 test dates.

Figure 2 shows the summary of the DSEE results for the ISL73148SEH Revision A devices tested on the June 2021 test date. One device passed at AV_{CC} = 6.5V and one device failed at AV_{CC} = 6.5V by violating the conditions in Table 1 for AV_{CC} current.

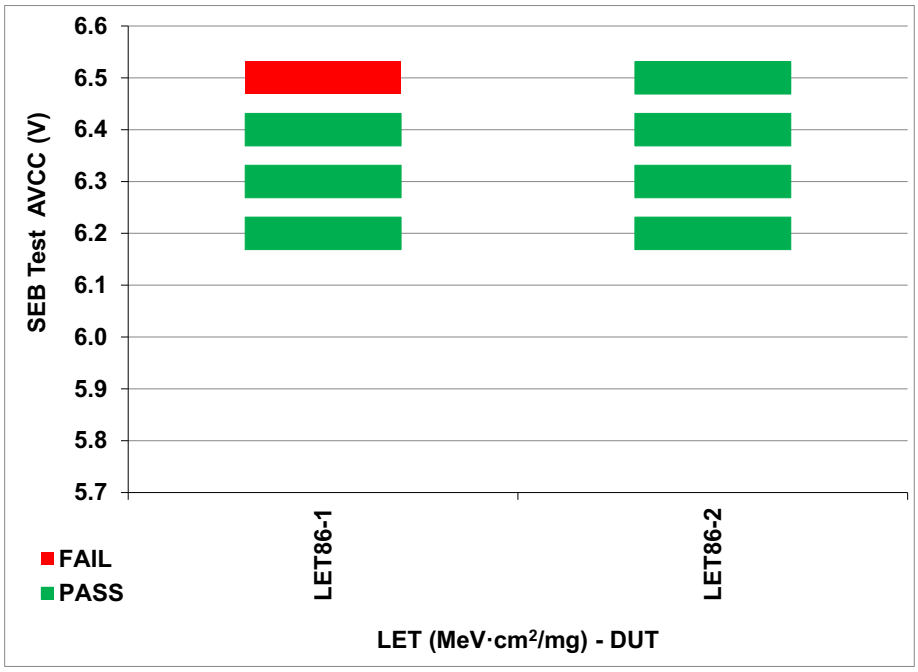

Figure 2. DSEE Testing Pass/Fail Summary - June 2021

Figure 3 shows the summary of the DSEE results for the ISL73148SEH Revision B devices (final released product) tested during the November 2021 test dates. All four devices passed at AV_{CC} = 6.5V and were not tested at a higher supply voltage.

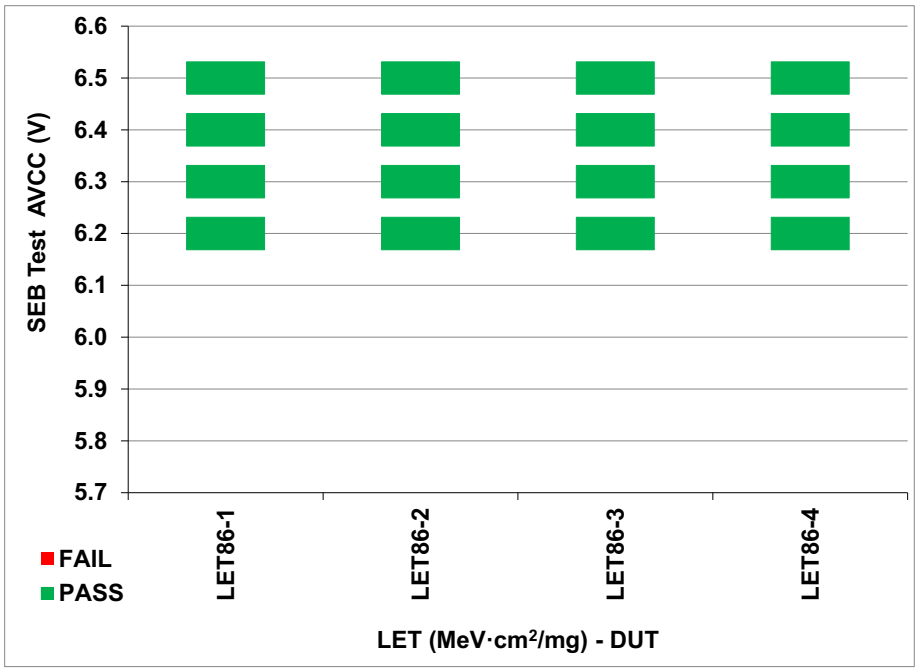

Figure 3. DSEE Testing Pass/Fail Summary - November 2021

DSEE of the ISL73148SEH was tested with normal incidence gold for 86MeV·cm^2/mg at a die temperature of 125°C ±10°C with DV_{CC}, and V_{REF}, input voltages held constant at maximum values of 4.6V and 3.6V, respectively. During all test dates, the AV_{CC} voltage was started at 6.2V and increased in 0.1V steps until DSEE was observed or 6.2V was reached. During all test dates, the ISL73148SEH was set to normal operation mode with the PGA bypassed with the sample rate was set to 900ksps. Before, during, and after irradiation three parameters (Table 1) were monitored to look for signs of DSEE. The results of this testing for the ISL73148SEH part are presented for Revision A in Table 3 and Revision B (final) silicon in Table 4. Failures to the criteria in Table 1 are indicated with bold and red text.

Table 3. ISL73148SEH Revision A DSEE Testing Results for Normal Incidence Gold at LET = 86MeV·cm^2/mg and 125°C ±10°C Die Temperature - June 2021[1]

Type- DUT	AV_{CC} (V)	I_{AVCC}			I_{DVCC}			I_{REF}		
		Pre (mA)	Post (mA)	Delta (%)	Pre (mA)	Post (mA)	Delta (%)	Pre (µA)	Post (µA)	Delta (%)
Rev A-1	6.2	22.123	22.129	0.03	5.137	5.137	0.00	433	433	0.00
	6.3	22.496	22.434	-0.28	4.807	4.810	0.06	436	434	-0.46
	6.4	22.810	22.805	-.02	4.800	4.810	0.21	433	433	0.00
	6.5	23.191	**63**	**171.66**	4.811	4.790	-0.44	432	436	0.93
Rev A-2	6.2	21.890	21.937	0.21	4.85	4.85	0.00	433	433	0.00
	6.3	22.298	22.275	-0.10	4.85	4.85	0.00	432	432	0.00
	6.4	22.642	22.628	-0.06	4.85	4.85	0.00	431	431	0.00
	6.5	23.010	23.000	-0.04	4.85	4.85	0.00	430	430	0.00

1. Each entry represents change across an irradiation of 5x10^{6}ion/cm^2.

Table 4. ISL73148SEH Revision B DSEE Testing Results for Normal Incidence Gold at LET = 86MeV·cm^2/mg and 125°C ±10°C Die Temperature - November 2021[1]

Type- DUT	AV_{CC} (V)	I_{AVCC}			I_{DVCC}			I_{REF}		
		Pre (mA)	Post (mA)	Delta (%)	Pre (mA)	Post (mA)	Delta (%)	Pre (µA)	Post (µA)	Delta (%)
Rev B-1	6.2	20.282	20.210	-.035	1.218	1.179	-3.20	338.2	338.2	0.00
	6.3	20.492	20.499	0.03	1.178	1.227	4.16	337.2	336.9	-0.09
	6.4	20.796	20.796	0.00	1.242	1.213	-2.33	336.1	336.1	0.00
	6.5	21.122	21.122	0.00	1.214	1.249	2.88	335.2	335.2	0.00
Rev B-2	6.2	20.032	20.910	4.38	1.296	1.292	-0.31	334.6	334.6	0.00
	6.3	20.414	20.414	0.00	1.306	1.283	-1.76	333.6	333.4	-0.06
	6.4	20.722	20.732	0.05	1.298	1.313	1.16	332.3	332.9	0.18
	6.5	21.063	21.088	0.12	1.311	1.293	-1.37	331.3	331.3	0.00
Rev B-3	6.2	20.278	20.259	-0.09	1.201	1.246	3.75	340.6	340.6	0.00
	6.3	20.533	20.532	0.00	1.245	1.246	0.08	339.6	339.5	-0.03
	6.4	20.831	20.861	0.14	1.247	1.256	0.72	338.6	338.8	0.06
	6.5	21.172	21.229	0.27	1.264	1.243	-1.66	338.1	337.6	-0.15

Table 4. ISL73148SEH Revision B DSEE Testing Results for Normal Incidence Gold at LET = 86MeV·cm^2/mg and 125°C ±10°C Die Temperature - November 2021[1] (Cont.)

Type- DUT	AV_{CC} (V)	I_{AVCC}			I_{DVCC}			I_{REF}		
		Pre (mA)	Post (mA)	Delta (%)	Pre (mA)	Post (mA)	Delta (%)	Pre (µA)	Post (µA)	Delta (%)
Rev B-4	6.2	20.086	20.075	-0.05	1.221	1.199	-1.80	338.7	338.6	-0.03
	6.3	20.352	20.378	0.13	1.197	1.222	2.09	337.6	337.6	0.00
	6.4	20.667	20.676	0.04	1.212	1.221	0.74	336.5	336.4	-0.03
	6.5	20.988	21.905	4.37	1.221	1.212	-0.74	335.6	335.8	-0.06

1. Each entry represents change across an irradiation of 5x10^{6}ion/cm^2.

2.2 SET Results

Single event transient testing was performed on the ISL73148SEH under the conditions listed in Table 5. The sequence in which these conditions were implemented was in alternating style from one DUT to the next in the order of 1-2, then 2-1 for normal mode tests and 3-4, then 4-3 for low power mode tests. Test condition #5 was specifically implemented to verify the channel sequencer of the ISL73148SEH, which is enabled by asserting the SCAN pin and was treated separately from modes 1 through 4. In SCAN mode, the ISL73148SEH sequences through all eight channels from 0 to 7 in repeating order. The alternating order of the tests in normal and low power modes was implemented to detect any potential dependency on cumulative dose effects. The sample rate of the ISL73148SEH changes depending on the operating mode and the state of the PGA. When the PGA is enabled for an additional 1µs of sampling time and when operating in low power mode, the CSB pulse width must be increased from the 150ns minimum in normal mode to 500ns. The sample rate for each operational mode is shown in Table 5. To detect any potential AV_{CC} voltage-related or sample rate-related issues, the ISL73148SEH was tested at the minimum analog supply voltage of AV_{CC} = 4.5V.

Table 5. ISL73148SEH SET Test Conditions

	Test Condition #1	Test Condition #2	Test Condition #3	Test Condition #4	Test Condition #5
AV_{CC}	4.5V	4.5V	4.5V	4.5V	4.5V
DV_{CC}	2.5V	2.5V	2.5V	2.5V	2.5V
V_{REF}	3.6V	3.6V	3.6V	3.6V	3.6V
Operating Mode	Normal	Normal	Low Power	Low Power	Normal
PGA Mode	Enabled	Bypassed	Enabled	Bypassed	Bypassed
SCAN	Disabled	Disabled	Disabled	Disabled	Enabled
Sample Rate	456.621ksps	900.091ksps	393.701ksps	684.932ksps	900.091ksps

SET cross-sections were produced for each of these conditions. The results from previous testing with the ISL73141SEH indicated a cumulative dose effect on the SET events when the total dose began to exceed 8.88krad. Therefore, during all SET testing performed in the June 2021, August 2021, and November 2021 test sessions, the cumulative dose was limited to less than 8.5krad to ensure a maximum number of observable SET.

The values shown in Table 6 represent the maximum amount of cumulative dose seen by any device for each given test condition.

Table 6. ISL73148SEH Maximum Cumulative Dose During SET Testing

Test Condition	LET = 2.7MeV·cm^2/mg (krad)	LET = 8.6MeV·cm^2/mg (krad)	LET = 43MeV·cm^2/mg (krad)	LET = 86MeV·cm^2/mg (krad)
	November 2021	November 2021	November 2021	November 2021
1	3.469	3.296	2.752	5.504
2	3.671	3.598	2.958	5.504
3	3.469	3.296	2.752	5.504
4	3.469	3.296	2.752	8.256
5	4.486	4.400	4.128	2.752

The cross-sections from the November 2021 test dates are shown in Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, and Figure 9. The cross-sections show a range of saturation values from 3.50x10^{2}µm^2 to 4.86x10^{5}µm^2. These cross-sections correspond to all five of the test conditions. For test condition #5, there are two cross-sections plotted. One cross-section (Figure 8) for test condition #5 is for data errors indicating that the data on the reported channel has violated the ±20 code threshold for the expected value on that channel. Recall that each channel has a specific input value applied to result in a particular output code. The other cross-section for test condition #5 is for info bit errors (Figure 9). The operational mode in test condition #5 is very similar to test condition #2 in terms of operating mode with the major difference being the enabling of the SCAN mode for test condition #5. Therefore, the cross-section plots show similar behavior between these modes. This illustrates that not only the number of SET are similar because of the similar operational mode, but also that the number of SET is independent of channel selection.

The implementation of the test was slightly different for test condition #5 compared to the other four test conditions. Unlike test conditions #1 through #4, the ADC data was not observed using a logic analyzer for test condition #5. Instead, all ADC sample data was collected and stored in memory during the radiation exposure. The stored data was subsequently post-processed using software on a PC using an algorithm similar to what is illustrated in Figure 1. In this case, however, the median code for each channel was input to the software on the PC where the ±20 code threshold around each median code value was applied to determine if a SET was present. In addition, this software performed a check on the info bits to determine if a SET had occurred with respect to the sequencing of the ADC channels. It was found that while SET occurred in the info bits, all of the SETs were a single sample where the info bits reported a different channel than was expected in the sequence. After such a SET occurred, the following sample indicated the next correct channel in the sequence. For example, a sequence with a SET in the info bits might look like this: 0-1-2-6-4-5-6-7. This shows that the info bits were out of sequence for one sample, but that the overall sequence would still rotate through all eight channels correctly outside of the one sample where the info bits were incorrect. The cross-section plot for the info bits shows a very low number of this type of SET because there were very few of these SE T observed. The two cross-sections generated for test condition #5 are illustrated in Figure 7 and Figure 8. The cross-section in Figure 7 shows the SETs where the observed ADC data violated the ±20 code threshold for the expected value. The cross-section in Figure 8 shows the SETs where the observed channel info bit did not match the expected value in the SCAN mode sequence. The data was further analyzed to determine the number of occurrences where there was simultaneously an observed ADC data SET and a channel info bit sequence SET. These simultaneous SETs occurred five times under exposure to gold ions (86MeV•cm^2/mg) and four times under exposure to silver ions (43MeV•cm^2/mg) and were not observed at any other LET.

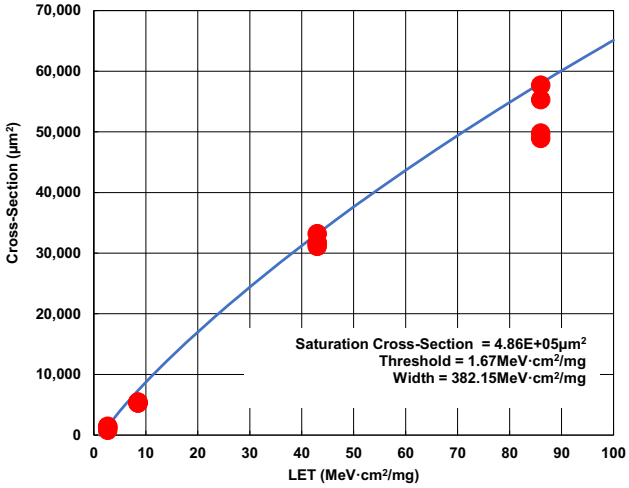

Figure 4. SET Cross-Section Test Condition #1

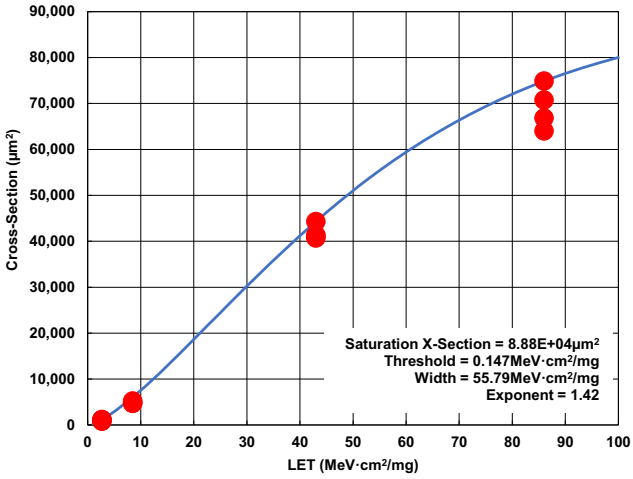

Figure 5. SET Cross-Section Test Condition #2

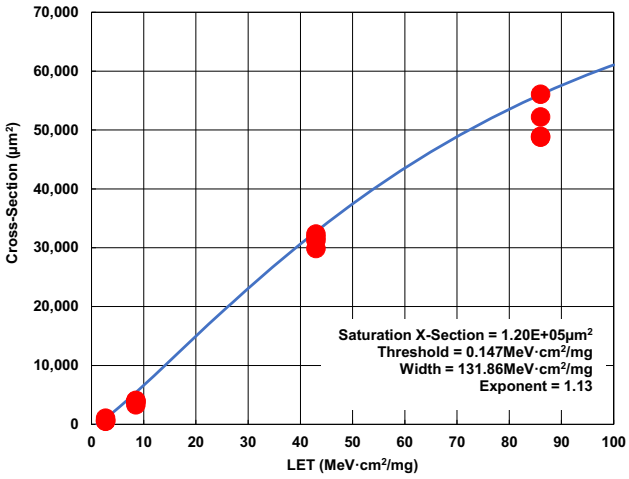

Figure 6. SET Cross-Section Test Condition #3

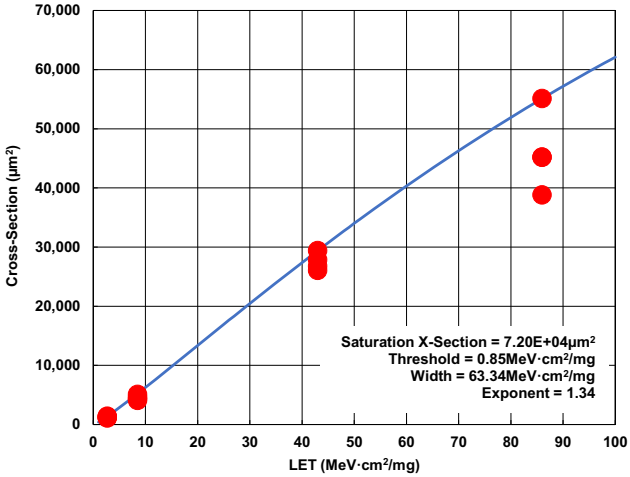

Figure 7. SET Cross-Section Test Condition #4

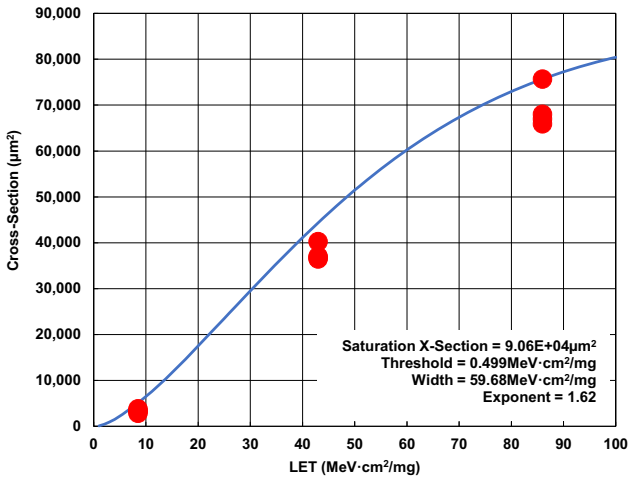

Figure 8. SET Cross-Section Test Condition #5 - Data

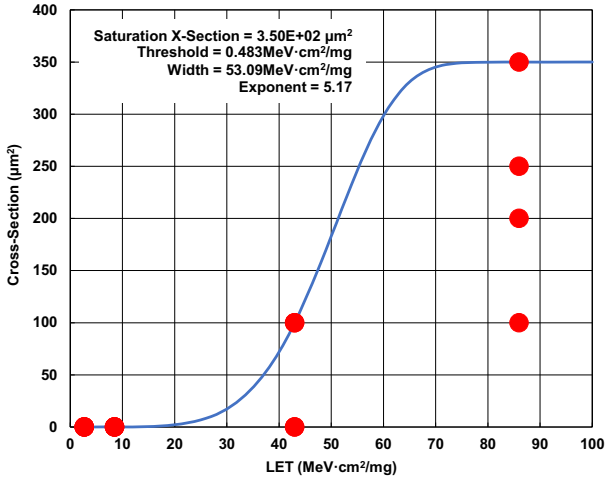

Figure 9. SET Cross-Section Test Condition #5 - Info Bits

The test data indicates that a majority of SET exhibited by the ISL73148SEH were under 100 codes in magnitude and lasted for a single sample. In fact, no SET observed lasted longer than two consecutive samples. The results show that out of all SET observed across all LET values that 81.93% were less than 100 codes in magnitude and 99.98% lasted for a single sample. The SET lasting two consecutive samples only occurred with LET values of 86MeV·cm^2/mg and 43MeV·cm^2/mg. There were no consecutive sample SETs observed at a LET value of 8.5MeV·cm^2/mg and 2.7MeV·cm^2/mg.

Figure 10, Figure 11, Figure 12, and Figure 13 show the magnitude versus time of a typical set of SET test runs at a LET of 2.7MeV·cm^2/mg under test conditions #1 through #4. As can be seen, the delta between the expected code and the actual code for each SET is generally less than 64 codes. A typical set of SET test runs at a LET of 86MeV·cm^2/mg is shown in Figure 14, Figure 15, Figure 16, and Figure 17. At this LET, there are a fews SET that are near positive and negative full scale, but the majority are within 128 codes of the expected value near mid-scale. No SEFIs were observed and the ADC returned to the expected code value range after every SET at all LET values that were tested.

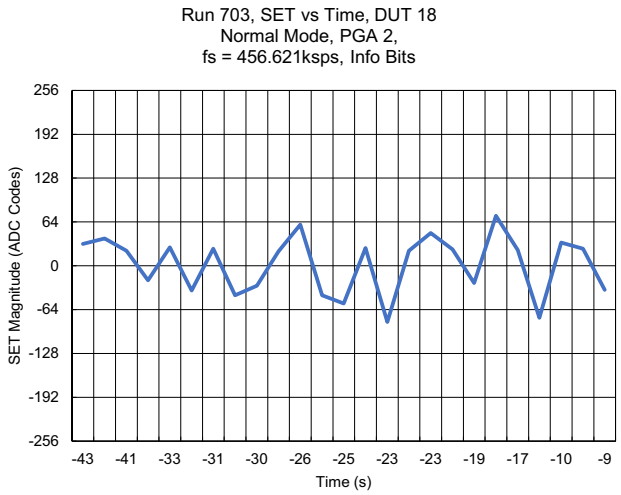

Figure 10. SET at LET = 2.7, Test Condition #1: Normal Mode, PGA Gain = 2

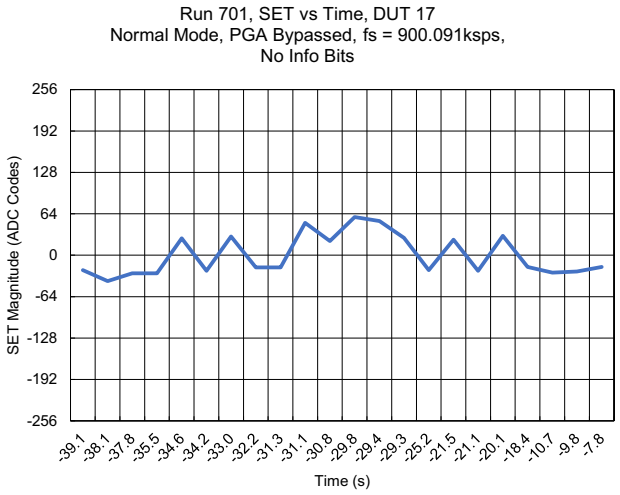

Figure 11. SET at LET = 2.7, Test Condition #2: Normal Mode, PGA Bypassed

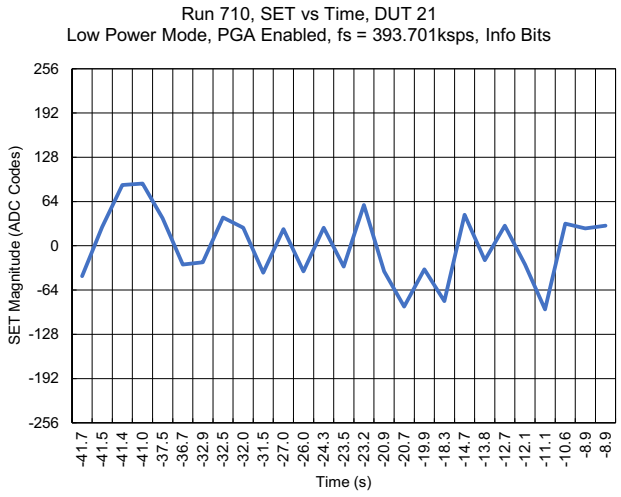

Figure 12. SET at LET = 2.7, Test Condition #3: Low Power Mode, PGA Gain = 2

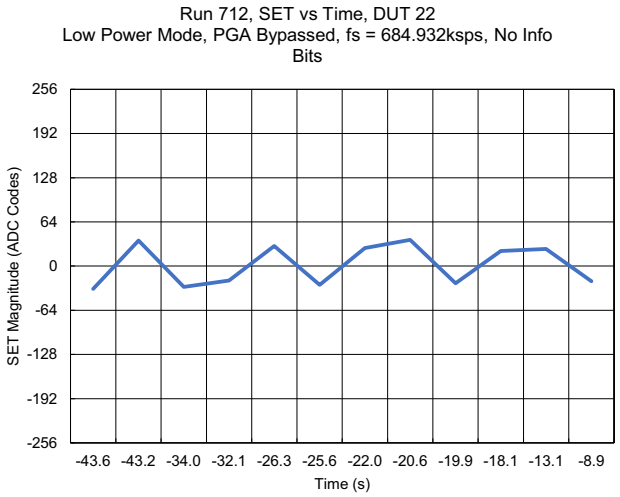

Figure 13. SET at LET = 2.7, Test Condition #4: Low Power Mode, PGA Bypassed

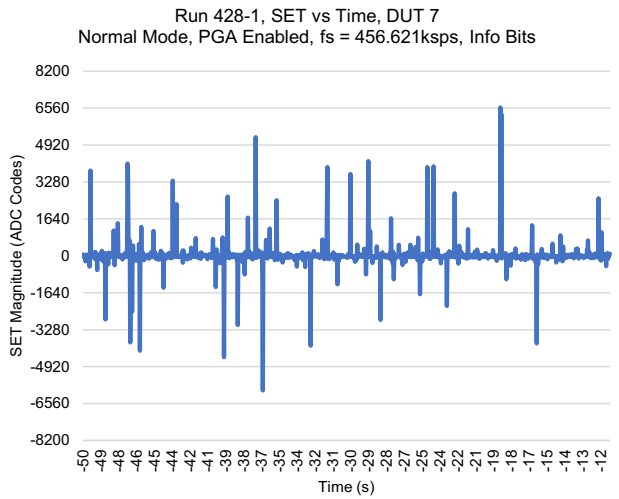

Figure 14. SET at LET = 86, Test Condition #1: Normal Mode, PGA Gain = 2

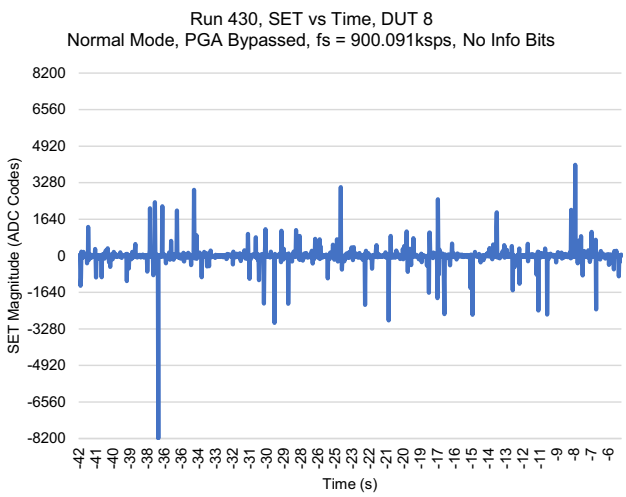

Figure 15. SET at LET = 86, Test Condition #2, Normal Mode, PGA Bypassed

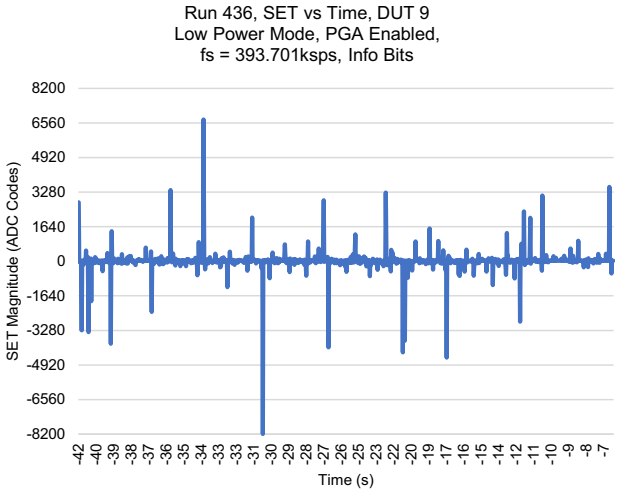

Figure 16. SET at LET = 86, Test Condition #3: Low Power Mode, PGA Gain = 2

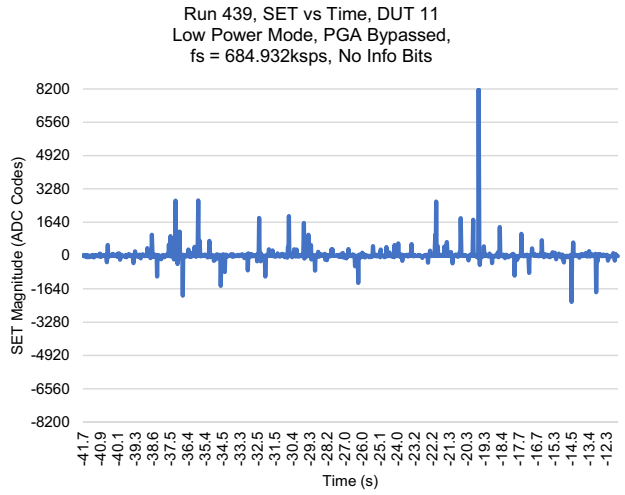

Figure 17. SET at LET = 86, Test Condition #4: Low Power Mode, PGA Bypassed

For the SET test runs shown in Figure 10 through Figure 17, a set of histograms were generated and are shown in Figure 18 through Figure 25. Even at the highest LET of 86MeV·cm^2/mg most of the SET are within 128 codes or less of the expected value. The expected code value is in the range of code 0 (mid-scale value) so the max deviation should be less than 8500 codes even if the SET excursion is to either positive or negative full scale. The histogram plots show that distribution of the SET code deltas is reasonably Gaussian and primarily concentrated close to the expected mid-scale value.

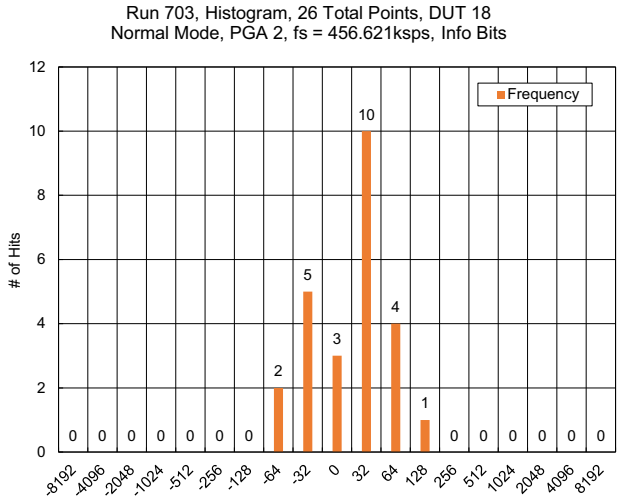

Figure 18. Histogram at LET = 2.7, Test Condition #1: Normal Mode, PGA Gain = 2

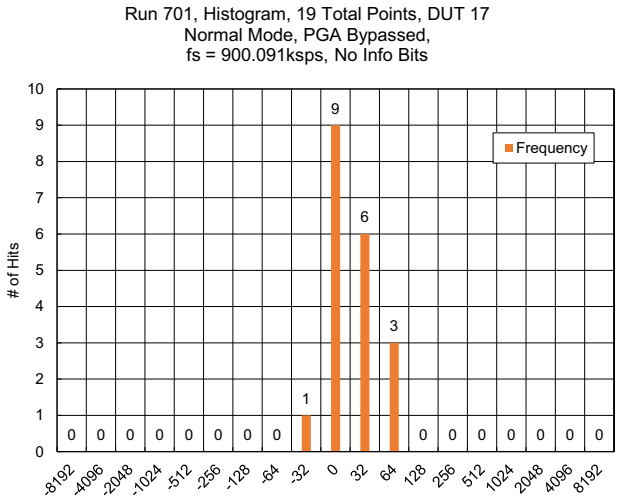

Figure 19. Histogram at LET = 2.7, Test Condition #2: Normal Mode, PGA Bypassed

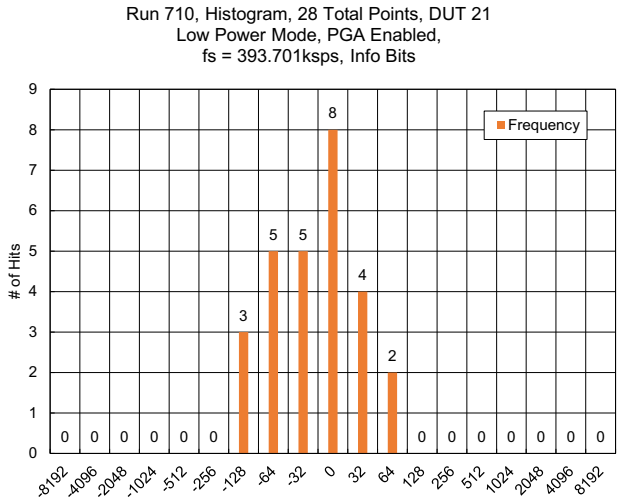

Figure 20. Histogram at LET = 2.7, Test Condition #3: Low Power Mode, PGA Gain = 2

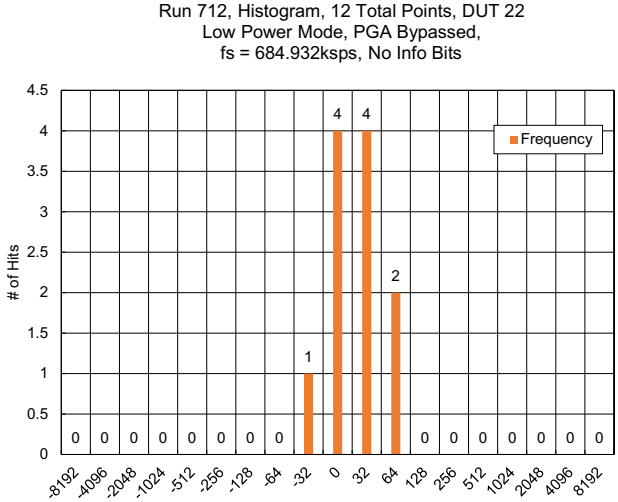

Figure 21. Histogram at LET = 2.7, Test Condition #4: Low Power Mode, PGA Bypassed

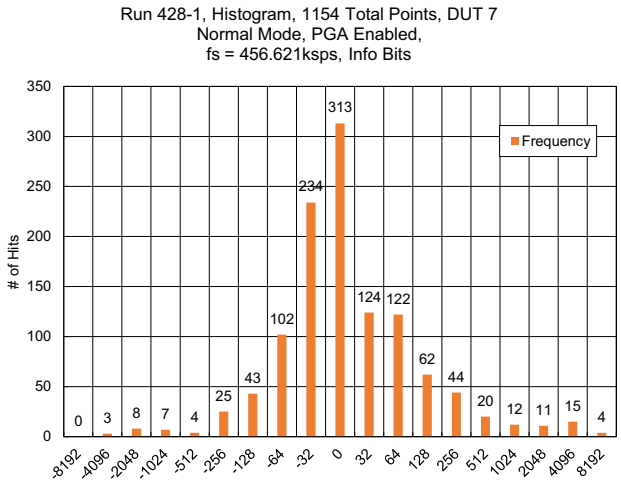

Figure 22. Histogram at LET = 86, Test Configuration #1: Normal Mode, PGA Gain = 2

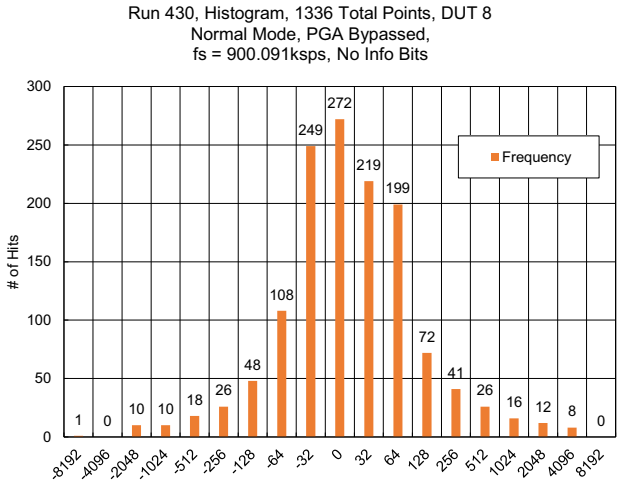

Figure 23. Histogram at LET = 86, Test Configuration #2: Normal Mode, PGA Bypassed

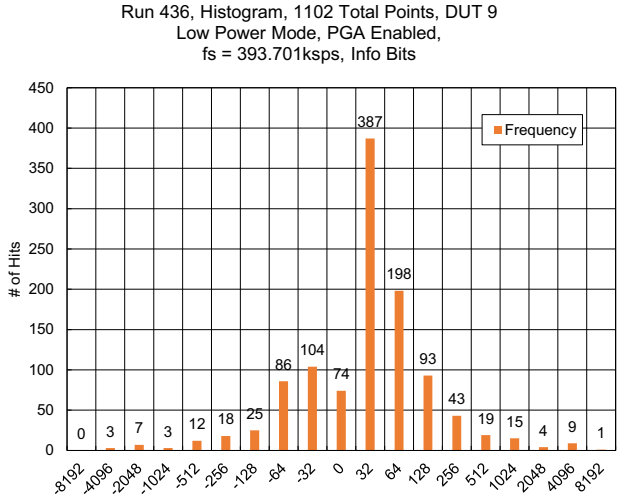

Figure 24. Histogram at LET = 86, Test Configuration #3: Low Power Mode, PGA Gain = 2

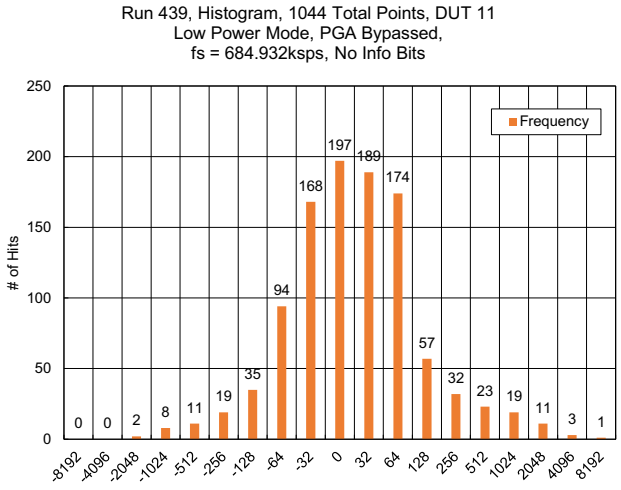

Figure 25. Histogram at LET = 86, Test Configuration #4: Low Power Mode, PGA Bypassed

All SET test runs from the final qualification testing in November 2021 are given in Table 7. Information is provided on the test conditions including DUT number, test number, LET, sample rate, operating mode, PGA condition, SCAN mode, total fluence, and approximate TID (total ionizing dose). The test results are given in terms of total SET, two consecutive sample SET, percentage of SET less than 100 codes in magnitude, and percentage of single sample SET.

During all testing dates for the ISL73148SEH, the total fluence was limited to $2x10^6$ for all test runs. The ISL73148SEH devices were tested with a range of LET values from 86MeV·cm^2/mg (gold) down to 2.7MeV·cm^2/mg (neon) including 8.5MeV·cm^2/mg (argon) and 43MeV·cm^2/mg (silver) all at normal incidence. By keeping the total fluence low during the test, the cumulative dose was maintained below 8.88krad, allowing for a higher number of SETs to be observed. Because previous results showed that the SET decreased with a higher cumulative dose, keeping the exposure of each DUT limited allows for the highest number of SET to be observed. This resulted in a condition where a worst-case cross-section of SET could be achieved. Overall, the data shows that the number of SETs decrease as the LET decreases. In addition, the average magnitude of the SET observed stays relatively small (less than 128 LSB deviation) across all LET even at the highest LET tested at

86MeV·cm^2/mg. The ISL73148SEH returned to normal operation after every SET observed and no SEFIs were observed during any test run.

Table 7. ISL73148SEH Revision B SET Testing Results - November 2021

Run	DUT	LET (cm^2/mg)	Sample Rate (ksps)	Operating Mode	PGA[1]	Info Bits[1]	SCAN	Approx. TID (krad)	Total SET	2 Sample SET	% SET <100 Codes	% SET Single Sample
427	7	86	900.091	Normal	Byp.	Dis.	No	2.752	1415	0	82.12	100.00
428-1	7	86	456.621	Normal	EN	EN	No	5.504	1154	0	77.99	100.00
429	8	86	456.621	Normal	EN	Dis.	No	2.752	1106	0	79.11	100.00
430	8	86	900.091	Normal	Dis.	Dis.	No	5.504	1336	0	80.39	100.00
431	28	86	900.091	Normal	Byp.	Dis.	No	2.752	1497	0	81.03	100.00
432	28	86	456.621	Normal	EN	EN	No	5.504	978	1	70.76	99.90
433	29	86	456.621	Normal	EN	EN	No	2.752	996	0	76.31	100.00
434	29	86	900.091	Normal	Byp.	Dis.	No	5.504	1280	0	83.20	100.00
435	9	86	684.932	LPM	Byp.	Dis.	No	2.752	1121	0	84.66	100.00
436	9	86	393.701	LPM	EN	EN	No	5.504	1102	0	79.67	100.00
437	10	86	393.701	LPM	EN	EN	No	2.752	904	0	79.54	100.00
438	10	86	684.932	LPM	Byp.	Dis.	No	5.504	975	0	84.00	100.00
439	11	86	684.932	LPM	Byp.	Dis.	No	2.752	1044	0	81.51	100.00
440	11	86	393.701	LPM	EN	EN	No	5.504	903	2	78.18	99.78
441-1	12	86	393.701	LPM	EN	EN	No	5.504	776	1	58.76	99.87
442	12	86	684.932	LPM	Byp.	Dis.	No	8.256	978	1	78.83	99.90
443	13	86	900.091	Normal	Byp.	EN	Yes	2.752	1339	-	84.62	-
444	14	86	900.091	Normal	Byp.	EN	Yes	2.752	1318	-	83.31	-
445	15	86	900.091	Normal	Byp.	EN	Yes	2.752	1513	-	82.68	-
446-1	27	86	900.091	Normal	Byp.	EN	Yes	2.752	1360	-	82.06	-
301	17	43	900.091	Normal	Byp.	Dis.	No	1.376	886	1	84.65	99.89
302	17	43	456.621	Normal	EN	EN	No	2.752	622	0	76.53	100.00
303	18	43	456.621	Normal	EN	EN	No	1.376	664	0	82.83	100.00
304-1	18	43	900.091	Normal	Byp.	Dis.	No	2.958	814	0	88.08	100.00
305	19	43	900.091	Normal	Byp.	Dis.	No	1.376	822	0	86.74	100.00
306	19	43	456.621	Normal	EN	EN	No	2.752	630	0	80.63	100.00
307	20	43	456.621	Normal	EN	EN	No	1.376	635	1	80.63	99.84
308-1	20	43	900.091	Normal	Byp.	Dis.	No	2.958	826	0	87.05	100.00
309	21	43	684.932	LPM	Byp.	Dis.	No	1.376	597	0	87.10	100.00
310	21	43	393.701	LPM	EN	EN	No	2.752	557	0	81.33	100.00
311	22	43	393.701	LPM	EN	EN	No	1.376	588	0	81.97	100.00
312	22	43	684.932	LPM	Byp.	Dis.	No	2.752	624	0	84.13	100.00
313	23	43	684.932	LPM	Byp.	Dis.	No	1.376	646	0	89.16	100.00

Table 7. ISL73148SEH Revision B SET Testing Results - November 2021 (Cont.)

Run	DUT	LET (cm^2/mg)	Sample Rate (ksps)	Operating Mode	PGA[1]	Info Bits[1]	SCAN	Approx. TID (krad)	Total SET	2 Sample SET	% SET <100 Codes	% SET Single Sample
314	23	43	393.701	LPM	EN	EN	No	2.752	535	0	78.13	100.00
315	24	43	393.701	LPM	EN	EN	No	1.376	521	0	81.96	100.00
316	24	43	684.932	LPM	Byp.	Dis.	No	2.752	635	0	86.30	100.00
317	13	43	900.091	Normal	Byp.	EN	Yes	4.128	729	-	85.87	-
318	14	43	900.091	Normal	Byp.	EN	Yes	4.128	735	-	81.63	-
319	15	43	900.091	Normal	Byp.	EN	Yes	4.128	805	-	87.20	-
320	27	43	900.091	Normal	Byp.	EN	Yes	4.128	741	-	85.70	-
101	17	8.6	900.091	Normal	Byp.	Dis.	No	3.024	99	0	90.91	100.00
102	17	8.6	456.621	Normal	EN	EN	No	3.296	105	0	80.00	100.00
103	18	8.6	456.621	Normal	EN	EN	No	1.854	107	0	83.18	100.00
104	18	8.6	900.091	Normal	Byp.	Dis.	No	2.126	104	0	90.38	100.00
105	19	8.6	900.091	Normal	Byp.	Dis.	No	3.024	93	0	94.62	100.00
106	19	8.6	456.621	Normal	EN	EN	No	3.296	109	0	82.57	100.00
107-1	20	8.6	456.621	Normal	EN	EN	No	3.230	107	0	73.83	100.00
108-1	20	8.6	900.091	Normal	Byp.	Dis.	No	3.598	95	0	92.63	100.00
109	21	8.6	684.932	LPM	Byp.	Dis.	No	3.024	77	0	92.21	100.00
110	21	8.6	393.701	LPM	EN	EN	No	3.296	92	0	81.52	100.00
111	22	8.6	393.701	LPM	EN	EN	No	3.024	87	0	79.31	100.00
112	22	8.6	684.932	LPM	Byp.	Dis.	No	3.296	66	0	89.39	100.00
113	23	8.6	684.932	LPM	Byp.	Dis.	No	3.024	81	0	91.36	100.00
114	23	8.6	393.701	LPM	EN	EN	No	3.296	81	0	81.48	100.00
115	24	8.6	393.701	LPM	EN	EN	No	3.024	102	0	84.31	100.00
116	24	8.6	684.932	LPM	Byp.	Dis.	No	3.296	78	0	91.03	100.00
117	13	8.6	900.091	Normal	Byp.	EN	Yes	4.4	65	-	96.92	-
118	14	8.6	900.091	Normal	Byp.	EN	Yes	4.4	56	-	91.07	-
119	15	8.6	900.091	Normal	Byp.	EN	Yes	4.4	76	-	93.42	-
120	27	8.6	900.091	Normal	Byp.	EN	Yes	4.4	67	-	91.04	-
701	17	2.7	900.091	Normal	Byp.	Dis.	No	3.382	23	0	82.61	100.00
702	17	2.7	456.621	Normal	EN	EN	No	3.469	16	0	87.50	100.00
703	18	2.7	456.621	Normal	EN	EN	No	2.213	26	0	100.00	100.00
704	18	2.7	900.091	Normal	Byp.	Dis.	No	2.299	19	0	100.00	100.00
705	19	2.7	900.091	Normal	Byp.	Dis.	No	3.382	24	0	100.00	100.00
706	19	2.7	456.621	Normal	EN	EN	No	3.469	29	0	82.76	100.00
707	20	2.7	456.621	Normal	EN	EN	No	3.412	24	0	95.83	100.00
7082	20	2.7	900.091	Normal	Byp.	Dis.	No	3.671	20	0	100.00	100.00

Table 7. ISL73148SEH Revision B SET Testing Results - November 2021 (Cont.)

Run	DUT	LET (cm^2/mg)	Sample Rate (ksps)	Operating Mode	PGA[1]	Info Bits[1]	SCAN	Approx. TID (krad)	Total SET	2 Sample SET	% SET <100 Codes	% SET Single Sample
709	21	2.7	684.932	LPM	Byp.	Dis.	No	3.382	21	0	100.00	100.00
710	21	2.7	393.701	LPM	EN	EN	No	3.469	28	0	92.86	100.00
711	22	2.7	393.701	LPM	EN	EN	No	3.382	24	0	91.67	100.00
712	22	2.7	684.932	LPM	Byp.	Dis.	No	3.469	12	0	100.00	100.00
713	23	2.7	684.932	LPM	Byp.	Dis.	No	3.382	12	0	100.00	100.00
714	23	2.7	393.701	LPM	EN	EN	No	3.469	26	0	80.77	100.00
715	24	2.7	393.701	LPM	EN	EN	No	3.382	22	0	100.00	100.00
716	24	2.7	684.932	LPM	Byp.	Dis.	No	3.469	10	0	100.00	100.00
717	13	2.7	900.091	Normal	Byp.	EN	Yes	4.486	-	-	-	-
718	14	2.7	900.091	Normal	Byp.	EN	Yes	4.486	-	-	-	-
719	15	2.7	900.091	Normal	Byp.	EN	Yes	4.486	-	-	-	-
720	27	2.7	900.091	Normal	Byp.	EN	Yes	4.486	-	-	-	-

1. EN = Enabled, Byp. = Bypassed, and Dis. = Disabled.

3. SET Mitigation Options

The ISL73148SEH experiences SET when exposed to irradiation. These SET are low in magnitude on average with most below 128 LSBs of deviation from the expected value. Overwhelmingly most SET last for a single sample with less than 10 observed SET lasting for two consecutive samples. No observed SET lasted longer than two consecutive samples. To mitigate these events, some possible options are presented in this report.

One option is to collect a large number of samples (such as 10000 or larger) and average the samples collected to reduce the effects of a SET within those samples. Averaging a large number of samples lowers the impact of any SET that may be present in the collected data. The application would dictate the number of samples required to reduce the effects and a potential SET below any appreciable system-level effect.

In an application where a known range of values are expected, a second option is to discount a set of samples if the sample(s) within a given acquisition of data is outside a defined window. This method is similar to the detection of SET presented herein. In this case, if samples are collected outside the expected range, it is disregarded and another acquisition of data occurs. In the unlikely event that repeated data acquisitions show a SET then another option can be used.

In this third option, a combination of the first two options is a potential solution. This option collects a large number of samples (such as 10000) and throws away any sample beyond an application based threshold window, and averages the remaining samples. If a set of sample data is collected with an expected value of 8200 and an expected range of 8150 to 8250, any code outside of this range is thrown out while the remaining samples are recorded.

4. Discussion and Conclusions

The ISL73148SEH proved to be DSEE immune up to an AV_{CC} supply voltage of 6.4V for irradiation with normal incidence Au for 86MeV·cm^2/mg. The testing was completed with a die temperature of 125°C ±10°C. A DSEE event was only observed on one DUT at AV_{CC} = 6.5V during the June 2021 testing where the AV_{CC} domain experienced a destructive latch-up with the current on AV_{CC} increasing by 171.66%. During the November 2021 testing, no DSEE events were observed on either of the four DUTs up to AV_{CC} = 6.5V. This results in a maximum allowable AV_{CC} voltage of 6.4V.

The ISL73148SEH exhibited no SEFIs and had mostly single sample low magnitude SETs. A cumulative dose effect exists with the device that results in a reduction of the number of SETs as the total ionizing dose increases above 8.88krad. The saturation cross-sections ranged from 3.50x10^{2}µm^2 to 4.86x10^{5}µm^2. The highest saturation cross-section was for test condition #1 where the ISL73148SEH was operated in normal mode with the PGA gain set to a value of 2. The next highest cross-section was for test condition #3, which was similar to test condition #1 and had the PGA gain set to a value of 2 with the operating mode in low power mode. The saturation cross-section values were also similar between test conditions #2 and #5 where the PGA was bypassed in both cases and the difference was in the operating mode, normal versus low power. The saturation cross-section for data errors in test condition #5 was nearly identical to that of test condition #2, which indicates that the channel sequencer has little to no impact at all on the SET. Finally, the lowest saturation cross-section was for the info bit SET in test condition #5. This shows that few SETs were observed with the channel sequencer operation.

Only a small number of SETs lasting two consecutive samples were observed with most lasting for a single sample and none lasting longer than two consecutive samples. The SET remains at a relatively low average magnitude up to a LET of 86MeV·cm^2/mg (less than 128 LSBs deviation). The data shows out of all SET observed 81.93% were less than 128 codes in magnitude and 99.92% lasted for a single sample. The SET data exhibits that the ISL73148SEH does not experience large magnitude SET on average and that when a SET occurs, the device recovers after one sample the majority of the time with no event lasting longer than two consecutive samples. In addition, no device SEFIs were observed. Overall, the SEE data illustrates the ISL73148SEH is well-suited for space applications offering robust DSEE performance and SET with minimal impact to the end application.

5. Revision History

Rev.	Date	Description
1.03	Jan 3, 2024	Updated SEE Results and Discussion and Conclusion sections.
1.02	Jan 20, 2023	Updated Table 5 and Table 7. Updated the second paragraph on page 9.
1.01	Sep 19, 2022	Changed radiation tolerant to radiation hardened throughout the document.
1.00	Jun 22, 2022	initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.