Date: Apr. 26, 2024

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0135A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G24 Descriptions in the User's Manual: Hardware Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G24 Group	Lot No. All lots	Reference Document	RL78/G24 User's Manual: Hardware Rev. 1.10 R01UH0961EJ0110 (Nov. 2023)		

This document describes misstatements found in the RL78/G24 User's Manual: Hardware Rev. 1.10 (R01UH0961EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
3.1 Memory Space	Page 106, Page 107,Page 112	Incorrect descriptions revised
20.3.3 A/D converter mode register 0 (ADM0)	Page 1071, Page 1075 to Page 1077, Page1079,Page 1081, Page 1083, Page 1084, Page 1086, Page 1088, Page 1090, Page 1091, Page 1093	Incorrect descriptions revised
20.3.4 A/D converter mode register 1 (ADM1)	Page 1096	Incorrect descriptions revised
20.3.5 A/D converter mode register 2 (ADM2)	Page 1098, Page1099	Incorrect descriptions revised
39.6.1 Self-programming procedure	Page 1760	Incorrect descriptions revised
39.10.1 Overview of the data flash memory	Page 1811	Incorrect descriptions revised
40.3 Security Settings for On-chip Debugging	Page 1814	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0961EJ0110
1	3.1 Memory Space			Page 106, Page 107,Page 112	Page 3 to Page 5
2	20.3.3 A/D converter mode register 0 (ADM0)			Page 1071, Page 1075 to Page 1077, Page 1079, Page 1081, Page 1083, Page 1084, Page 1086, Page 1088, Page 1090, Page 1091, Page 1093	Page 6 to Page 18
3	20.3.4 A/D converter mode register 1 (ADM1)			Page 1096	Page 19
4	20.3.5 A/D converter mode register 2 (ADM2)			Page 1098, Page1099	Page 20, Page21
5	39.6.1 Self-programming procedure			Page 1760	Page 22
6	39.10.1 Overview of the data flash memory			Page 1811	Page 23
7	40.3 Security Settings for On-chip Debugging			Page 1814	Page 24

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G24 Correction for incorrect description notice

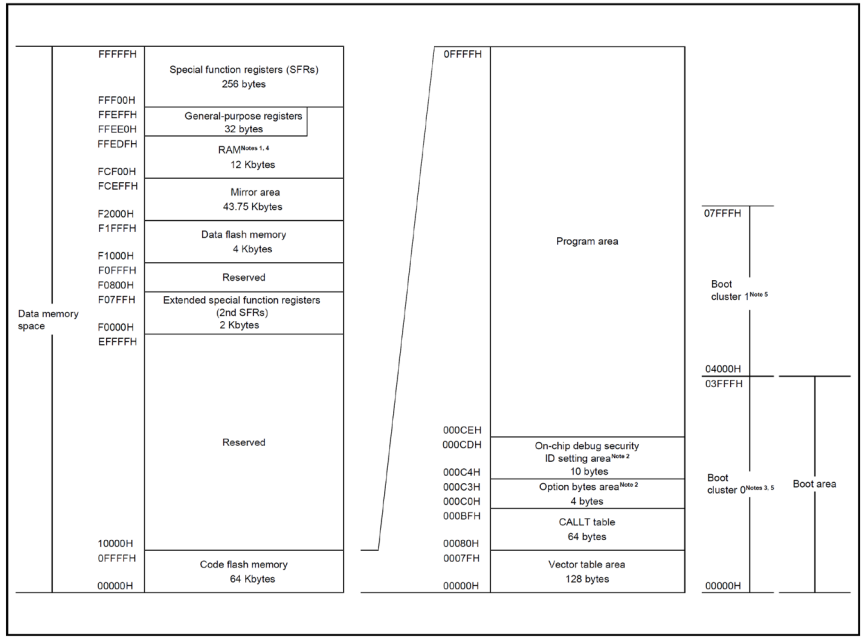
Document Number	Issue Date	Description
TN-RL*-A0135A/E	Apr. 26, 2024	First edition issued Corrections No.1 to No.7 revised (this document)

1. Memory Space (Page 106, Page107, Page 112)

Incorrect:
(Page 106)

Products in the RL78/G24 can access a 1 MB address space. For details, see Figures 3 - 1 and 3 - 2.

Figure 3 - 1 Memory Map (R7F101GxE (x = 6, 7, 8, A, B, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

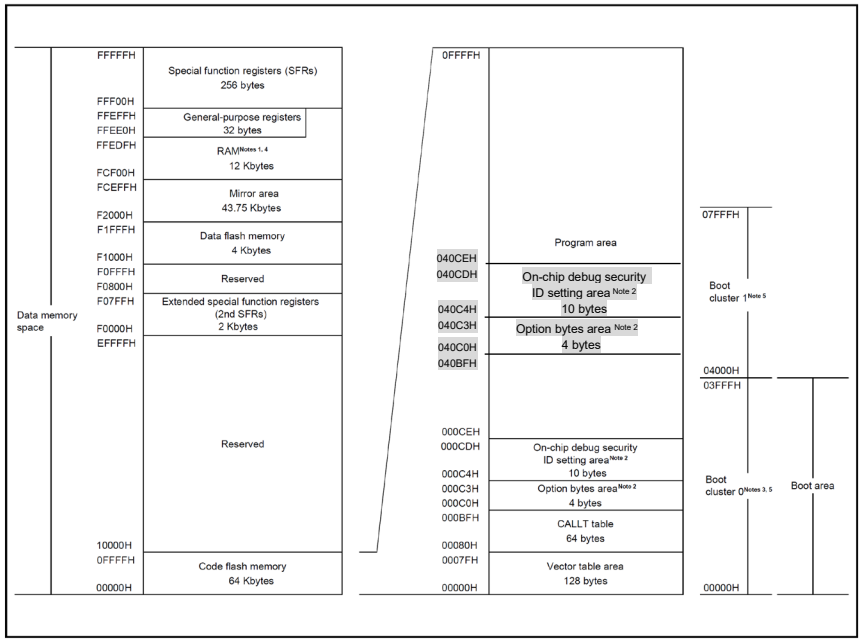
Note 2. **When boot swap is not used**: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Correct:

Products in the RL78/G24 can access a 1 MB address space. For details, see Figures 3 - 1 and 3 - 2.

Figure 3 - 1 Memory Map (R7F101GxE (x = 6, 7, 8, A, B, E, F, G, J, L))



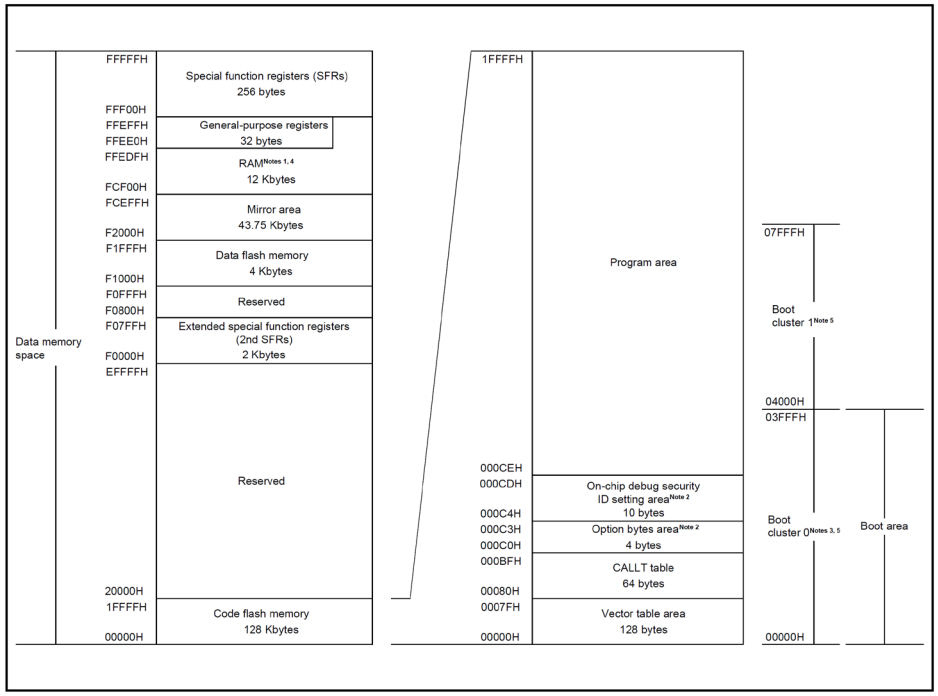
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 107)

Figure 3 - 2 Memory Map (R7F101GxG (x = 6, 7, 8, A, B, E, F, G, J, L))

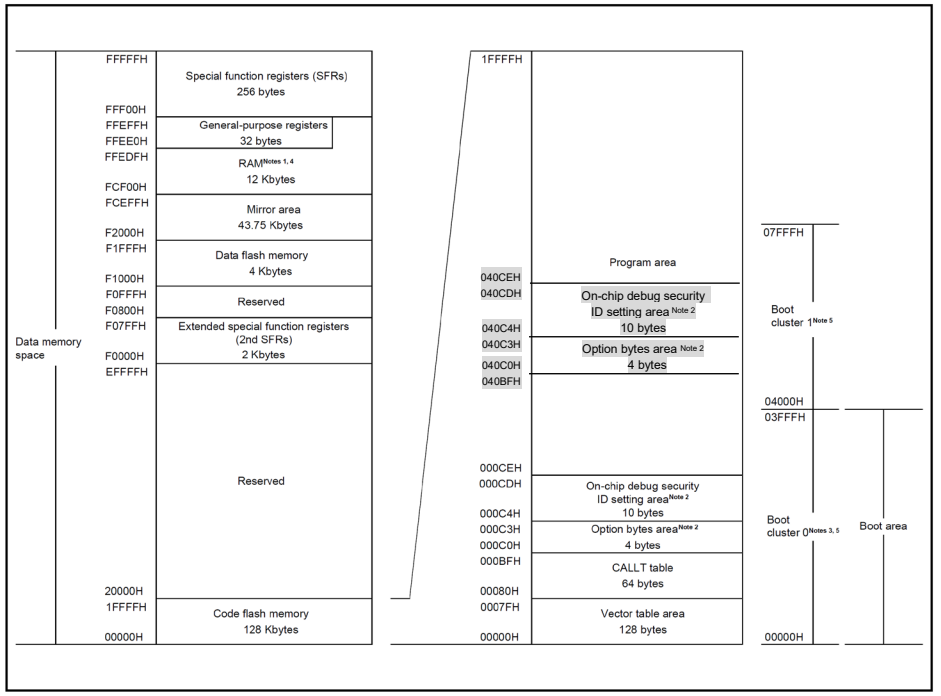


Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used**: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 2 Memory Map (R7F101GxG (x = 6, 7, 8, A, B, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 112)

(omitted)

3. Option bytes area
   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when **the boot swap is used**. For details, see Section 38 Option Bytes.
4. On-chip debug security ID setting area
   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when **the boot swap is not used** and at 000C4H to 000CDH and at 040C4H to 040CDH when **the boot swap is used**. For details, see Section 40 On-chip Debugging.

(omitted)

3. Option bytes area
   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 38 Option Bytes.
4. On-chip debug security ID setting area
   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. Set the 10-byte security ID for on-chip debugging at 000C4H to 000CDH when boot swapping is not to be used, that is, the value of the BTFLG bit in the FLSEC register is 1, and at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 40 On-chip Debugging.

2. 20.3.3 A/D converter mode register 0 (ADM0) (Page 1071, Page 1075 to Page1077, Page1079, Page 1081, Page 1083, Page 1084, Page 1086, Page 1088, Page 1090, Page 1091, Page 1093)

Incorrect:
(Page 1071)

Figure 20 - 4 Format of A/D Converter Mode Register 0 (ADM0)

(omitted)

ADCE	A/D voltage comparator operation control[Note 2]
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Note 1. For details of the FR[2:0] and LV[1:0] bits and A/D conversion, see Table 20 - 6 Selection of A/D Conversion Time.

Note 2. While in the software trigger no-wait mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 μs + 2 cycles of the conversion clock (fAD) from the start of operation for the operation to stabilize. Therefore, immediately after the ADCS bit is set to 1 after at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed from the time ADCE bit is set to 1, the conversion result becomes valid. When ADCS is set to 1 while ADCE = 0, A/D conversion starts after the stabilization wait time has passed. If ADCS is set to 1 before at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed, ignore data of the first conversion.

Caution 1. Change the ADMD, FR[2:0], and LV[1:0] bits while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. Setting change from ADCS = 1 and ADCE = 1 to ADCS = 1 and ADCE = 0 is prohibited.

Caution 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to follow the procedure described in 20.7 A/D Converter Setup Flowchart.

Caution 4. Do not set ADMS to 1 when the advanced mode is enabled.

Caution 5. Do not overwrite ADCS with 1 when the setting of ADCS is 1 in the advanced mode.

Caution 6. Do not overwrite ADCE with 1 when the setting of ADCE is 1 in the advanced mode.

Correct:

Figure 20 - 4 Format of A/D Converter Mode Register 0 (ADM0)

(omitted)

ADCE	A/D voltage comparator operation control[Note 2]
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Note 1. For details of the FR[2:0] and LV[1:0] bits and A/D conversion, see Table 20 - 6 Selection of A/D Conversion Time.

Note 2. While in the software trigger no-wait mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 μs + 2 cycles of the conversion clock (fAD) from the start of operation for the operation to stabilize. Therefore, immediately after the ADCS bit is set to 1 after at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed from the time ADCE bit is set to 1, the conversion result becomes valid. When ADCS is set to 1 while ADCE = 0, A/D conversion starts after the stabilization wait time has passed. If ADCS is set to 1 before at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed, ignore data of the first conversion.

Caution 1. Change the ADMD, FR[2:0], and LV[1:0] bits while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. Setting change from ADCS = 1 and ADCE = 1 to ADCS = 1 and ADCE = 0 is prohibited.

Caution 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to follow the procedure described in 20.7 A/D Converter Setup Flowchart.

Caution 4. Do not set ADMS to 1 when the advanced mode is enabled.

Caution 5. Do not overwrite ADCS with 1 when the setting of ADCS is 1 in the advanced mode.

Caution 6. Do not overwrite ADCE with 1 when the setting of ADCE is 1 in the advanced mode.

Caution 7. Following stoppage of conversion by setting the ADCS and ADCE bits to 0 from the conversion standby or conversion state, wait for at least 5 μs before restoring the values of the bits to 1. Note that, when changing the settings of bits ADMD, FR2 to FR0, LV1, and LV0, start by setting the ADCS and ADCE bits to 0, then wait for at least 0.2 μs before changing the rest of the bits.

(Page 1075)

Caution 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby state.

Caution 2. While in the one-shot conversion mode of the hardware trigger no-wait mode or advanced mode, the ADCS bit is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

Caution 3. Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby state).

Caution 4. In advanced mode, three cycles of the f_{CLK} clock are required from the occurrence of a trigger source until detection of the trigger. Table 20 - 5 lists the required numbers of clock cycles from the occurrence of a trigger or completion of the most recently executed conversion until A/D conversion starts in advanced mode.

Caution 5. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the f_{CLK} clock + conversion start time + A/D conversion time

Hardware trigger wait mode: **2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time**

Advanced mode: 3 cycles of the f_{CLK} clock + conversion start time + A/D conversion time

(omitted)

Caution 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby state.

Caution 2. While in the one-shot conversion mode of the hardware trigger no-wait mode or advanced mode, the ADCS bit is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

Caution 3. Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby state).

Caution 4. In advanced mode, three cycles of the f_{CLK} clock are required from the occurrence of a trigger source until detection of the trigger. Table 20 - 5 lists the required numbers of clock cycles from the occurrence of a trigger or completion of the most recently executed conversion until A/D conversion starts in advanced mode.

Caution 5. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the f_{CLK} clock + conversion start time + A/D conversion time

Hardware trigger wait mode: 2 f_{CLK} clock cycles + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 5µs

Advanced mode: 3 cycles of the f_{CLK} clock + conversion start time + A/D conversion time

(omitted)

(Page 1076)

Table 20 - 6 Selection of A/D Conversion Time (1/11)

1. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	64 f_{AD}	1 f_{AD}	2112/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	66 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	64 f_{AD}	1 f_{AD}	1056/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	66 µs	33 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	181 f_{AD}	1 f_{AD}	366/f_{CLK}	Setting prohibited	91.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	183/f_{CLK}	183 µs	45.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Table 20 - 6 Selection of A/D Conversion Time (1/11)

1. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	64 f_{AD}	1 f_{AD}	2112/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	66 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	64 f_{AD}	1 f_{AD}	1056/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	66 µs	33 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	181 f_{AD}	1 f_{AD}	366/f_{CLK}	Setting prohibited	91.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	183/f_{CLK}	183 µs	45.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

(Page 1077)

Table 20 - 6 Selection of A/D Conversion Time (2/11)

2. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

Table 20 - 6 Selection of A/D Conversion Time (2/11)

2. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

(Page 1079)

Table 20 - 6 Selection of A/D Conversion Time (3/11)

3. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	181 f_{AD}	4 f_{AD}	378/f_{CLK}	Setting prohibited	94.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	191/f_{CLK}	191 µs	47.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (3/11)

3. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	181 f_{AD}	4 f_{AD}	378/f_{CLK}	Setting prohibited	94.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	191/f_{CLK}	191 µs	47.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

(Page 1081)

Table 20 - 6 Selection of A/D Conversion Time (4/11)

4. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	4 f_{AD}	80 f_{AD}	4 f_{AD}	2816/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	88 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	80 f_{AD}	4 f_{AD}	1408/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	88 µs	44 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	107 f_{AD}	4 f_{AD}	230/f_{CLK}	Setting prohibited	57.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	117/f_{CLK}	117 µs	29.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (4/11)

4. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	4 f_{AD}	80 f_{AD}	4 f_{AD}	2816/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	88 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	80 f_{AD}	4 f_{AD}	1408/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	88 µs	44 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	107 f_{AD}	4 f_{AD}	230/f_{CLK}	Setting prohibited	57.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	117/f_{CLK}	117 µs	29.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

(Page 1083)

Table 20 - 6 Selection of A/D Conversion Time (5/11)

5. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V			
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	0	0	Normal 1	fCLK/32	1 fAD	64 fAD	1 fAD	8256/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	258 µs
0	0	0	1				fCLK/16	1 fAD	64 fAD	1 fAD	4128/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	258 µs	129 µs
1	1	0	0				fCLK/2	1 fAD	181 fAD	1 fAD	1452/fCLK	Setting prohibited	363 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	181 fAD	1 fAD	726/fCLK	726 µs	181.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark fCLK: CPU/peripheral hardware clock frequency

Table 20 - 6 Selection of A/D Conversion Time (5/11)

5. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V			
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	0	0	Normal 1	fCLK/32	1 fAD	64 fAD	1 fAD	8256/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	258 µs
0	0	0	1				fCLK/16	1 fAD	64 fAD	1 fAD	4128/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	258 µs	129 µs
1	1	0	0				fCLK/2	1 fAD	181 fAD	1 fAD	1452/fCLK	Setting prohibited	363 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	181 fAD	1 fAD	726/fCLK	726 µs	181.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark fCLK: CPU/peripheral hardware clock frequency

(Page 1084)

Table 20 - 6 Selection of A/D Conversion Time (6/11)

6. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	10304/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	322 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	5152/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	322 µs	161 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	860/fCLK	Setting prohibited	215 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	430/fCLK	430 µs	107.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

Table 20 - 6 Selection of A/D Conversion Time (6/11)

6. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	10304/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	322 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	5152/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	322 µs	161 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	860/fCLK	Setting prohibited	215 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	430/fCLK	430 µs	107.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

(Page 1086)

Table 20 - 6 Selection of A/D Conversion Time (7/11)

7. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)										2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	$f_{CLK}/32$	4 f_{AD}	64 f_{AD}	4 f_{AD}	8448/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	264 µs
0	0	0	1				$f_{CLK}/16$	4 f_{AD}	64 f_{AD}	4 f_{AD}	4224/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	264 µs	132 µs
1	1	0	0				$f_{CLK}/2$	4 f_{AD}	181 f_{AD}	4 f_{AD}	1464/f_{CLK}	Setting prohibited	366 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	734/f_{CLK}	734 µs	183.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (7/11)

7. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)										2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	$f_{CLK}/32$	4 f_{AD}	64 f_{AD}	4 f_{AD}	8448/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	264 µs
0	0	0	1				$f_{CLK}/16$	4 f_{AD}	64 f_{AD}	4 f_{AD}	4224/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	264 µs	132 µs
1	1	0	0				$f_{CLK}/2$	4 f_{AD}	181 f_{AD}	4 f_{AD}	1464/f_{CLK}	Setting prohibited	366 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	734/f_{CLK}	734 µs	183.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

(Page 1088)

Table 20 - 6 Selection of A/D Conversion Time (8/11)

8. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	4 fAD	80 fAD	4 fAD	10496/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	328 µs
0	0	0	1				fCLK/16	4 fAD	80 fAD	4 fAD	5248/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	328 µs	164 µs
1	1	0	0				fCLK/2	4 fAD	107 fAD	4 fAD	872/fCLK	Setting prohibited	218 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	6 fAD	107 fAD	4 fAD	438/fCLK	438 µs	109.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (fAD) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (tCONV) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (8/11)

8. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	4 fAD	80 fAD	4 fAD	10496/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	328 µs
0	0	0	1				fCLK/16	4 fAD	80 fAD	4 fAD	5248/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	328 µs	164 µs
1	1	0	0				fCLK/2	4 fAD	107 fAD	4 fAD	872/fCLK	Setting prohibited	218 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	6 fAD	107 fAD	4 fAD	438/fCLK	438 µs	109.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (fAD) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (tCONV) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

(Page 1090)

Table 20 - 6 Selection of A/D Conversion Time (9/11)

9. Normal mode 1 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7 are to be A/D converted

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion Note	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)						
(ADM1)	(ADM0)											2.4 V ≤ VDD ≤ 5.5 V					2.7 V ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz	fCLK = 48 MHz
0	0	0	0	0	0	Normal 1	fCLK/32	1 fAD	41 fAD	1 fAD	1376/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	43 μs	28.667 μs
0	0	0	1				fCLK/16	1 fAD	41 fAD	1 fAD	688/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	43 μs	21.5 μs	14.333 μs
1	1	0	0				fCLK/2	1 fAD	41 fAD	1 fAD	86/fCLK	Setting prohibited	21.5 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	41 fAD	1 fAD	43/fCLK	43 μs	10.75 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMODregister is 01B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the simultaneous sampling is to proceed, the following conditions must be met.
ADLSP = 0, FR[2:0] = 100, LV[1:0] = 00, fCLK ≥ 32 MHz, VDD ≥ 2.7 V
ADLSP = 0, FR[2:0] = 101, LV[1:0] = 00, fCLK ≥ 16 MHz, VDD ≥ 2.7 V

Remark fCLK: CPU/peripheral hardware clock frequency

Table 20 - 6 Selection of A/D Conversion Time (9/11)

9. Normal mode 1 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7 are to be A/D converted

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMODregister is 01B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 μs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the simultaneous sampling is to proceed, the following conditions must be met.
ADLSP = 0, FR[2:0] = 100, LV[1:0] = 00, fCLK ≥ 32 MHz, VDD ≥ 2.7 V
ADLSP = 0, FR[2:0] = 101, LV[1:0] = 00, fCLK ≥ 16 MHz, VDD ≥ 2.7 V

Remark fCLK: CPU/peripheral hardware clock frequency

(Page 1091)

Table 20 - 6 Selection of A/D Conversion Time (10/11)

10. Normal modes 1 and 2 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7, and ANI16 to ANI30 are to be A/D converted

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion Note	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ V_{DD} ≤ 5.5 V				2.7 V ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	f_{CLK} = 48 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	48 f_{AD}	1 f_{AD}	1600/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	33.333 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	48 f_{AD}	1 f_{AD}	800/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	25 µs	16.667 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	261 f_{AD}	1 f_{AD}	526/f_{CLK}	Setting prohibited	131.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	261 f_{AD}	1 f_{AD}	263/f_{CLK}	263 µs	65.75 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMOD register is 00B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Table 20 - 6 Selection of A/D Conversion Time (10/11)

10. Normal modes 1 and 2 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7, and ANI16 to ANI30 are to be A/D converted

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion Note	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ V_{DD} ≤ 5.5 V				2.7 V ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	f_{CLK} = 48 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	48 f_{AD}	1 f_{AD}	1600/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	33.333 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	48 f_{AD}	1 f_{AD}	800/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	25 µs	16.667 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	261 f_{AD}	1 f_{AD}	526/f_{CLK}	Setting prohibited	131.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	261 f_{AD}	1 f_{AD}	263/f_{CLK}	263 µs	65.75 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMOD register is 00B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

(Page 1093)

Table 20 - 6 Selection of A/D Conversion Time (11/11)

11. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (advanced mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)						
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz	fCLK = 48 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	54.667 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs	27.333 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

Table 20 - 6 Selection of A/D Conversion Time (11/11)

11. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (advanced mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)						
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz	fCLK = 48 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	54.667 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs	27.333 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

3. 20.3.4 A/D converter mode register 1 (ADM1) (p. 1096)

Incorrect:

(omitted)

Caution 1. Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).

Caution 2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time

Hardware trigger wait mode: **2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time**

(omitted)

Correct:

(omitted)

Caution 1. Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).

Caution 2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time

Hardware trigger wait mode: 2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 5μs

(omitted)

4. 20.3.5 A/D converter mode register 2 (ADM2) (Page 1098, Page 1099)

Incorrect:

(Page 1098)

(omitted)

Figure 20 - 8 Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	ADTYP1	ADTYP0

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AVREFP/ANI0
1	0	Supplied from the internal reference voltage Note 1
1	1	Discharged

• Use the following procedure to rewrite the ADREFP[1:0] bits.
<1> Set ADCE = 0.
<2> Set ADREFP[1:0] to 11B. This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<3> Reference voltage discharge time: 1 µs
This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<4> Change the value of the ADREFP[1:0] bit.
<5> Reference voltage stabilization wait time A
<6> Set ADCE = 1.
<7> Reference voltage stabilization wait time B
When the ADREFP[1:0] bits are set to 10B, A = 5 µs and B = 1 µs + 2 cycles of the conversion clock (fAD).
When the ADREFP[1:0] bits are set to 00B or 01B, **a wait A is not required** and B = 1 µs + 2 cycles of the conversion clock (fAD).
After <7> stabilization time, start the A/D conversion.
• When the ADREFP[1:0] bits are set to 10B, A/D conversion of the temperature sensor output voltage and internal reference voltage Note 1 cannot proceed.
Be sure to perform A/D conversion while ADISS = 0.

(omitted)

Correct:

(omitted)

Figure 20 - 8 Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	ADTYP1	ADTYP0

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AVREFP/ANI0
1	0	Supplied from the internal reference voltage Note 1
1	1	Discharged

• Use the following procedure to rewrite the ADREFP[1:0] bits.
<1> Set ADCE = 0.
<2> Wait for at least 0.2 us.
<3> Set ADREFP[1:0] to 11B. This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<4> Reference voltage discharge time: 1 µs
This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<5> Change the value of the ADREFP[1:0] bit.
<6> Reference voltage stabilization wait time A
<7> Set ADCE = 1.
<8> Reference voltage stabilization wait time B
When the ADREFP[1:0] bits are set to 10B, A = 5 µs and B = 1 µs + 2 cycles of the conversion clock (fAD).
When the ADREFP[1:0] bits are set to 00B or 01B, A = 4.8 µs and B = 1 µs + 2 cycles of the conversion clock (fAD).
After <8> stabilization time, start the A/D conversion.
• When the ADREFP[1:0] bits are set to 10B, A/D conversion of the temperature sensor output voltage and internal reference voltage Note 1 cannot proceed.
Be sure to perform A/D conversion while ADISS = 0.

(omitted)

(Page 1099)

(omitted)

AWC	Specification of the SNOOZE mode
0	Does not use the SNOOZE mode function
1	Uses the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (fCLK). If any other clock is selected, specifying this mode is prohibited.
- When using the SNOOZE mode function, set AWC to 0 in software trigger wait mode, and set AWC to 1 in hardware trigger wait mode.
- Using the SNOOZE mode function in the software trigger no-wait mode, hardware trigger no-wait mode, or advanced mode is prohibited.
- Using the SNOOZE mode function in hardware trigger wait mode in sequential conversion mode is prohibited.
- When using the SNOOZE mode function, specify a hardware trigger interval of at least **"transition time to SNOOZE mode[Note 2] + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 cycles of the fCLK clock".**
- Even when using the SNOOZE mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to STOP mode. Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation. If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE mode or normal operation.

(omitted)

(omitted)

AWC	Specification of the SNOOZE mode
0	Does not use the SNOOZE mode function
1	Uses the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (fCLK). If any other clock is selected, specifying this mode is prohibited.
- When using the SNOOZE mode function, set AWC to 0 in software trigger wait mode, and set AWC to 1 in hardware trigger wait mode.
- Using the SNOOZE mode function in the software trigger no-wait mode, hardware trigger no-wait mode, or advanced mode is prohibited.
- Using the SNOOZE mode function in hardware trigger wait mode in sequential conversion mode is prohibited.
- When using the SNOOZE mode function, specify a hardware trigger interval of at least "transition time to SNOOZE mode[Note 2] + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 cycles of the fCLK clock + 5us".
- Even when using the SNOOZE mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to STOP mode. Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation. If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE mode or normal operation.

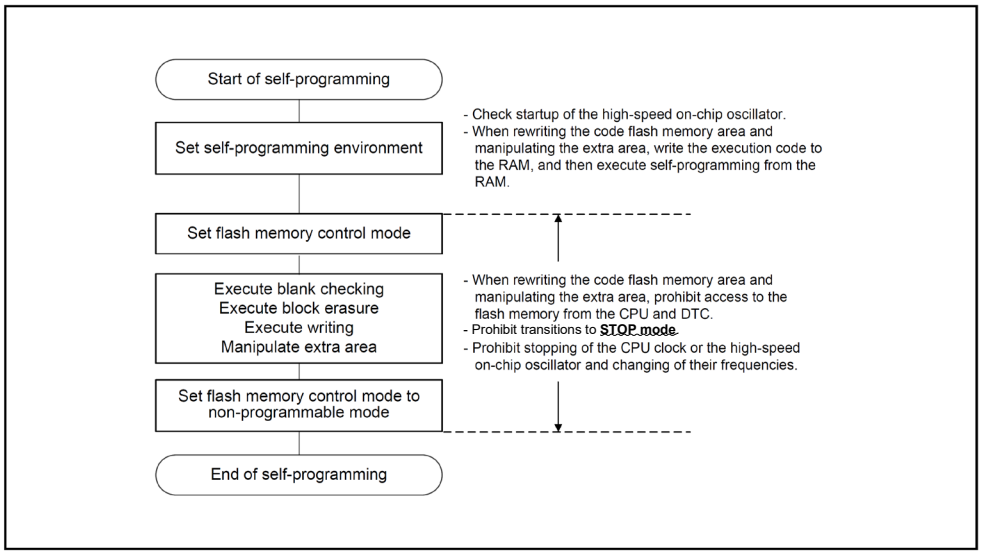
(omitted)

5. 39.6.1 Self-programming procedure (Page 1760)

Incorrect:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 39.6.2 Registers to control the flash memory.

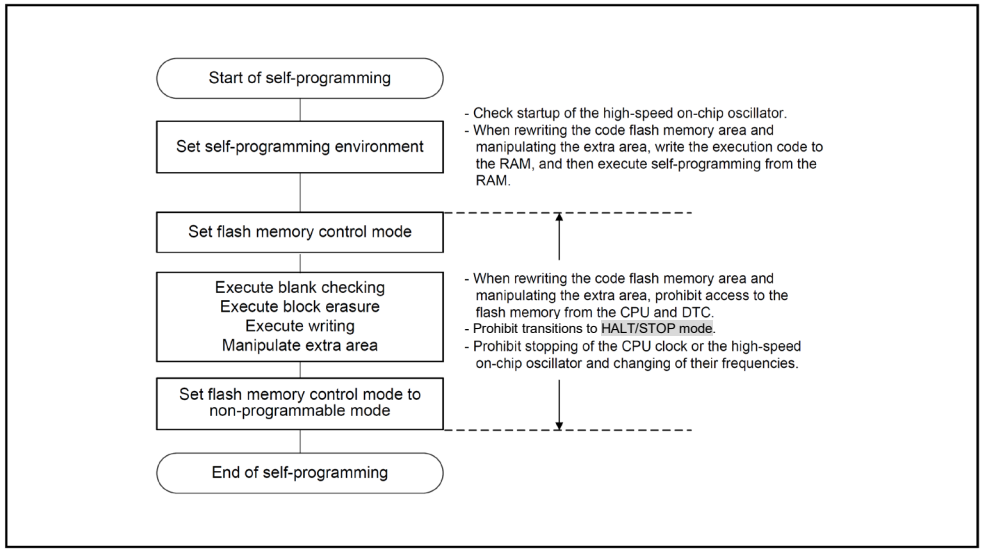
Figure 39 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



Correct:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 39.6.2 Registers to control the flash memory.

Figure 39 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



6. 39.10.1 Overview of the data flash memory (Page 1811)

Incorrect:

An overview of the data flash memory is provided below.

(omitted)

• Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
• Transition to the **STOP mode** is prohibited while rewriting the data flash memory.

Correct:

An overview of the data flash memory is provided below.

(omitted)

• Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
• Transition to the HALT/STOP mode is prohibited while rewriting the data flash memory.

7. 40.3 Security Settings for On-chip Debugging (Page 1814)

Incorrect:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 39.9 Security Settings).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 38 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.Note

Note The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Table 40 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID codeNote
040C4H to 040CDH	

Note. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

Correct:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 39.9 Security Settings).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 38 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.Note

Note The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Table 40 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID codeNote 1, 2
040C4H to 040CDH	

Note 1. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

Note 2. Set the 10-byte security ID for on-chip debugging at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0.