

4 Channel Power Up/Down Sequencer Using GreenPAK™ SLG46110

This application note describes a 4-channel power up/down sequencer implemented using the SLG46110 GreenPAK.

The application note comes complete with design files which can be found in the Reference section.

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1. Terms and Definitions

CNT	Counter
DLY	Delay
EN	Enable
LUT	Look-up Table
OSC	Oscillator
PG	Power Good
POR	Power-On Reset
VDD	Supply Voltage

2. References

For related documents and software, please visit:

[GreenPAK | Renesas](#)

Download our free Go Configure Software Hub [1] to open the .gp file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC. We also recommend that you familiarize yourself with the full capabilities of the GreenPak SLG46110 [5].

[1] [GreenPAK Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics

[2] [AN-1067 Power Sequencer using GreenPAK.gp](#), GreenPAK Design File, Renesas Electronics

[3] [GreenPAK Development Tools](#), GreenPAK Development Tools Webpage, Renesas Electronics

[4] [GreenPAK Application Notes](#), GreenPAK Application Notes Webpage, Renesas Electronics

[5] [SLG46110 Datasheet](#), Renesas Electronics

3. Introduction

Modern day electronics often have multi-core and multi-rail processors that require regulated power up sequencing for each rail in order to maintain proper operation. Some processors also require regulated power down sequencing for each rail in order to maximize processor life cycle.

The GreenPAKs consist of various analog and digital building blocks called “macro cells”; the delay and look-up-table cells can be used to build highly intelligent sequencers with reconfigurable turn on and turn off sequence. This app note goes over 3 example designs.

4. Design 1: Power UP Only Sequencing

The SLG46110's delay macro cells “CNTx/DLYx” can be used to generate daisy-chained delays starting from an enable signal as shown in Figure 1. Sequencing begins at the rising edge of the “EN” pin. A 2-bit Look-Up-Table (LUT) is used to make sure the GreenPAK's power-on-reset (POR) is met when the sequence begins. The “CNT0/DLY0” cell introduces a delay from EN high to OUT0 high. The “CNT1/DLY1” cell then introduces a delay from OUT0 high to OUT1 high and so on. The 3-bit LUTs between the delay cells and output pins realize an AND function. When “Enabled” is high, these LUTs make sure an output turns high with some delay after the previous rail turns high. When “Enable” is low, these LUTs make sure all outputs are pulled low instantaneously and simultaneously as show in Figure 2.

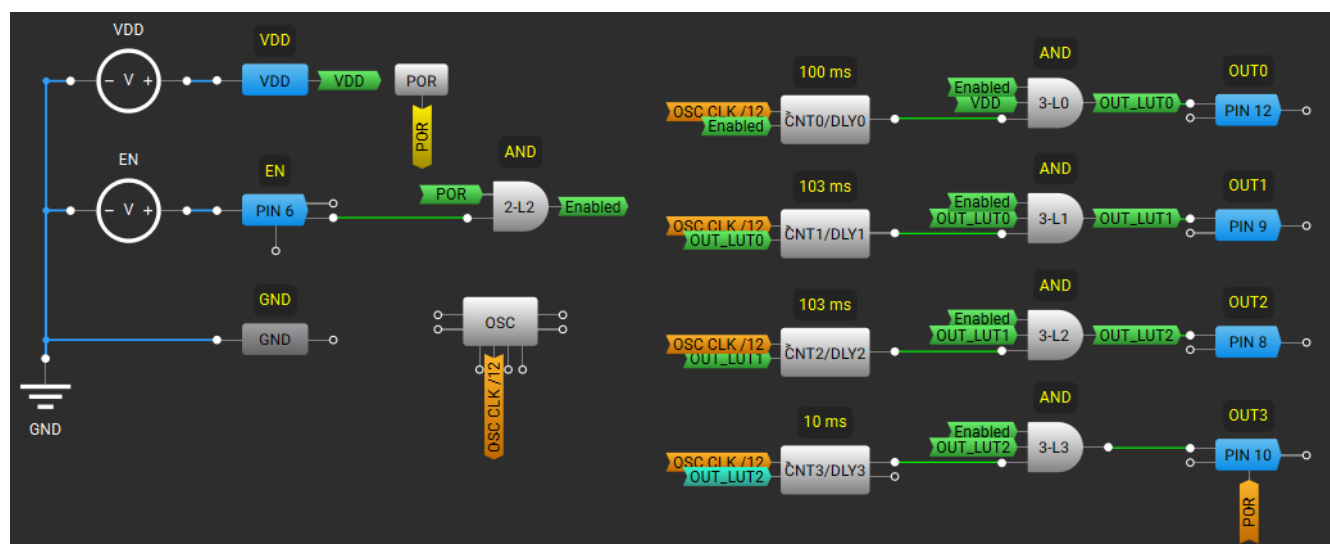


Figure 1. Power up sequencer block diagram

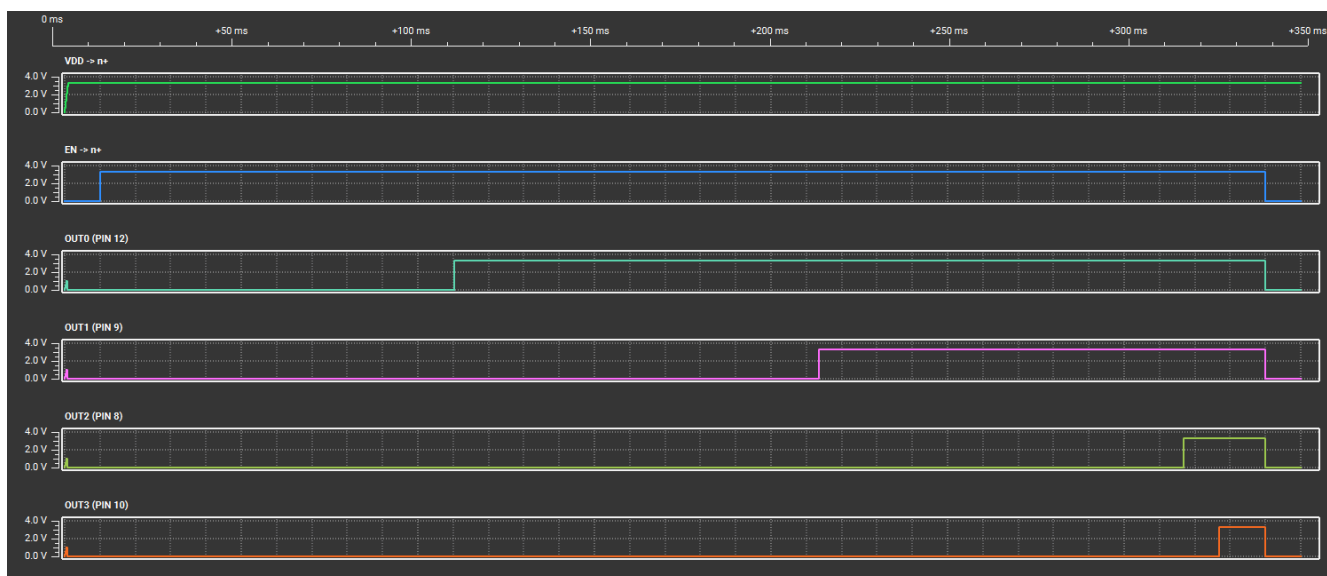


Figure 2. Power up sequencing waveform

5. Design 2: Power UP and Power DOWN Sequencing

In addition to power up sequence, power down sequence can also be realized as shown in Figure 3. Comparing with Figure 1, notice how the wirings have changed slightly in Figure 3. When EN is high, the LUTs make sure an output turns high with some delay only after the previous rail turns high. When EN is low, these LUTs make sure an output turns low with some delay only after the previous rail turns low. The timing waveform is shown in Figure 4. The logic states of the LUTs used are shown in the appendix.

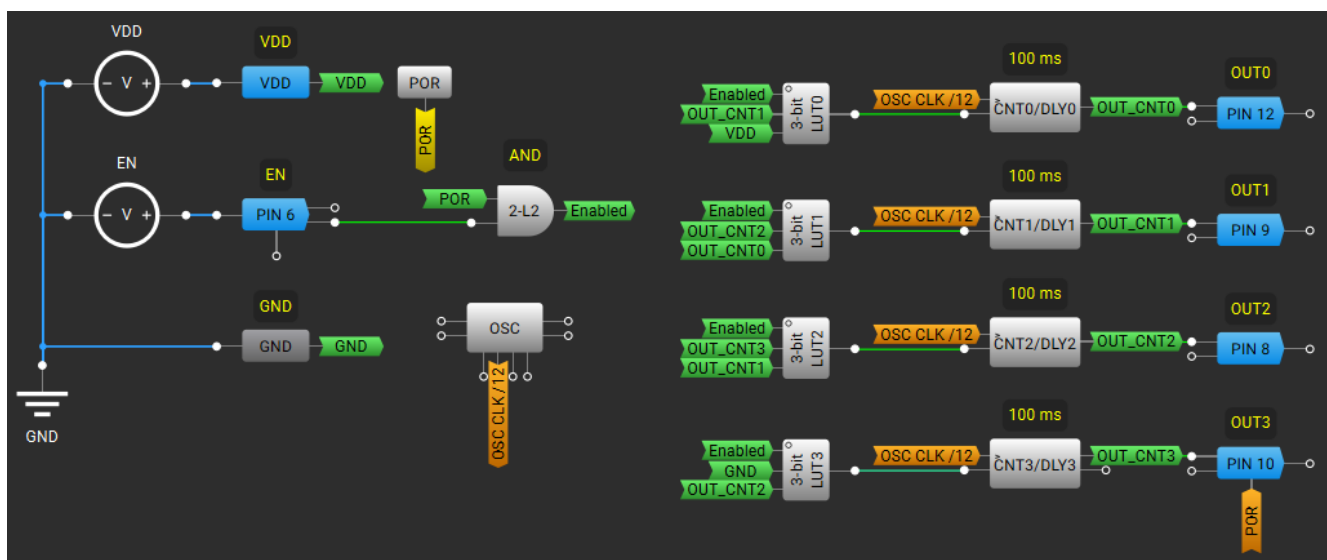


Figure 3. Power up and down sequencer block diagram

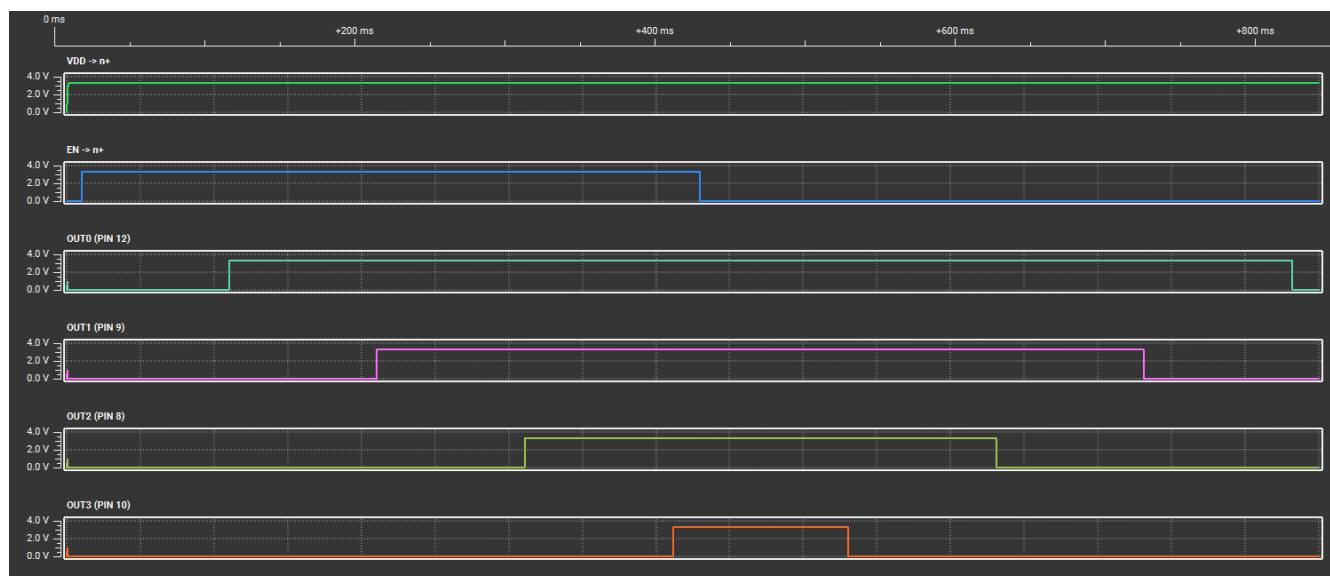


Figure 4. Power sequence up and down waveform

6. Design 3: Sequencing with PG indicator

Often times the outputs of a sequencer are used to enable individual DCDC converters, which turn on different cores inside a processor at different times. Sometimes these DCDC converters have an unknown amount of turn on time, so the sequencer needs a PG signal from the converters before enabling the next converter. Figure 5 shows a modified power up and down sequencer with PG input. Now an output needs to wait for a PG signal from a previous rail's converter before going high. The timing waveform is shown in Figure 7.



Figure 5. Power up and down sequencer with PG input block diagram

4 Channel Power Up/Down Sequencer Using GreenPAK

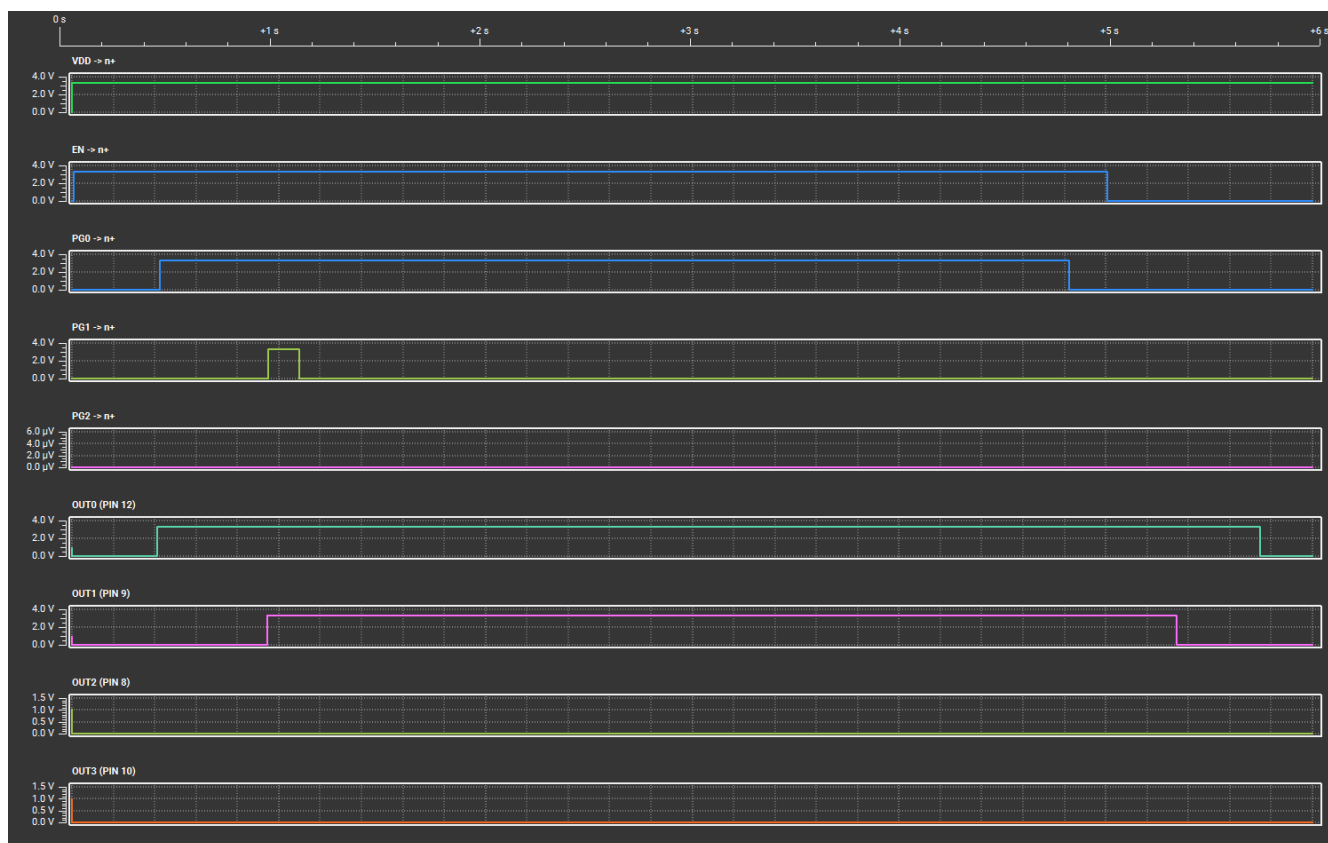


Figure 6. Power up and down sequencer with PG waveform, EN held high

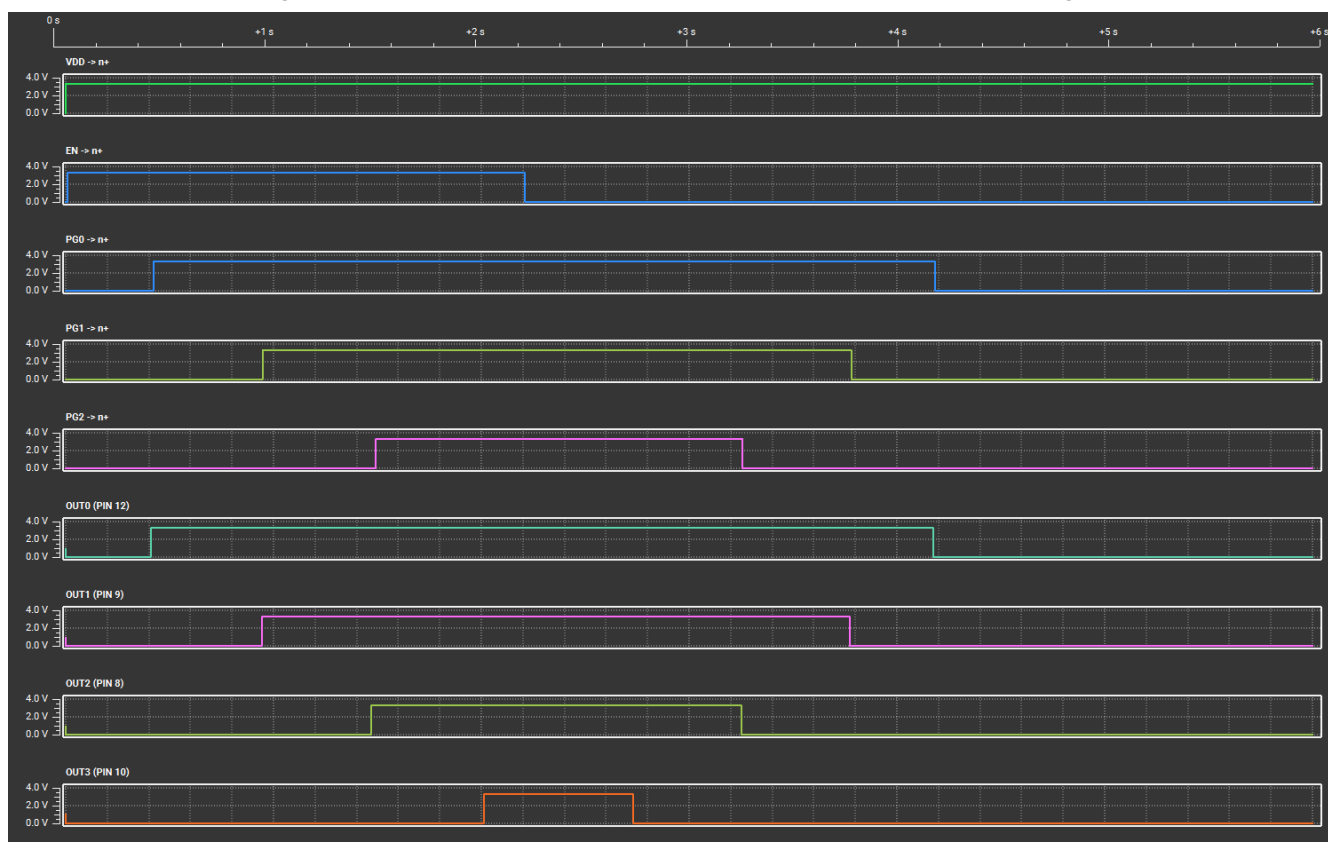


Figure 7. Power up and down sequencer with PG waveform, short EN pulse

7. Conclusion

This application note demonstrates how the SLG46110 GreenPAK can implement a complete 4-channel power up/down sequencer. With programmable mixed-signal ASIC technology, the SLG46110 provides delay macro cells and LUTs that enable highly flexible sequencing logic in a compact, low-cost package.

The SLG46110-based programmable mixed-signal ASICs have the ability to not only sequence, monitor, and supervise power rails but also daisy-chain to each other to multiply the number of rails controlled. The three designs presented here — power-up-only, power-up-and-down, and PG-indicator-based sequencing — cover the most common sequencing scenarios found in modern multi-rail processor designs.

8. Revision History

Revision	Date	Description
2.00	May 29, 2026	Changed the base part number
1.00	May 20, 2015	Initial release.

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