I2C Expander
SLG46537

The application note gives step-by-step guidelines for creating a I2C IO Controllers 8-bit BUS.

The application note comes complete with design files which can be found in the Reference section.

Contents

Figures

1. Terms and Definitions

IC	Integrated Circuit
GPIO	General-Purpose Input/Output
LUT	Look-up Table
MCU	Microcontroller Unit

2. References

For related documents and software, please visit:

GreenPAK Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics

[2] AN-1144 I2C Expander.gp, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

[5] SLG46537 Datasheet, Renesas Electronics

3. Introduction

This app note is a corollary to another app note AN-1090 Simple I2C IO Controllers with SLG46537V. AN-1090 explains how to make I2C IO Controllers with separate input and output pins. However, this app note will explain how to setup an 8-bit bus controller which combines input pins with output pins. Refer to Figure 1 for the System Level View.

4. Digital Input/Output and OE

To combine inputs with outputs, each pin interfacing the bus is set to 'Digital Input/Output'. Only 9 GPIOs in the SLG46537V are 'Digital Input/Output' capable and we will be using 8 of those pins: PINs #19, 18, 16, 14,13, 7, 5, 3. Each of these pins have an OE signal that toggles the mode. Set the properties as shown in Figure 3 and setup the matrix connections as shown in Figure 2.

Each output signal is controlled by an I2C Virtual Input. OE is controlled by 2-bit LUT0. The inputs to the 2-bit LUT0 are both gnd. Therefore, if the LUT is configured as in Figure 4, then OE will be logic 1. If the LUT is configured as in Figure 5, then OE will be logic 0. We will be using I2C to change the LUT configuration on the fly.

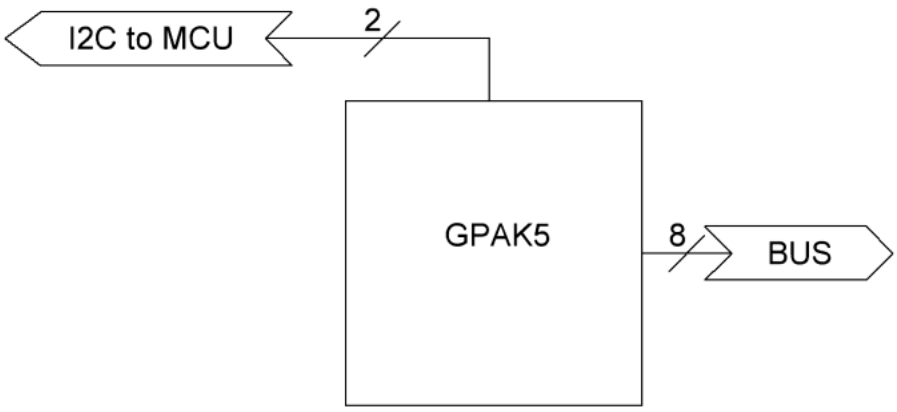

Figure 1. System Level View

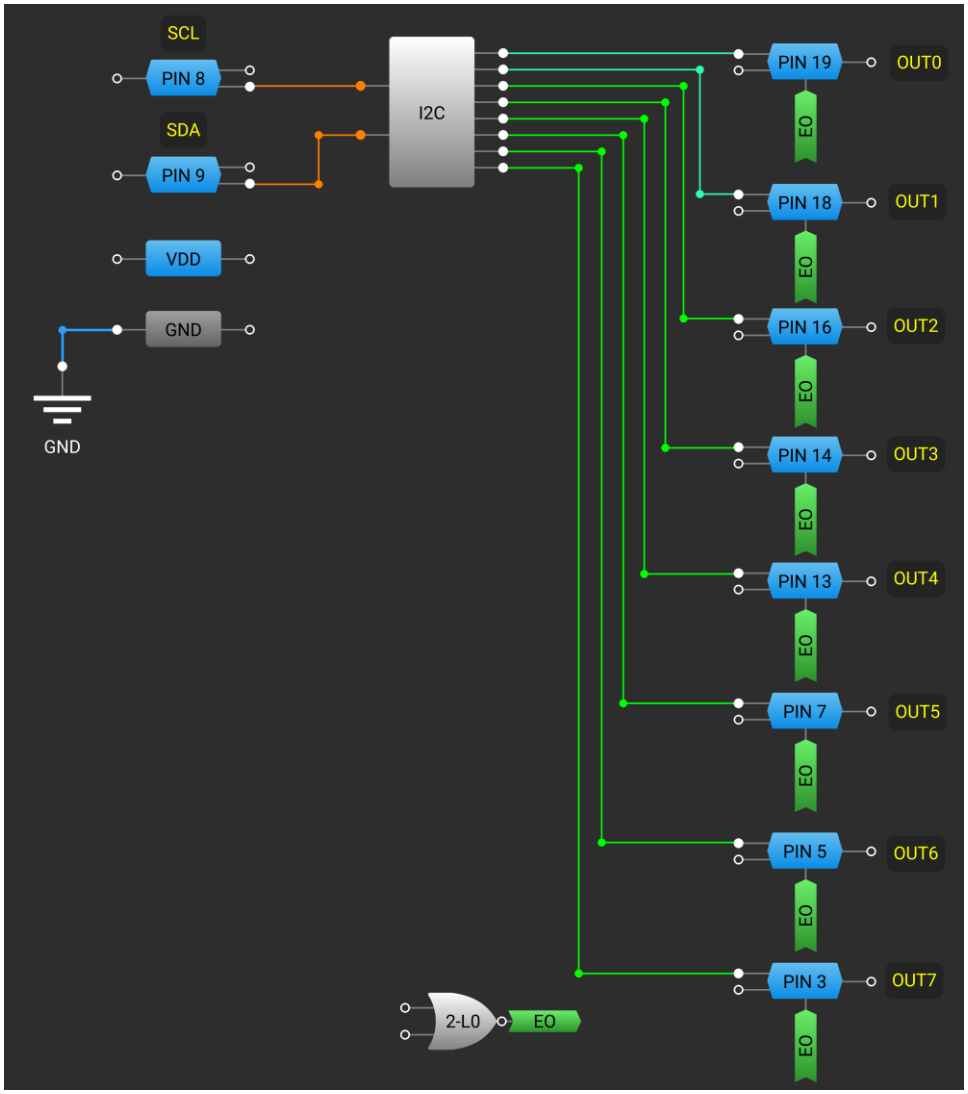

Figure 2. GreenPAK Design

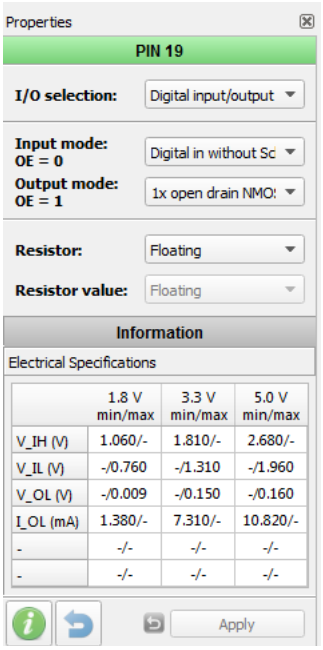

Figure 3. PIN Configuration

IN1	IN0	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Figure 4. 2-LUT0 Configuration, OE = 1 (output pin mode)

IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	0

Figure 5. 2-LUT0 Configuration, OE = 0 (input pin mode)

5. I2C Bus Write

To write the bus, the MCU must send 2 commands: first write to the I2C Virtual Inputs, then set OE = 1 by re-configuring 2-bit LUT0:

i) **W: I2C Virtual Inputs**, write to address 0xF4. Each bit corresponds to an I2C Virtual Input. The order from left to right is PINs #19, 18, 16, 14, 13, 7, 5 and 3.

0xF4	0	0	0	0	0	0	0	0

0xF4	1	1	1	1	1	1	1	1

ii) **W: 2-bit LUT0**, write to the second nibble of address 0x96 with the byte value 0x8. To mask the first nibble, read the byte and change only the latter four bits.

0x96	X	X	X	X	1	0	0	0

6. I2C Bus Read

To read from the bus, the MCU must send 2 commands: first set OE = 0 by reconfiguring 2-bit LUT0, then read from the GPIO Input Levels.

i) **W: 2-bit LUT0**, write to the second nibble of address 0x96 with the byte value 0x0. To mask the first nibble, read the byte and change only the latter four bits.

0x96	X	X	X	X	0	0	0	0

ii) **R: Input levels**, read from address 0xF0 and 0xF6 the input levels of PIN#3, 5, 7 and PIN#13, 14, 16, 18, 19 respectively. Then parse the data based on bit location.

0xF0	X	X	PIN3	X	PIN5	X	PIN7	X

0xF6	X	PIN13	PIN14	X	PIN16	0	PIN18	PIN19

7. Warning

The following warning can be ignored because 2- bit LUT0 inputs are intentionally left static, and the truth table will be re-configured through I2C.

Time	Event	Rule	Note
14:27:21	Fail	2-bit LUT0/DFF/LATCH0: The truth table is configured incorrectly.	The truth table is configured so that all combinations of the inputs that are connected to the blocks, do not cause changes on the output.
14:27:21	Warning	2-bit LUT0/DFF/LATCH0: No input connected.	2-bit LUT0/DFF/LATCH0's input is not connected.

Figure 6. Warnings and Rules Checker

8. Examples I2C Commands

The output of each example is shown in Figure 7 through 10, which are screenshots from the I2C Tool.

Emulation

Each Digital IO pin has a pull-up active-low button. Enable I2C Tools after Emulation.

Syntax**: [** is the start bit, **]** is the stop bit, and **SA** is the slave address with a r/w bit.

i) I2C write to I2C Virtual Inputs the logic 0, 0, 0, 1, 0, 1, 1, 1.

[SA 0xF4, 0xE8 **]**

ii) I2C write 2-bit LUT0 configuration to 1, 0, 0, 0:

[SA 0x96 0x08 **]**

iii) I2C write 2-bit LUT0 configuration to 0, 0, 0, 0:

[SA 0x96 0x00 **]**

iv) I2C Read the input levels from PINs #7, 5 and 3 and also #19, 18, 16, 14 and 13:

[SA 0xF0 **[** 0xSA read **]**

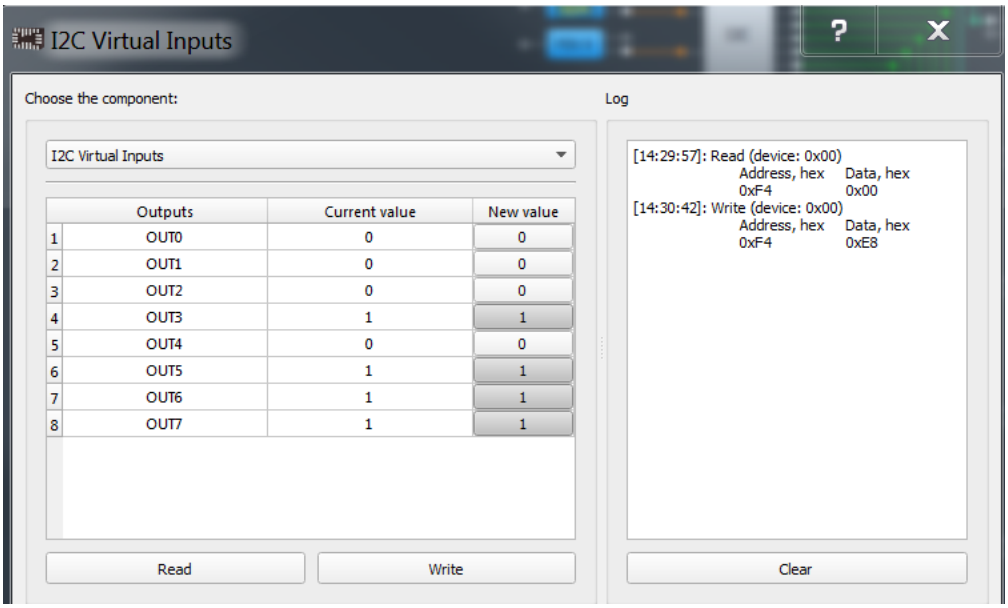

Figure 7. Example i

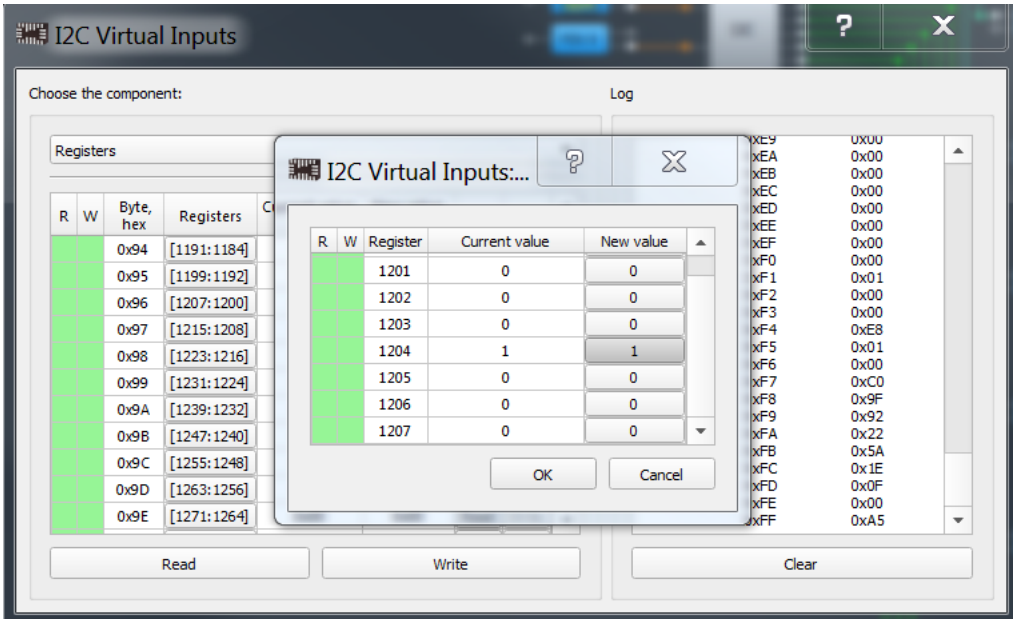

Figure 8. Example ii

v) I2C write 2-bit LUT0 configuration to 0, 0, 0, 0:

[SA 0x96 0x00]

vi) I2C Read the input levels f rom PINs #7, 5 and 3 and also #19, 18, 16, 14 and 13:

[SA 0xF0 [0xSA read]

[SA 0xF6 [0xSA read]

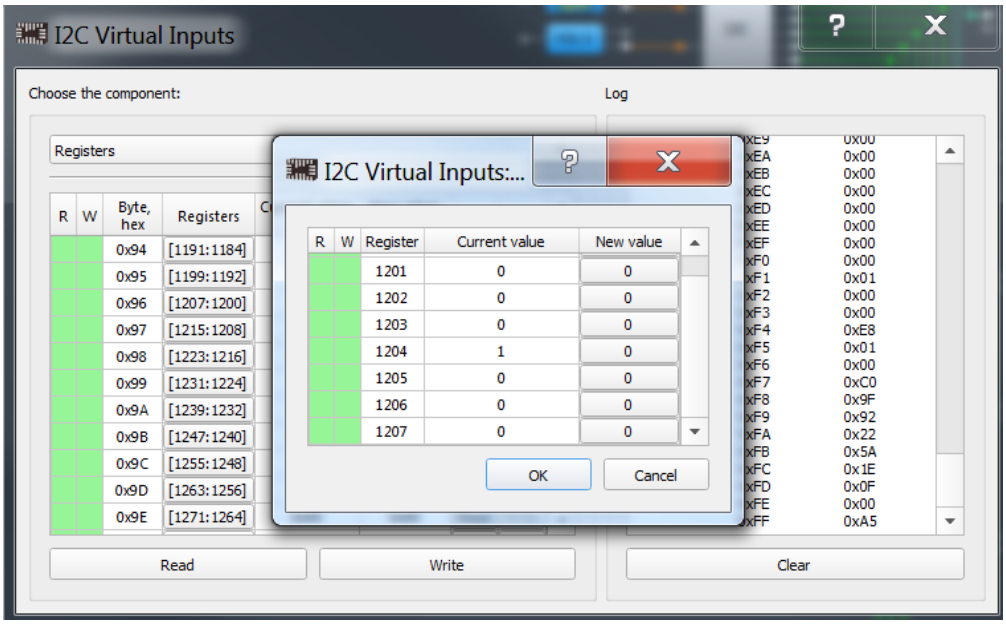

Figure 9. Example iii

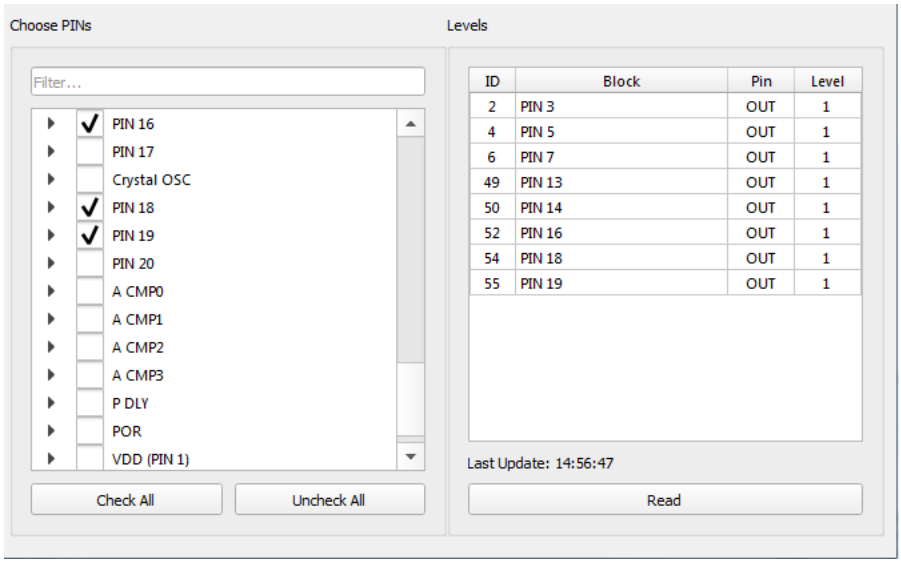

Figure 10. Example iv

9. Conclusion

By the end of this app note, you should be able to make a GreenPAK Design and the I2C Commands. Unlike AN-1090, this design uses less GPIOs at the expense of more I2C commands.

10. Revision History

Revision	Date	Description
1.00	Sep 19, 2016	Initial release.
2.00	May 5, 2026	The part number has been changed from SLG46531V to SLG46537V.

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