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瑞萨电子公司

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H8/300L SLP 系列

通过 16 位定时器计数器功能进行中断次数的计数

要点

进行定时器 F 中断次数的计数，在进行了 50 次的中断计数时程序结束。设定为每隔定时器计数器 F (TCF) 溢出的时间 52.429ms 发生一次定时器 F 中断。

动作确认器件

H8/38024

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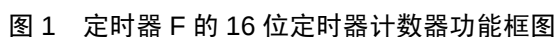
1. 规格

- (1) 使用定时器 F 的 16 位定时器计数器功能，进行定时器 F 中断次数的计数，在进行了 50 次的中断计数时程序结束。
- (2) 通过定时器计数器 F (TCF) 溢出，发生使用定时器 F 溢出的中断请求，在定时器 F 中断处理中使设定在 RAM 中的 8 位计数器进行递减。
- (3) 设定在 RAM 中的 8 位计数器在定时器 F 中断处理中进行减量。然后，在进行了 50 次的定时器 F 中断计数时禁止定时器 F 中断请求，并且结束程序的执行。
- (4) 定时器 F 中断设定为定时器计数器 F (TCF) 溢出时间每隔 52.429ms 发生一次。

2. 使用功能说明

- (1) 在本例子中，使用定时器 F 的 16 位定时器计数器功能，进行定时器 F 中断次数的计数。
 - (a) 定时器 F 的 16 位定时器计数器功能框图如图 1 所示。以下说明有关定时器 F 的 16 位定时器计数器功能框图。
 - 系统时钟 (φ) 为 5MHz，是 CPU 和外围功能运行的基准时钟。
 - 预定标器 S (PSS) 是以 φ 为输入的 13 位计数器，按每个周期进行一次累加计数。
 - 定时器计数器 F (TCF) 是 16 位可读写的递增计数器，由输入的内部时钟/外部时钟进行累加计数。输入时钟可选择系统时钟的 4 分频、16 分频、32 分频以及外部时钟的 4 种时钟。在本例子中，TCF 的输入时钟选择系统时钟的 4 分频。
 - 定时器控制寄存器 F (TCRF) 是 8 位可读写的寄存器，进行 16 位模式和 8 位模式的转换、4 种内部时钟和外部事件的选择、TMOFH 和 TMOFL 管脚输出电平的设定。
 - 定时器控制状态寄存器 F (TCSR) 是 8 位寄存器，进行寄存器清除的选择、溢出标志的置位、比较匹配标志的置位、由溢出的中断请求允许的控制。
 - 以下表示本例子中定时器计数器 F (TCF) 的溢出周期的计算方法。

$$\begin{aligned}
 \text{TCF 溢出周期} &= \frac{1}{\text{系统时钟}/4\text{分频}} \times 65536 \\
 &= \frac{1}{5\text{MHz}/4\text{分频}} \times 65536 \\
 &= 52.429 \text{ ms}
 \end{aligned}$$



(2) 本例子的功能分配如表 1 所示。分配如表 1 所示的功能，通过定时器 F 16 位定时器计数器功能进行中断次数的计数。

表 1 功能分配

功能	功能分配
PSS	将系统时钟作为输入的 13 位递增计数器
TCRF	选择 TCF 的输入时钟
TCSRf	允许 TCF 溢出中断，选择 TCF 的清除方法
TCFH,TCFL	以系统时钟的 4 分频为时钟输入的 16 位计数器
IENTFH	允许定时器 FH 溢出的中断请求
IRRTFH	定时器 FH 溢出的中断标志
counter_sub	对定时器 F 中断次数进行 50 次计数的 8 位计数器

3. 运行说明

(1) 运行说明如图 2 所示。根据如图 2 所示的硬件处理和软件处理，使用定时器 F 的 16 位定时器计数器功能进行中断次数的计数。

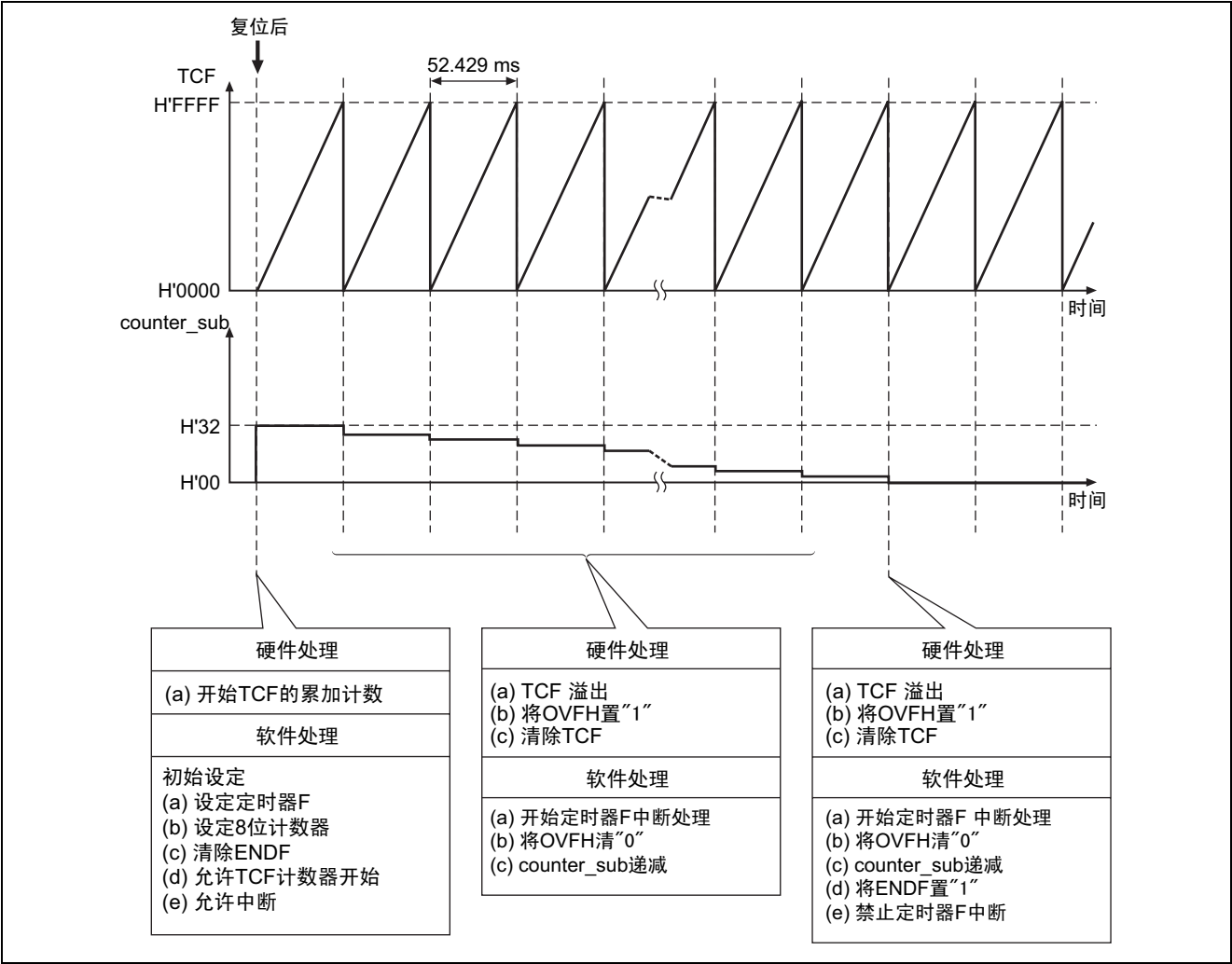


图 2 通过定时器 F 的 16 位定时器计数器功能进行中断次数计数的运行说明

4. 软件说明

- (1) 模块说明
- 本例子的模块如表 2 所示。

表 2 模块说明

模块名	标号名	功能
主程序	main	设定定时器 F 的 16 位定时器计数器功能，设定 8 位计数器，允许中断，设定 TCF 计数器的开始，并且在 ENDF 被置"1"时程序结束
中断计数	tfint	在定时器 F 中断处理中，进行 8 位计数器的递减，在计数器值为 H'00 时将 ENDF 置"1"，禁止定时器 F 中断

- (2) 参数说明
- 本例子不使用参数。

(3) 使用内部寄存器的说明

本例子使用的内部寄存器如表 3 所示。

表 3 使用内部寄存器的说明

寄存器名		功能	地址	设定值
TCRF	CKSH2 CKSH1 CKSH0	定时器控制寄存器 F（时钟选择 H） ：如果设定为 CKSH2=0、CKSH1=0、CKSH0=0 或者 CKSH2=0、CKSH1=0、CKSH0=1 或者 CKSH2=0、 CKSH1=1、CKSH0=0，TCF 就作为 16 位计数器运行	H'FFB6 位 6 位 5 位 4	CKSH2=0 CKSH1=0 CKSH0=0
	CKSL2 CKSL1 CKSL0	定时器控制寄存器 F（时钟选择 L） ：CKSL2=1、CKSL1=1，CKSL0=0 时，TCF 对系统时钟的 4 分频进行计数	H'FFB6 位 2 位 1 位 0	CKSL2=1 CKSL1=1 CKSL0=0
TCSR	OVFH	定时器控制状态寄存器 F （定时器溢出标志 H） ：OVFH=0 时，TCF 没溢出 ：OVFH=1 时，TCF 溢出	H'FFB7 位 7	0
	CMFH	定时器控制状态寄存器 F （比较匹配标志 H） ：CMFH=0 时，不发生比较匹配 F ：CMFH=1 时，发生比较匹配 F	H'FFB7 位 6	0
	OVIEH	定时器控制状态寄存器 F （定时器溢出中断允许 H） ：OVIEH=1 时，允许 TCF 溢出的中断请求	H'FFB7 位 5	1
	CCLR	定时器控制状态寄存器 F （计数器清除 H） ：CCLR=0 时，禁止由比较匹配清除 TCF	H'FFB7 位 4	0
TCF		定时器计数器 F ：将系统时钟的 4 分频作为输入的 16 位递增计数器	H'FFB8	H'0000
IENR2	IENR2H	中断允许寄存器 2（定时器 FH 中断允许） ：IENR2H=0 时，禁止定时器 FH 中断请求 ：IENR2H=1 时，允许定时器 FH 中断请求	H'FFF4 位 3	1
IRR2	IRR2H	中断请求寄存器 2（定时器 FH 中断请求标志） ：IRR2H=0 时，没发生定时器 FH 中断请求 ：IRR2H=1 时，发生定时器 FH 中断请求	H'FFF7 位 3	0

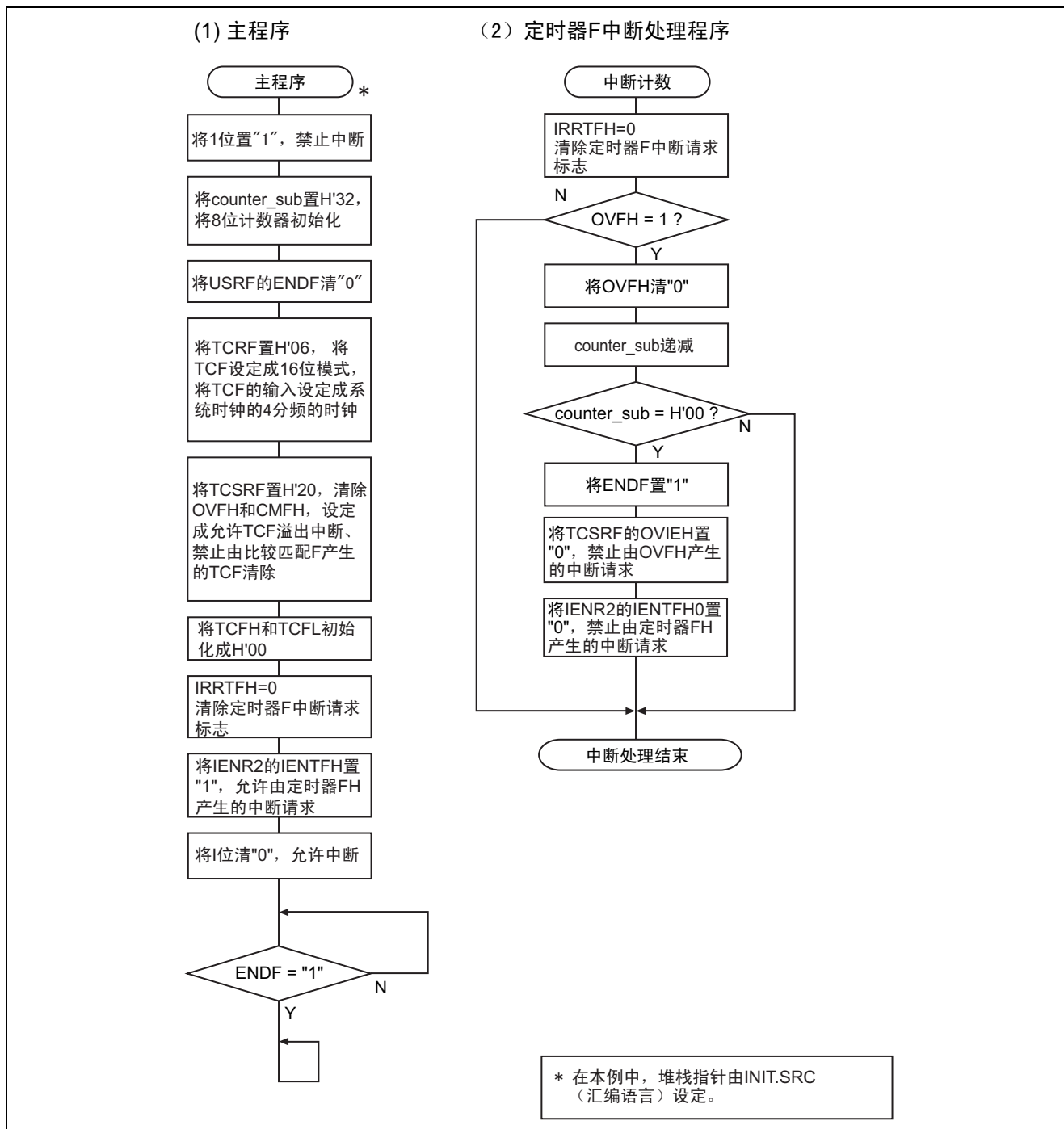
(4) 使用 RAM 的说明

本例子使用的 RAM 如表 4 所示。

表 4 使用 RAM 说明

标号名		功能	地址	使用模块名
counter_sub		8 位计数器	H'FB80	主程序 中断计数
USRF	ENDF	判断 8 位计数器的计数器值是否为 H'00 的标志	H'FB81 位 0	主程序 中断计数

5. 流程图



6. 程序清单

6.1 INIT.SRC (程序清单)

```

        .EXPORT  _INIT
        .IMPORT  _main
;
        .SECTION P, CODE
_INIT:
        MOV.W    #H'FF80, R7
        LDC.B    #B'10000000, CCR
        JMP      @_main
;
        .END

```

```

/*****
/*
/*
/* H8/300L Super Low Power Series
/*      -H8/38024 Series-
/*      Application Note
/*
/* 'Interrupt Counting by 16-bit Timer Counter
/*      Function'
/*
/*      Function
/*      : Timer F 16bit Timer Counter
/*
/*      External Clock : 10MHz
/*      Internal Clock : 5MHz
/*      Sub Clock      : 32.768kHz
/*
*****/

```

```

#include    <machine.h>

/*****
/*      Symbol Definition
*****/
struct BIT {
    unsigned char    b7:1;    /* bit7 */
    unsigned char    b6:1;    /* bit6 */
    unsigned char    b5:1;    /* bit5 */
    unsigned char    b4:1;    /* bit4 */
    unsigned char    b3:1;    /* bit3 */
    unsigned char    b2:1;    /* bit2 */
    unsigned char    b1:1;    /* bit1 */
    unsigned char    b0:1;    /* bit0 */
};

#define    TCRF        *(volatile unsigned char *)0xFFB6    /* Timer Control Register F */
#define    TCRF_BIT    (*(struct BIT *)0xFFB6)    /* Timer Control Register F */
#define    TOLH        TCRF_BIT.b7    /* Toggle Output Level F */
#define    CKSH2        TCRF_BIT.b6    /* Clock Select H2 */
#define    CKSH1        TCRF_BIT.b5    /* Clock Select H1 */
#define    CKSH0        TCRF_BIT.b4    /* Clock Select H0 */
#define    TCSRFB        *(volatile unsigned char *)0xFFB7    /* Timer Control Status Register F */
#define    TCSRFB_BIT    (*(struct BIT *)0xFFB7)    /* Timer Control Status Register F */

```

```
#define OVFH      TCSR_F_BIT.b7      /* Timer Overflow Flag H      */
#define CMFH      TCSR_F_BIT.b6      /* Compare Match Flag H      */
#define OVIEH     TCSR_F_BIT.b5      /* Timer Overflow Interrupt Enable */
#define CCLR_H    TCSR_F_BIT.b4      /* Output Select 3          */
#define OCR_FL    *(volatile unsigned char *)0xFFB8 /* Output Compare Register FL */
#define TCFH      *(volatile unsigned char *)0xFFB8 /* Timer Counter FL          */
#define TCFL      *(volatile unsigned char *)0xFFB9 /* Timer Counter FL          */
#define IENR2     *(volatile unsigned char *)0xFFF4 /* Interrupt Enable Register 2 */
#define IENR2_BIT (*(struct BIT *)0xFFF4) /* Interrupt Enable Register 2 */
#define IENTFH    IENR2_BIT.b3      /* Timer FH Interrupt Enable   */
#define IENTFL    IENR2_BIT.b2      /* Timer FH Interrupt Enable   */
#define IRR2_BIT  (*(struct BIT *)0xFFF7) /* Interrupt Request Register 2 */
#define IRRF_H    IRR2_BIT.b3      /* Timer FH Interrupt Request Flag */
#define IRRF_L    IRR2_BIT.b2      /* Timer FH Interrupt Request Flag */

#pragma interrupt (tfint)
/*****
/* Function define
*****/
extern void INIT ( void ); /* SP Set
void      main ( void );
void      tfint ( void );

/*****
/* RAM define
*****/
unsigned char counter_sub;
unsigned char USRF; /* User Flag Area

#define USRF_BIT (*(struct BIT *)&USRF)
#define ENDF     USRF_BIT.b0 /* End Flag

/*****
/* Vector Address
*****/
#pragma section V1 /* VECTOR SECT0IN SET
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT /* 00 Reset
};
#pragma section V2 /* VECTOR SECT0IN SET
void (*const VEC_TBL2[])(void) = {
    tfint /* 1E Timer F Interrupt
};

#pragma section /* P
/*****
/* Main Program
*****/
void main ( void )
{
    set_imask_ccr(1); /* Interrupt Disable

    counter_sub = 0x32; /* Initialize 8bit Counter_sub
    ENDF = 0; /* Initialize ENDF
```

```

TCRF = 0x06; /* Initialize Clock Select */
TCSRF = 0x20; /* Initialize Overflow Interrupt */

TCFH = 0x00; /* Clear Timer CounterF */
TCFL = 0x00; /* Clear Timer CounterF */

IRRTFH = 0;
IENTFH = 1;

set_imask_ccr(0); /* Interrupt Enable */

while(ENDF != 1){ /* ENDF = 1 ? */
    ;
}

while(1){
    ;
}
}

/*****
/* Timer F Interrupt */
*****/
void tfint ( void )
{
    IRRTFH = 0;

    if ( OVFH == 1 ){
        OVFH = 0; /* Clear OVFH */
        counter_sub--; /* Decrement 8bit Counter */

        if ( counter_sub == 0x00 ){
            /* 8bit Counter != H'00 */
            ENDF = 1; /* Set ENDF */
            OVIEH = 0;
            IENTFH = 0;
        }
    }
}
}

```

连接地址指定

段名	地址
CV1	H'0000
CV2	H'001E
P	H'0100
B	H'FB80

修订记录

Rev.	发行日	修订内容	
		页	修订要点
1.00	2005.09.14	—	初版发行

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