49FCT3805D Jitter Performance

This application note describes the tests used to observe and compare the jitter performance when different frequencies are used at the A and B banks of the Renesas 49FCT3805D device and the clock buffer FCT3805D (Vendor A).

Contents

1. Overview

The 49FCT3805D is composed of two banks, A and B. Each bank has five outputs and its own output enable control.

The purpose of this test is to observe the jitter when different frequencies are used at the two banks, A and B, of the clock buffer FCT3805D. It also provides the jitter performance comparison of Vendor A's FCT3805D and Renesas' 49FCT3805D devices.

2. Test Method

The Lecroy WaveMaster 8600A, HP81130A and HP 81133A pulse generators were used in this test. Both test setup block diagrams are shown in Figure 1 and Figure 2. The HP81133A was used to generate two synchronous 66MHz and 33MHz clocks to banks A and B. The output A1 and B1 were then brought to the Lecroy scope for the period jitter test.

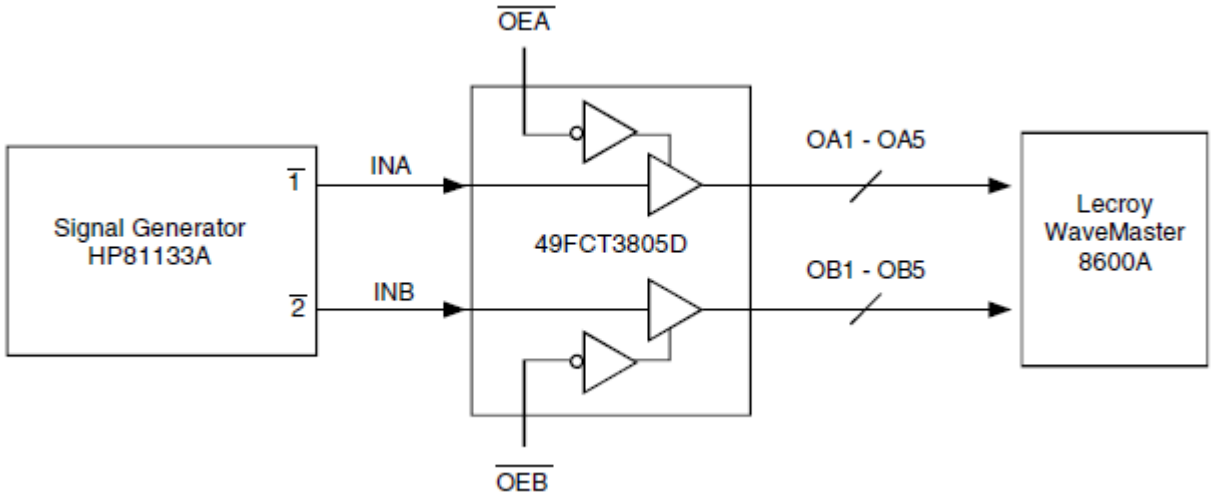

Figure 1. Test Set-up for Synchronous Input Clock on Bank A and B

In the second setup, two pulse generators HP81130A and HP81133A were used separately as the input sources for bank A and B. This was the asynchronous output jitter test.

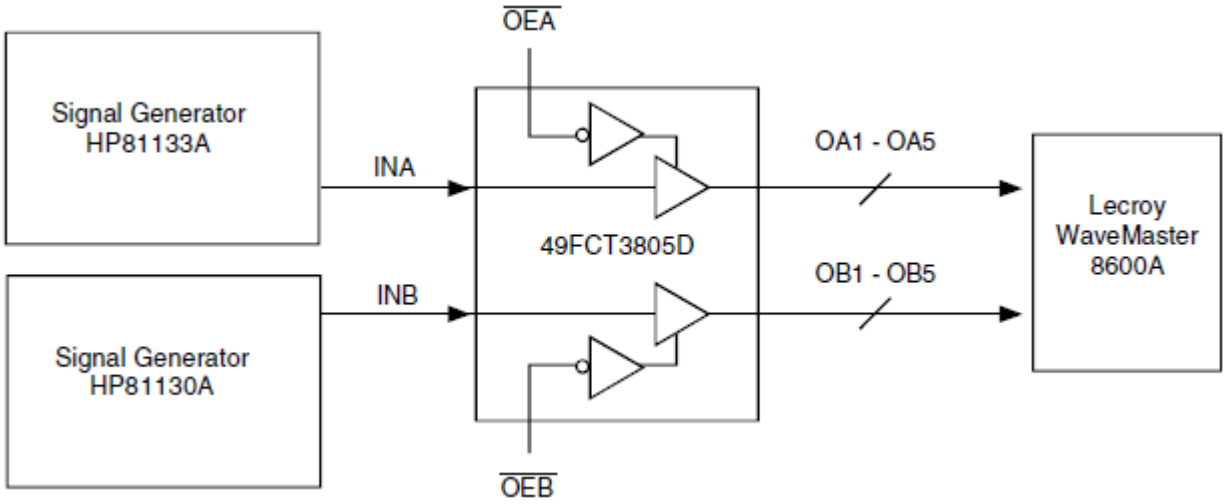

Figure 2. Test Set-up for Asynchronous Input Clock on Bank A and B

3. Test Results

The input jitter of both Vendor A's FCT3805D and the Renesas 49FCT3805D are similar. Under the same input conditions, the Vendor A part has more output period jitter compared to the Renesas part. The results of the synchronous test (using input frequencies, 66MHz and 33MHz) are shown in the following Input and Output Period Jitter of Two Synchronous Clocks table. Note that for the Renesas part, the peak-to-peak period jitter on bank A and bank B are different by about 50ps.

3.1 Input and Output Period Jitter of Two Synchronous Clocks

	Peak-to-Peak Period Jitter of the Synchronous Clock Output	
Frequency (I/O)	**Vendor A's FCT3805D**	**Renesas 49FCT3805D**
66MHz Input INA	64.5ps	66.5ps
33MHz Input INB	67.5ps	63ps
66MHz Output OA1	303ps	244ps
33MHz Output OB1	229.5ps	187.5ps

In the second test, two clock sources from HP81133A and HP81130A were used to provide asynchronous inputs at 66MHz and 33MHz to both parts. As shown in the following Output Period Jitter of Two Asynchronous Clocks table, the jitter at OA1 increased by a factor of 3–4, as compared to the synchronous clock test results shown in the Input and Output Period Jitter of Two Synchronous Clocks table. The period jitter of Vendor A's FCT3805D (measured at the output A1) was 999.5ps, as compared to only 788.5ps for the Renesas 49FCT3805D.

When the two pulse generators were switched to the same frequency (66MHz), the peak-to-peak period jitter of the two banks A1 and B1 went down to the ranges seen in the synchronous source test.

3.2 Output Period Jitter of Two Asynchronous Clocks

	Peak-to-Peak Period Jitter of the Asynchronous Clock Output	
Frequency (Output)	**Vendor A's FCT3805D**	**Renesas 49FCT3805D**
66MHz Output OA1	999.5ps	788.5ps
33MHz Output OB1	227ps	195.5ps
66MHz Output OA1 (same frequency as OB1)	210.5ps	275ps
66MHz Output OB1 (same frequency as OA1)	257.5ps	193.3ps

A third test was performed with the same setup as the asynchronous test described previously. However, this time the lower frequency input was routed to bank A and the higher frequency input was routed to bank B. The Output Period Jitter of Two Asynchronous Clocks (Swapped) table below shows the results. Notice that the results were much improved for both banks on the IDT device as compared to the results in the Output Period Jitter of Two Asynchronous Clocks table. Notice also that the output with the higher frequency always has higher jitter. In the case of the IDT device, providing the higher frequency to bank B dramatically improved the jitter performance of both banks.

3.3 Output Period Jitter of Two Asynchronous Clocks (Swapped)

	Peak-to-Peak Period Jitter of the Asynchronous Clock Output [1]	
Frequency (Output)	**Vendor A's FCT3805D**	**Renesas 49FCT3805D**
33MHz Output OA1	178ps	189.5ps
66MHz Output OB1	1.017ns	284ps

1. The inputs of the Output Period Jitter of Two Asynchronous Clocks table are swapped.

The final test was performed with two clock sources from HP81133A and HP81130A running at 66MHz. This provided two asynchronous inputs to the 49FCT3805D. The peak-to-peak period jitter was measured on one bank with the other bank disabled. The purpose of this test was to determine the source of the additional jitter as noted in the previous tests. As noted in the table, the output jitter was significantly improved; the device only adds a few picoseconds of jitter to the input clock.

3.4 Output Period Jitter of Clock Output

(Two asynchronous inputs and other output bank disabled)

	Peak-to-Peak Period Jitter of the Clock Output
Frequency (Output)	**Renesas 49FCT3805D**
66MHz Input	69ps
66MHz Output OA1 (bank B disabled)	65ps
66MHz Output OB1 (bank A disabled)	67ps

4. Conclusion

The frequency of the two inputs to the part has a huge impact on the jitter performance at the outputs. When two synchronous inputs, each operating at a different frequency, were provided, there was approximately a 1.3 times difference between the jitter measured at one bank versus that measured at the other bank (Input and Output Period Jitter of Two Synchronous Clocks table). However, if the output bank was disabled, the running outputs only added a few picoseconds of jitter to the input clock. This suggests that the coupling between the two channels is a major contributor to the device's output jitter.

If asynchronous sources were used, and the frequencies were the same, the jitter remained at approximately 1.3 times different between the two banks. If two asynchronous sources were used, each operating at a different frequency, and the higher frequency input was provided to the sensitive bank (bank A), the jitter of one bank was more than three times that of the other bank (Output Period Jitter of Two Asynchronous Clocks table). However, if two asynchronous sources were used, each operating at a different frequency, and the higher frequency input was provided to the less sensitive bank (bank B), the jitter was about 1.3 times different between the two banks (Output Period Jitter of Two Asynchronous Clocks (Swapped) table). In all four tests, however, the Renesas 49FCT3805D had better jitter performance than Vendor A's FCT3805D.

5. Revision History

Revision	Date	Description
1.00	Nov 12, 2021	Rebranded and reformatted application note with the latest template.

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