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April 1st, 2010
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Application Notes

8

38K0 Group

USB Application Notes

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- **About '38K0 Group USB Application Notes'**

  *Explicit samples for 38K0 Group USB implementation

  *Programs listed in these notes are examples and should be modified according to the applications

- **Related Materials**

  *RENESAS Microcomputers 38K0 Group Data Sheet

  [http://www.renesas.com/en/usb]

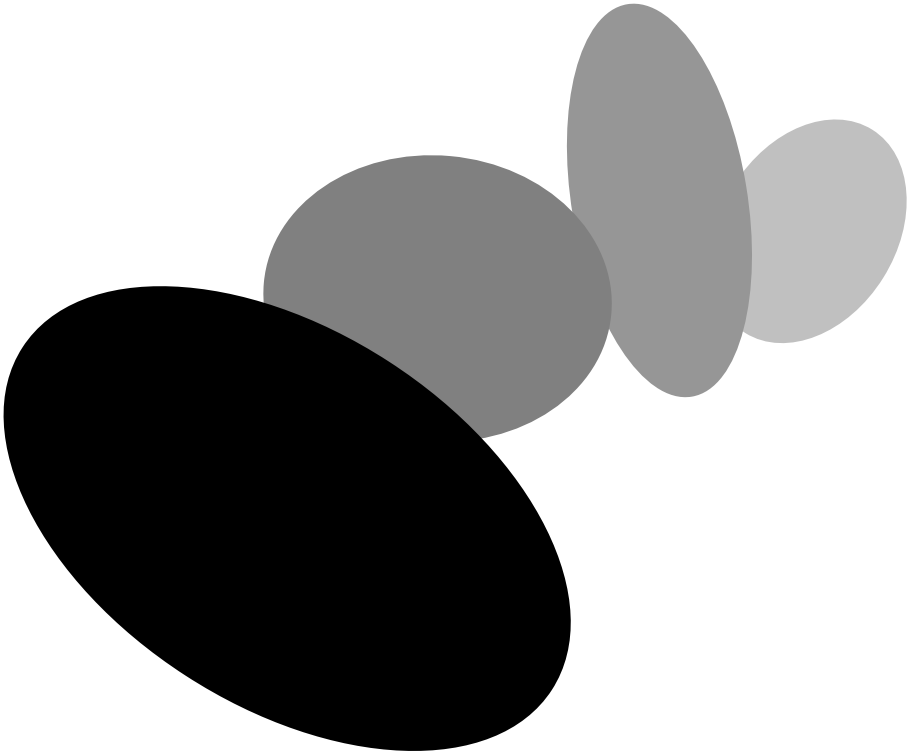
  *USB Specification Ver2.0

  [http://www.usb.org/developers/docs.html]

- **Notes on USB Communication**

  In applications requiring high-reliability, we recommend providing the system with protective measures such as USB function initialization by software or USB reset by the host to prevent USB communication from being terminated unexpectedly, for example due to external causes such as noise.

- Table of contents -



Chapter 1
USB Initial Setting

USB initialization consists of enabling the USB block and every endpoint setting of the transfer type and the interrupt configuration.

1.1.USB Function Outline

The 38K0 Group is equipped with a USB Device Control Unit (USBDCU = USB Block). The USBDCU enables highly effective interfacing with the host computer. This circuit is in compliance with USB Specification Version 2.0 and supports the following four transfer types, as defined in the specification.

- Control Transfer
  Mainly used for data transfer during setup, when the USB device is first attached (two-way transfer).

- Isochronous Transfer
  Used for transfer of relatively large quantities of data, such as voice or movie data, which requires a constant transfer rate (one-way transfer).

- Interrupt Transfer
  Used for transfer of relatively small quantities of data to be transferred in real-time, such as keyboard or mouse input (one-way transfer).

- Bulk Transfer
  Used for transfer of data that does not require real-time operations, such as printer output, etc. (one-way transfer).

The USB Device Control Unit has 4 endpoints (Endpoint 0 to 3). Endpoints 1 to 3 can be used for Isochronous, Bulk and Interrupt transfers. Endpoint 0 can only provide Control transfer.

Any data transfer is inhibited during reset on 38K0 MCUs. Initialize the necessary endpoints for the type of data transfer to be used. The USB block provides the following USB interrupts: USB bus reset interrupt, USB SOF interrupt and USB device interrupt. Make sure the USB block is in the enabled-state before using the USB function.

1.2.USB Related Registers

There are a total of 17 USB-related registers, including the index register and the register window. Nine registers are defined in one register window (same address area), which can be selected by the index register. In addition to these registers, the USBDCU has three interrupts: USB bus reset interrupt, USB SOF interrupt and USB device interrupt. See Chapter 2 for more details concerning USB interrupts.

Table 1.1 is a list of USB-related registers and Table 1.2 is a list of registers that require an index-switch.

Table 1.1. USB-Related Registers

Address	Symbol	Register Name
0010H	USBCON	USB Control Register
0011H	USBAE	USB Function Enable Register
0012H	USBA0	USB Function Address Register
0014H	FNUML	Frame Number Register LOW
0015H	FNUMH	Frame Number Register HIGH
0016H	USBICON	USB Interrupt Source Enable Register
0017H	USBIREQ	USB Interrupt Source Register
0018H	USBINDEX	Endpoint Index Register
0019H	EPXXREG1	Endpoint Field Register 1
001AH	EPXXREG2	Endpoint Field Register 2
001BH	EPXXREG3	Endpoint Field Register 3
001CH	EPXXREG4	Endpoint Field Register 4
001DH	EPXXREG5	Endpoint Field Register 5
001EH	EPXXREG6	Endpoint Field Register 6
001FH	EPXXREG7	Endpoint Field Register 7

0FECH	EPXXREG8	Endpoint Field Register 8
0FEDH	EPXXREG9	Endpoint Field Register 9

0FF8H	PLLCON	PLL Control Register

003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1

Refer to Table 1.2

Table 1.2. List of Registers Switched by Endpoint Index Register (USBINDEX)

Index Register Value	Address	Symbol	Register Name
00H	0019H	EP00STG	EP00 Status Register
	001AH	EP00CON1	EP00 Control Register 1
	001BH	EP00CON2	EP00 Control Register 2
	001CH	EP00CON3	EP00 Control Register 3
	001DH	EP00REQ	EP00 Interrupt Source Register
	001EH	EP00BYT	EP00 Byte Number Register
	001FH	-	-
	0FECH	-	-
	0FEDH	EP00BUF	EP00 Buffer Area Setup Register
01H	0019H	EP01CFG	EP01 Setup Register
	001AH	EP01CON1	EP01 Control Register 1
	001BH	EP01CON2	EP01 Control Register 2
	001CH	EP01CON3	EP01 Control Register 3
	001DH	EP01REQ	EP01 Interrupt Source Register
	001EH	EP01BYT0	EP01 Byte Number Register 0
	001FH	EP01BYT1	EP01 Byte Number Register 1
	0FECH	EP01MAX	EP01 MAX Packet Size Register
	0FEDH	EP01BUF	EP01 Buffer Area Set Register
02H	0019H	EP02CFG	EP02 Set Register
	001AH	EP02CON1	EP02 Control Register 1
	001BH	EP02CON2	EP02 Control Register 2
	001CH	EP02CON3	EP02 Control Register 3
	001DH	EP02REQ	EP02 Interrupt Source Register
	001EH	EP02BYT0	EP02 Byte Number Register 0
	001FH	EP02BYT1	EP02 Byte Number Register 1
	0FECH	EP02MAX	EP02 MAX Packet Size Register
	0FEDH	EP02BUF	EP02 Buffer Area Set Register
03H	0019H	EP03CFG	EP03 Setup Register
	001AH	EP03CON1	EP03 Control Register 1
	001BH	EP03CON2	EP03 Control Register 2
	001CH	EP03CON3	EP03 Control Register 3
	001DH	EP03REQ	EP03 Interrupt Source Register
	001EH	EP03BYT0	EP03 Byte Number Register 0
	001FH	EP03BYT1	EP03 Byte Number Register 1
	0FECH	EP03MAX	EP03 MAX Packet Size Register
	0FEDH	EP03BUF	EP03 Buffer Area Set Register

1.3.How to Use the USB Function

In order to use the USB function, enable the USB block and set the appropriate endpoints. Please refer to the 38K0 Group Data Sheet [USB Register List] for details on how to set each register.

Table 1.3 shows the list of registers that enable the USB block.

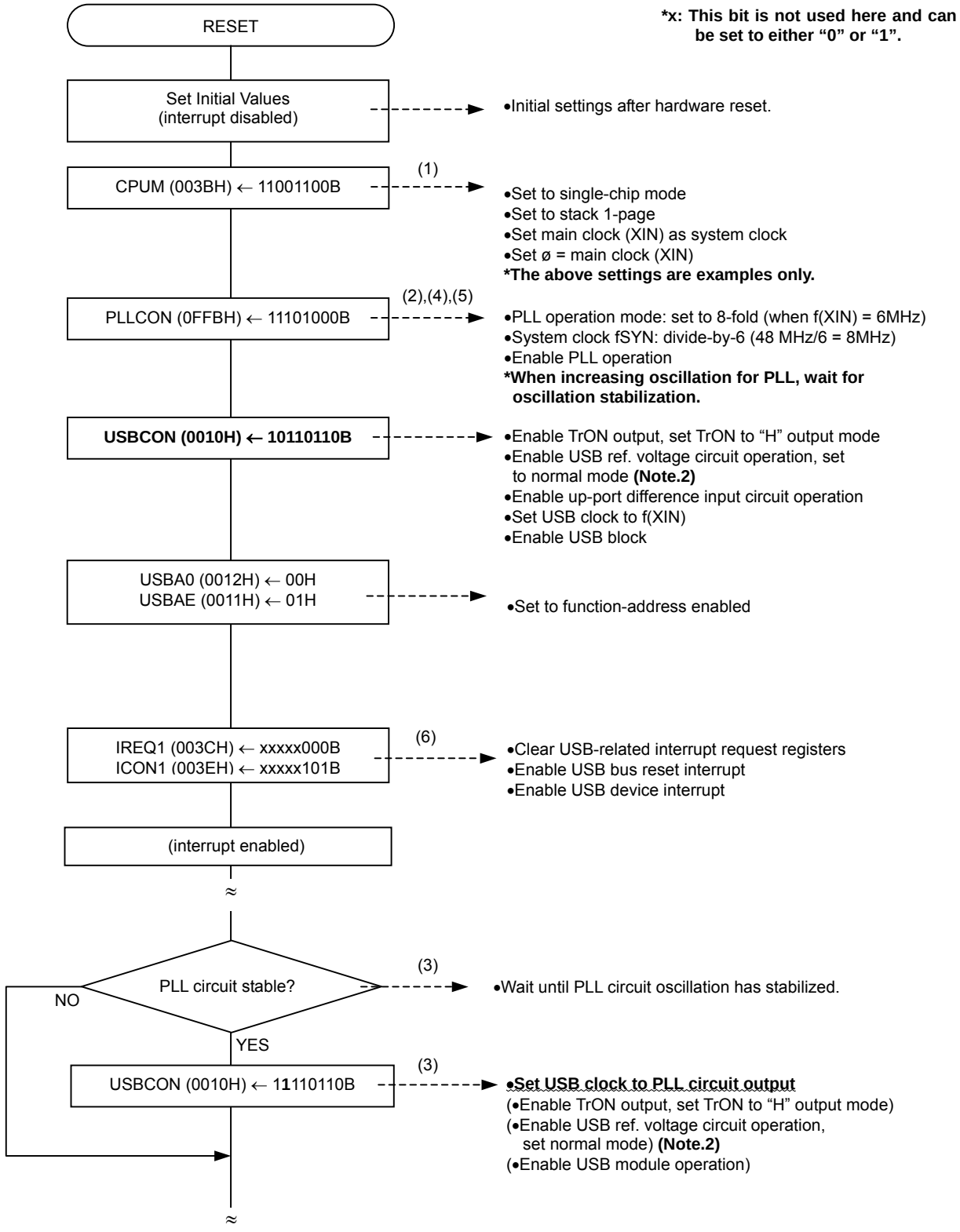
Table 1.3. USB Registers that Enable USB Block

Address	Symbol	Register Name
0010H	USBCON	USB Control Register
0011H	USBAE	USB Function Enable Register
0012H	USBA0	USB Function Address Bit
0016H	USBICON	USB Interrupt Source Enable Register
0017H	USBIREQ	USB Interrupt Source Register
0018H	USBINDEX	Endpoint Index Register
0FF8H	PLLCON	PLL Control Register
003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1

1.3.1. How to Enable the USB Device Block

Always enable the USB block after the oscillation of the MCU has stabilized. After enabling the PLL operation, add a wait period (about 1ms) to avoid any instability caused by the clock. Then enable the PLL circuit output after the wait period. By enabling the TrON port of the USBCON register to output “H”, the D+ signal is pulled up and the host (upstream-side) detects a connection of a USB device.

Figure 1.1 shows how to enable the USB block after a hardware reset. Figure 1.2 shows how to setup after a USB bus reset interrupt.



*x: This bit is not used here and can be set to either "0" or "1".

Note 1: This flowchart only shows steps that are related to the USB function.
Note 2: This setting is at Vcc=5V operation. At Vcc=3V operation, USB reference voltage enable bit (VREFE) must be set to disable ("0") (USB reference voltage control bit is ignored).

Figure 1.1 USB Device Block Enable and Initialization Process Example (at hardware reset)

The following are detailed descriptions of the steps shown in [Figure 1.1 USB Device Block Enable and Initialization Process Example (at hardware reset)].

(1) After setting the PLLCON register to generate a 48MHz USB clock, enable the PLL operation. The actual USB clock (fUSB) is supplied by setting the USB clock selection bit of the USBCON register to fVCO.
(2) The PLL circuit needs about 1ms for the output clock to stabilize after operation is enabled. Therefore, you must set the USB clock selection bit of USBCON to external oscillation f(XIN) for the first USB clock f(USB). At hardware reset, the USB clock select bit is “0” already.
(3) After PLL output clock stabilization, set the USBCON register USB clock select bit to “1” and the PLL clock output circuit (fVCO) is enabled..
(4) The USBCON USB reference voltage control bit is set to “0” in normal mode and “1” in suspend mode.*1
(5) The USBCON USB module operation enable bit is set to “1” in USB module operation enabled.

◆About USB module operation enable bit(USBE)

The USB module is initialized by setting the USB module operation enable bit of the USBCON register to “0”.

The registers that are initialized by a USB module reset are listed below.
For more details, refer to the description “at S/W reset” in the [USB Related Registers] Chapter of the 38K0 Group Data Sheet.

Note that only USBA0 (USB Function Address) is automatically initialized (“00” state) when a USB bus reset interrupt is generated.

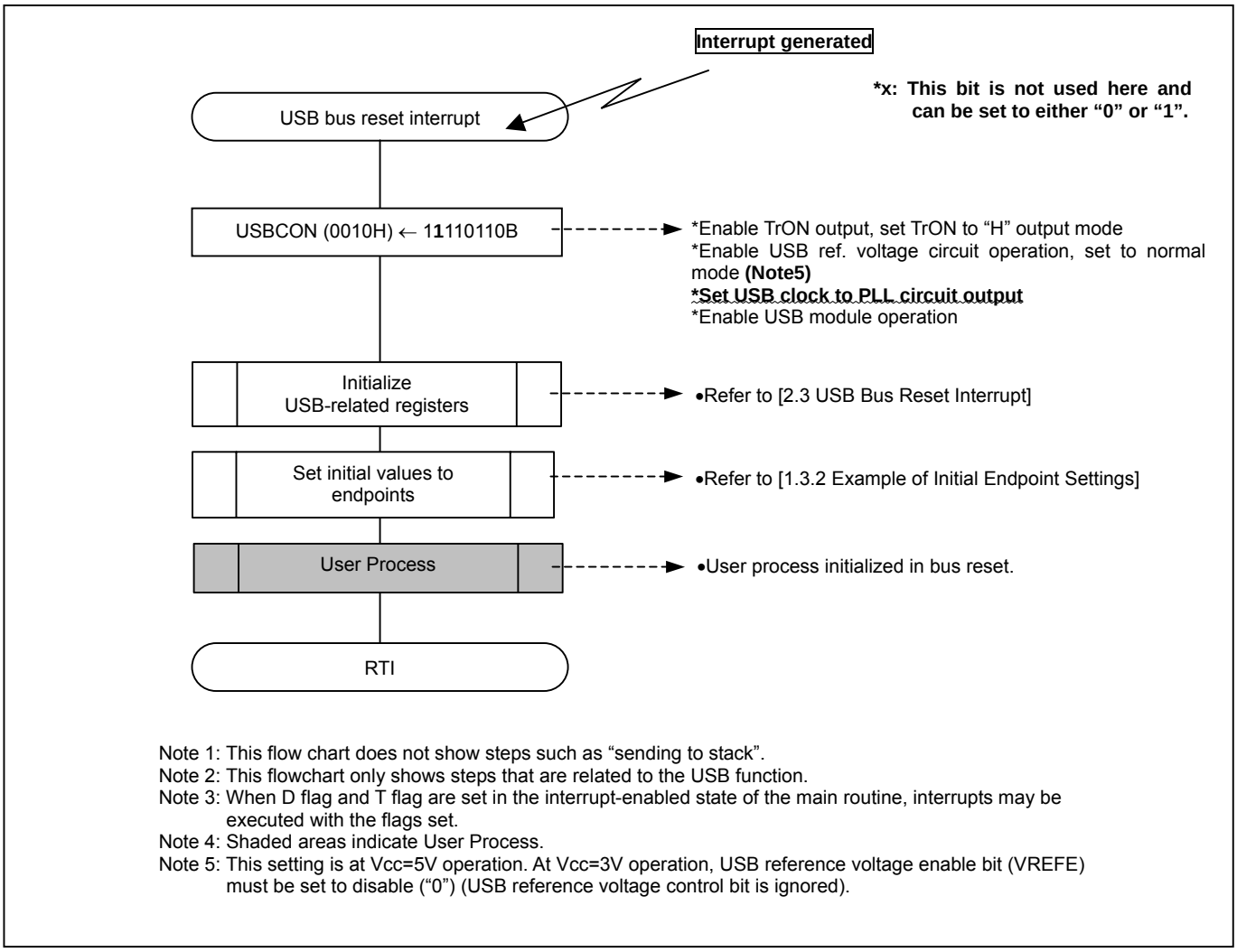
Table 1.4 USB Related Registers at S/W Reset

Address	Symbol	Register Name
0012H	USBA0	USB Function Address Register
0016H	USBICON	USB Interrupt Source Enable Register
0017H	USBIREQ	USB Interrupt Source Register
0019H	EP00STG	EP00 Status Register (when USBINDEX = “00”)
001DH	EPXXREQ	EPXX Interrupt Source Register (XX = USBINDEX = “00” to “03”)

(6) The USB bus reset interrupt and USB Device interrupt are enabled in the ICON1 register setting.

Other USB-related registers are set after the USB bus reset interrupt is executed. Refer to [Chapter 2.3 USB Bus Reset Interrupt] for more details.

*1 This setting is at Vcc=5V operation. At Vcc=3V operation, USB reference voltage enable bit (VREFE) must be set to disable (“0”) (USB reference voltage control bit is ignored).



Note 1: This flow chart does not show steps such as "sending to stack".
Note 2: This flowchart only shows steps that are related to the USB function.
Note 3: When D flag and T flag are set in the interrupt-enabled state of the main routine, interrupts may be executed with the flags set.
Note 4: Shaded areas indicate User Process.
Note 5: This setting is at Vcc=5V operation. At Vcc=3V operation, USB reference voltage enable bit (VREFE) must be set to disable ("0") (USB reference voltage control bit is ignored).

Figure 1.2 Initialization Process Example at USB Bus Reset Interrupt

1.3.2. Initialization of Endpoints

After specifying the endpoints to be set in the USB index register, set the MAX OUT packet size, transfer type, etc., for each endpoint to be used. Enable the USB interrupt as necessary.
When setting the start address for the buffer area of each endpoint, make sure the addresses for single buffer and double buffer do not overlap. For more details, refer to [Chapter 3: USB Transfer/Receive].
Figure 1.3 shows an example of initial endpoint settings. Make sure the USB block and USB clock are both enabled before programming the related registers.

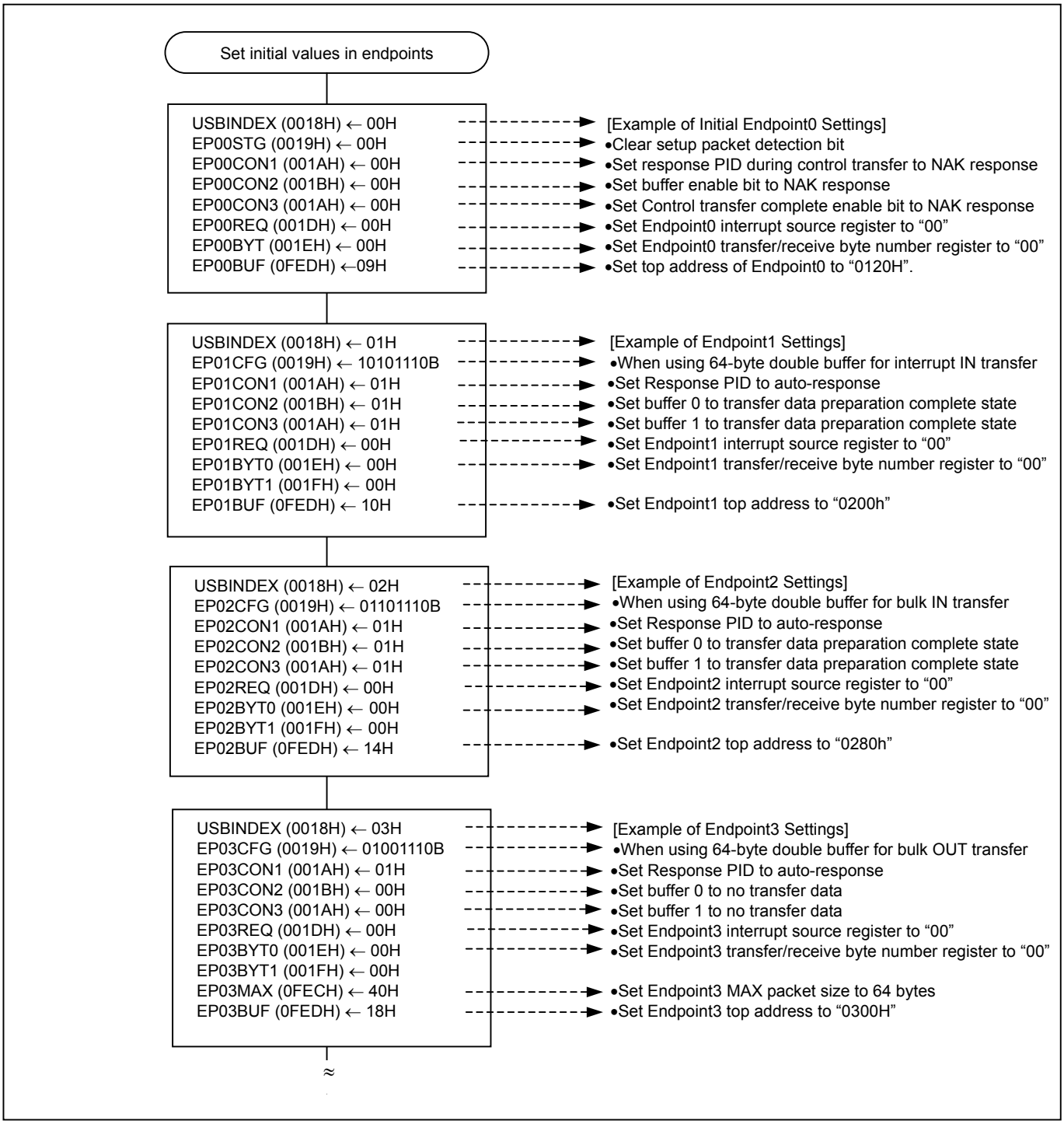


Figure 1.3 Examples of Initial Endpoint Settings

1.3.3. Re-Enumeration Process During USB Transfer

This process allows you to re-enumerate the MCU during a USB transfer without removing and re-inserting the USB cable. Follow the re-enumeration process shown in Figure 1.1 using the instructions below.

***Always perform a complete evaluation on the user system when executing this process.**

(1) Enable the Detach status by setting TRONE (TrON Output Enable Bit) of the USBCON register to "1" (output enabled status) and TRONCON (TrON Output Control Bit) to "0" ("L" output mode).
(2) You can also enable the Detach status by setting the TRONE bit to "0" (output disabled status).
(3) After executing Step (1) or (2), add a WAIT of at least 2.5μs so that the host has enough time to recognize the Detach status. A wait is also necessary for the D+ discharge. The length of the WAIT period will depend on the system itself so it is necessary for the user to evaluate the MCU on the target system. In addition, the time it takes the TrONCON bit to go to "L" will be longer for Step 2 than Step 1. This should also be considered when programming the length of the WAIT.
(4) Due to the TrON "L" output mode and the TrON output disable status (Hi-Z status), the USB Device Control Unit may recognize the SE0 state and determine it to be a bus reset. To avoid this, disable the USB bus-reset interrupt in ICON1 (interrupt control register) before performing Step 1 or 2.
(5) D+ is pulled up by setting the USBCON register TRONE bit to "1" (output enabled status) and the TRONCON bit to "1" ("H" output mode).
(6) Clear the USB bus-reset interrupt request in the interrupt request register (IREQ1) and enable the USB bus-reset interrupt in ICON1.

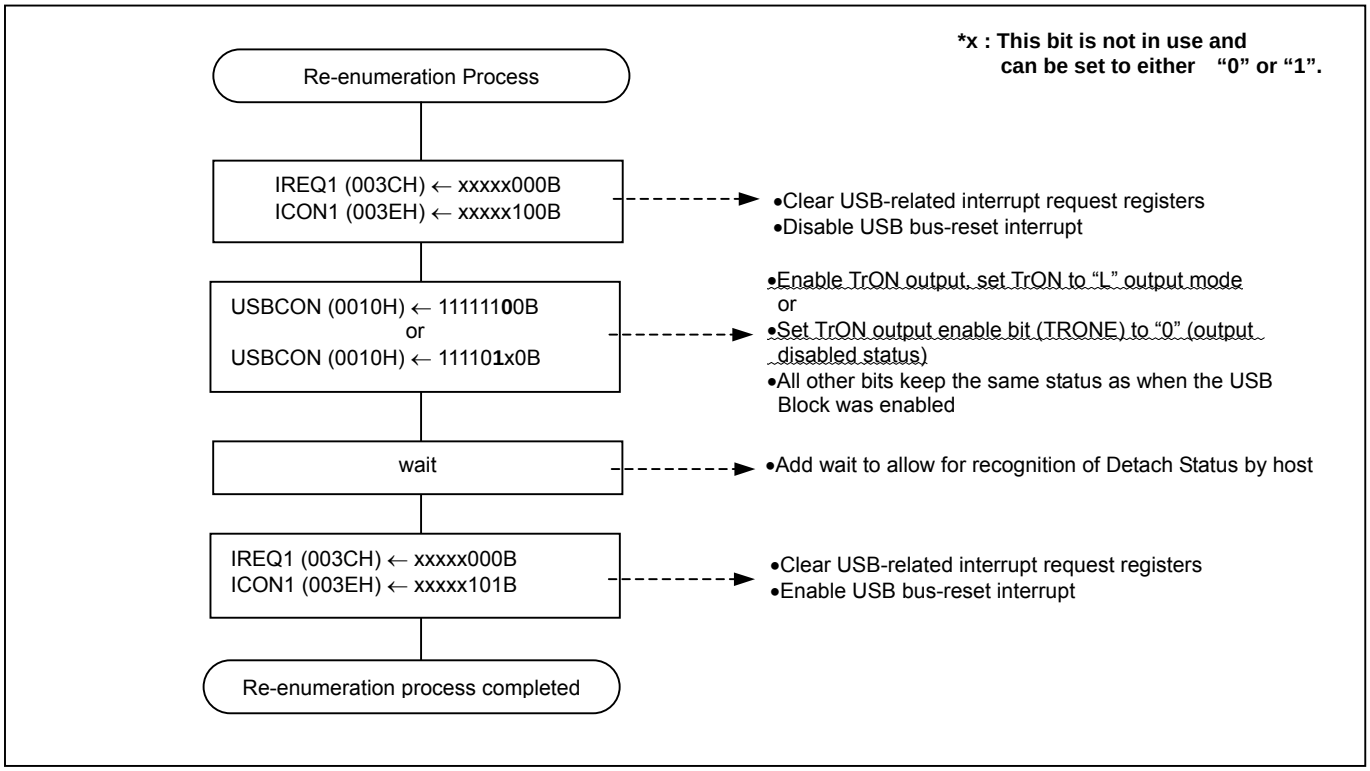
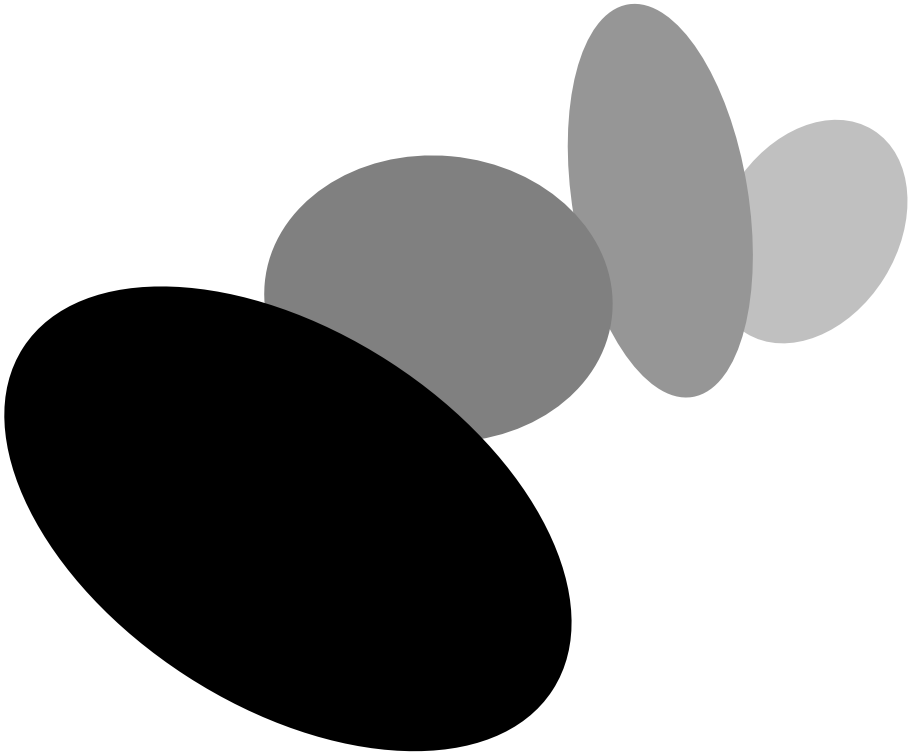


Figure 1.4 Re-Enumeration Process



Chapter 2
State Transition and USB Interrupts

The 38K0 Group USB Interrupts consist of the device interrupt, the SOF interrupt and the Bus Reset Interrupt. This Chapter explains the USB Interrupts and State Transition.

2.1. Device State Transition

The USB device moves from one state to another according to the current operations. In the 38K0 Group, device state transition occurs with each USB interrupt (reset, suspend, resume) or Endpoint0 device standard request processing.

Figure 2.1 shows device state transitions for the 38K0 Group.

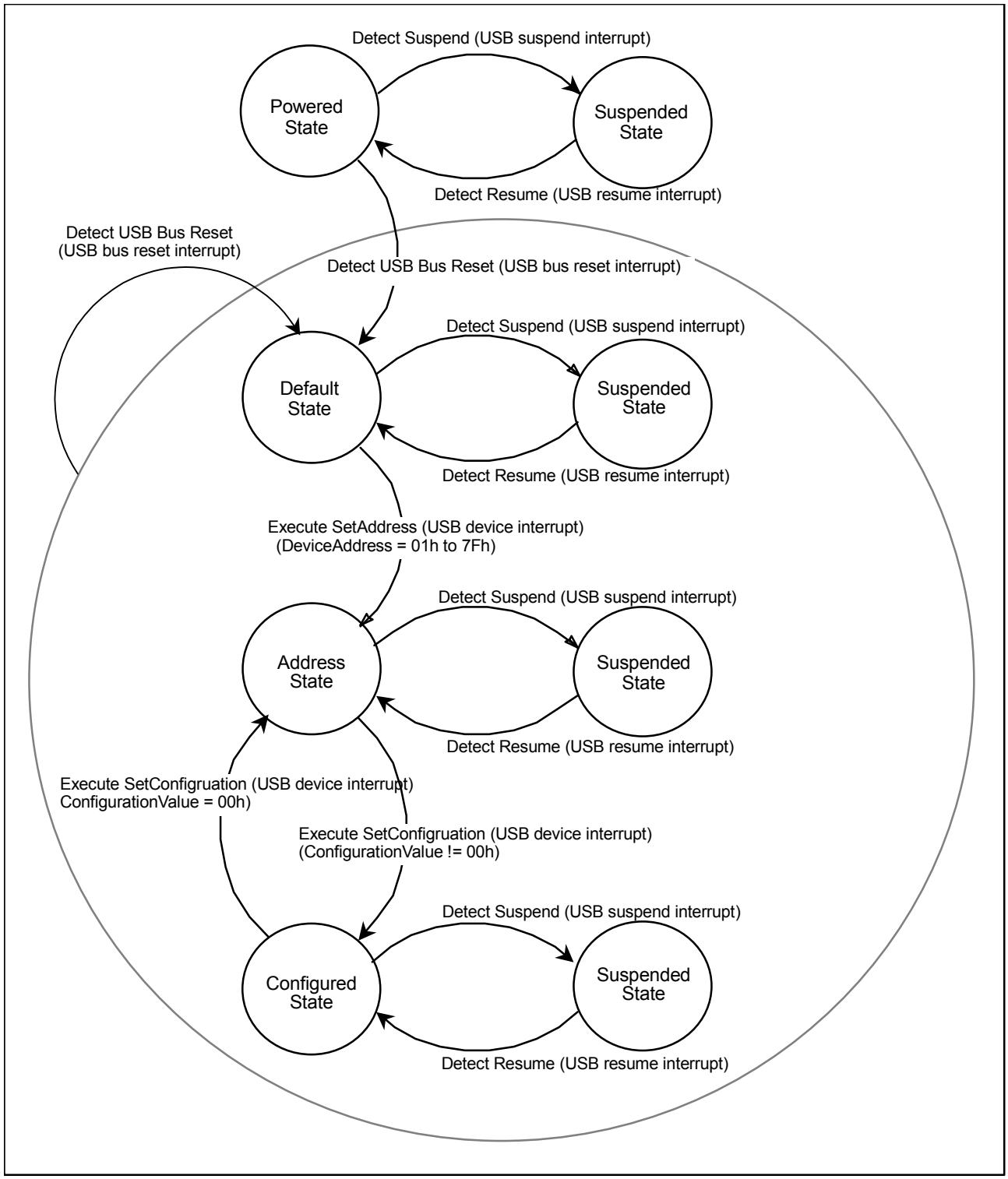


Figure 2.1 Device State Transitions

2.2. How to Use USB Interrupts

The 38K0 Group has three basic sources of USB interrupts: bus reset, device, and USB SOF. The USB device interrupt is used for data flow control and special USB signals (suspend, resume). Interrupt vector addresses are shown in Table 2.1 and registers related to USB interrupts are shown in Table 2.2

For details concerning the states and interrupts of each register, refer to Chapters [Interrupts] and [USB Register List] in the 38K0 Group Data Sheet.

Table 2.1 Interrupt Vector Addresses and Priority

Interrupt Source	Priority	Vector Address		Interrupt Request Generation Conditions
		Upper	Lower	
Reset	1	FFFDH	FFFCH	Reset
USB bus reset	**2**	**FFFBH**	**FFFAH**	**Detection of USB bus reset signal (SE0 for 2.5 µs)**
USB SOF	**3**	**FFF9H**	**FFF8H**	**Detection of USB SOF signal**
USB device	**4**	**FFF7H**	**FFF6H**	**Detection of Resume signal (K state or SE0) or Detection of Suspend signal (bus idle for 3ms) or Transaction complete**
External bus	5	FFF5H	FFF4H	

Table 2.2 USB Registers and Interrupt Registers

Address	Symbol	Register Name
0016H	USBICON	USB Interrupt Source Enable Register
0017H	USBIREQ	USB Interrupt Source Register
0018H	USBINDEX	Endpoint Index Register
0019H	EPXXREG1	Endpoint Field Register 1
001AH	EPXXREG2	Endpoint Field Register 2
001BH	EPXXREG3	Endpoint Field Register 3
001CH	EPXXREG4	Endpoint Field Register 4
001DH	EPXXREG5	Endpoint Field Register 5
001EH	EPXXREG6	Endpoint Field Register 6
001FH	EPXXREG7	Endpoint Field Register 7
0FECH	EPXXREG8	Endpoint Field Register 8
0FEDH	EPXXREG9	Endpoint Field Register 9
003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1

2.3. USB Bus Reset Interrupt

The USB bus reset interrupt is generated when SE0 continues for 2.5µs or more on the USB bus. Table 2.3 lists registers related to USB devices and Figure 2.2 shows an example of the USB device interrupt routine.

(1) Cause of USB bus reset detection

A reset is detected when SE0 ("L" level in the D+/D- line) continues on the USB bus for at least 2.5µs.

(2) Action when a USB bus reset is detected

When a USB bus reset is detected as described above, the USB bus reset interrupt request bit of IREQ1 (Interrupt Request Register) is set to "1".

(3) USB bus reset interrupt settings

Set the USB bus reset interrupt enable bit of ICON1 (Interrupt Control Register) to "1".

(4) Conditions for accepting a USB bus reset interrupt

A USB bus reset interrupt will be generated when all of the following conditions are fulfilled:

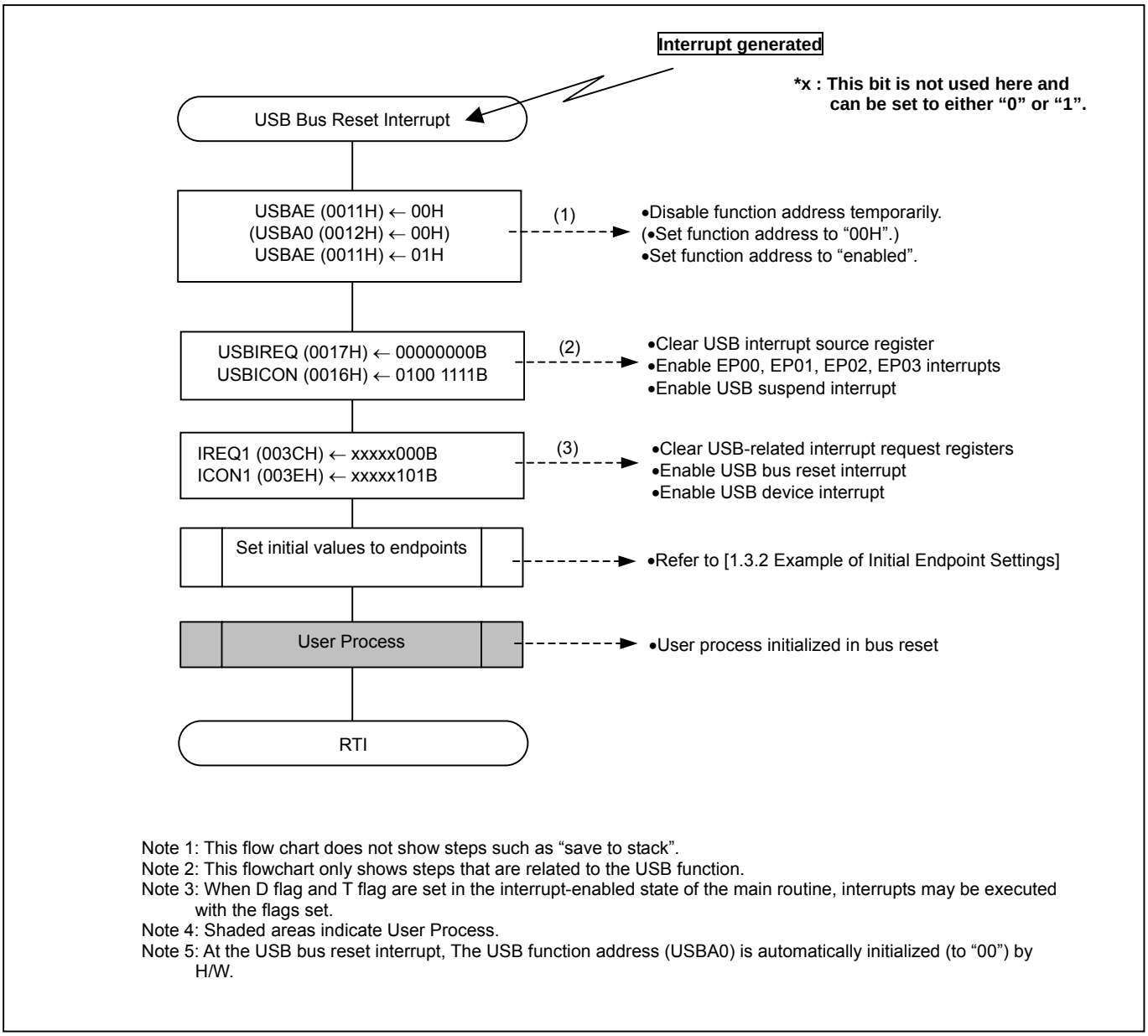
- I Flag (Interrupt Disable Flag) of the processor status register is "0" (interrupt enabled).
- The USB bus reset interrupt enable bit of ICON1 is "1" (enabled state)
- USB bus reset interrupt request bit of IREQ1 is "1" (interrupt generated)

(5) USB bus reset interrupt routine

- Figure 2.2 shows an example of the USB bus reset interrupt routine.
- When a USB bus reset interrupt is received, the interrupt request flag is cleared at the same time the interrupt is generated. Therefore, it is not necessary to clear the flag in the interrupt routine.

Table 2.3 Registers related to USB Reset Interrupt

Address	Symbol	Register Name
003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1



Note 1: This flow chart does not show steps such as “save to stack”.
Note 2: This flowchart only shows steps that are related to the USB function.
Note 3: When D flag and T flag are set in the interrupt-enabled state of the main routine, interrupts may be executed with the flags set.
Note 4: Shaded areas indicate User Process.
Note 5: At the USB bus reset interrupt, The USB function address (USBA0) is automatically initialized (to “00”) by H/W.

Figure 2.2 Example of USB Bus Reset Interrupt Routine

The following are detailed descriptions of the steps shown in [Figure 2.2 Example of USB Bus Reset Interrupt Routine].

(1) USB address initialization
- When setting an address to the USBA0 register, if the USBAE register changes from “00H” to”01H”, the contents of the USBA0 register become valid.

(2) USB-related interrupt settings #1
- Clear USBIREQ.
- Enable SUSE (USB Suspend Interrupt) and EP00E (Endpoint0 interrupt) of the USBICON register.
- Enable the SUSE interrupt and Endpoints 1 to 3 interrupts (EP0xE) as necessary.

*We recommend clearing the interrupt request bits before enabling interrupts.

(3) USB-related interrupt settings #2
- Clear IREQ1 interrupts (USB bus reset, USB SOF, and USB device interrupts).
- Enable USB bus reset and USB device interrupts of ICON1.

2.4. USB Device Interrupt

The USB device interrupt is used for data flow control and USB special signals (suspend, resume). The types of interrupts used for data flow control are listed below.

- **Interrupt generated when Endpoint0 data transfer/receive is complete**
- **Interrupt generated when Endpoint1 data transfer/receive is complete**
- **Interrupt generated when Endpoint2 data transfer/receive is complete**
- **Interrupt generated when Endpoint3 data transfer/receive is complete**

The following two interrupts are used for USB special signals (suspend, resume).

- **USB suspend interrupt**
- **USB resume interrupt**

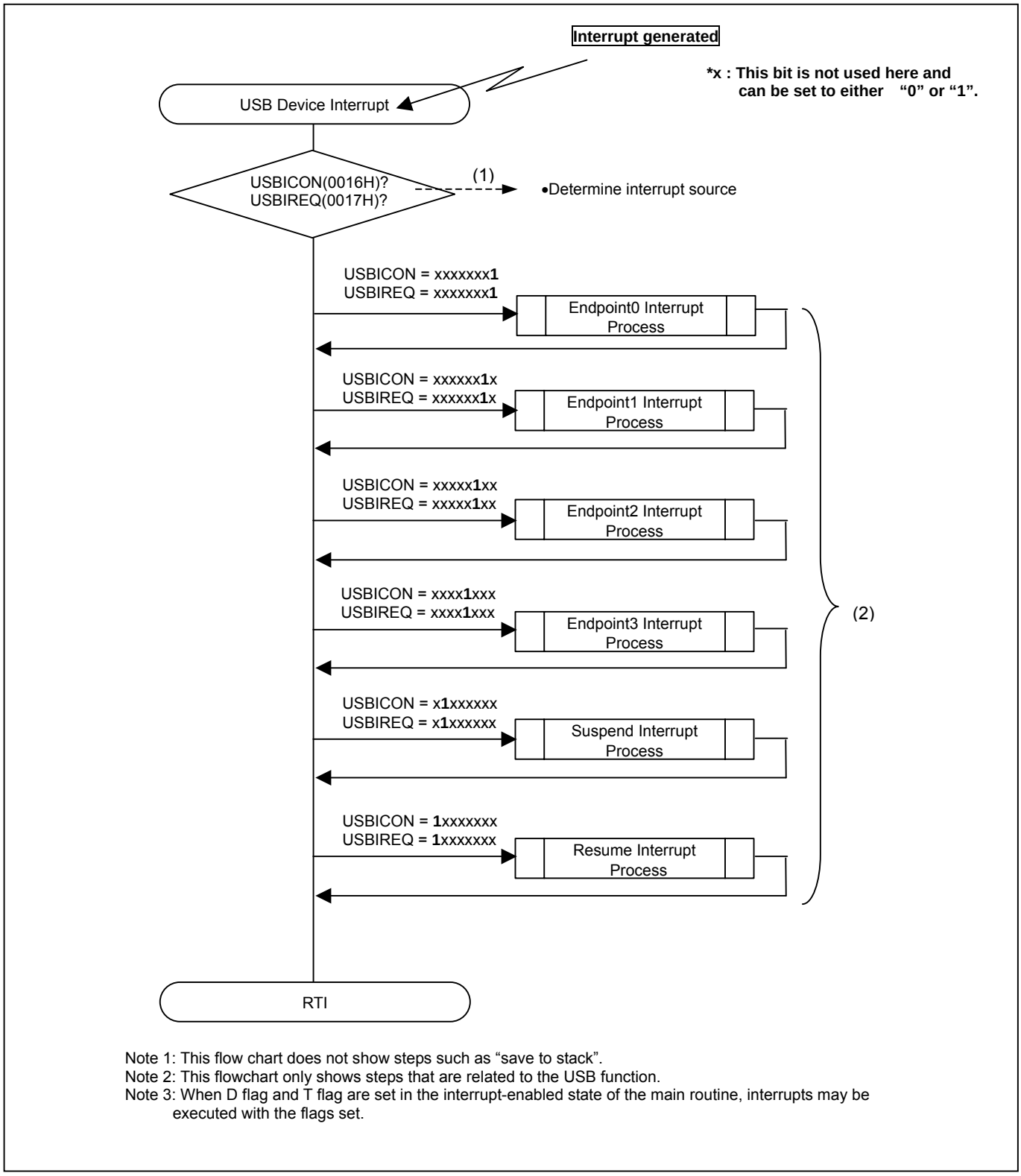
In order to enable the USB device interrupt, set the USB device interrupt enable bit of ICON1 (Interrupt Control Register) to “1”.

To enable any of the above interrupts, set the corresponding USBICON (USB Interrupt Source Enable Register) bit to “1”. The bit corresponding to USBIREQ (USB Interrupt Request Register) or EP0xREQ (EP0x Interrupt Source Register, x = 1 to 3) will indicate the interrupt request state.

Table 2.4 lists the USB device interrupt registers and Figure 2.3 shows an example of the USB device interrupt routine.

Table 2.4 USB Device Interrupt Registers

Address	Symbol	Register Name
0016H	USBICON	USB Interrupt Source Enable Register
0017H	USBIREQ	USB Interrupt Source Register
0018H	USBINDEX	Endpoint Index Register
001DH	EP0xREQ	EP0x Interrupt Source Register (x = 0 to 3)
003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1



Note 1: This flow chart does not show steps such as "save to stack".
Note 2: This flowchart only shows steps that are related to the USB function.
Note 3: When D flag and T flag are set in the interrupt-enabled state of the main routine, interrupts may be executed with the flags set.

Figure 2.3 Example of USB Bus Device Interrupt Routine

The following are detailed descriptions of the steps shown in [Figure 2.3 Example of Bus Reset Interrupt Routine].

(1) Interrupt Source Determination Method #1

The bus device interrupt is determined by the AND condition of the enable bit state of USBICON (USB Interrupt Source Enable Register) and the source bit state of USBIREQ (USB Interrupt Source Register). In other words, when both bits are “1”, the next step in the process (the Chapter indicated by (2) in Figure 2.3) is valid.

(2) Interrupt Source Determination Method #2

To prevent sources from being ignored and left unprocessed when multiple interrupt sources are generated simultaneously, each source is checked and processed according to order of receipt. Depending on the transmission timing, each time interrupts are generated, all bits of both USBICON and USBIREQ are judged and interrupts are processed accordingly to avoid continuously processing only Endpoint0.

◆ “38K2 group USB sample firmware” has sample procedures (1) and (2).

2.4.1. USB Function/Endpoint Interrupts

The interrupts available for Endpointx are as follows.

♦Interrupt generated when Endpoint0 data transfer/receive is complete
1.Endpoint0 data buffer ready interrupt
2.Control transfer complete interrupt
3.Status stage transition interrupt
4.Endpoint0 SETUP buffer ready interrupt
5.Error interrupt

♦Interrupt generated when Endpointx*1 data transfer/receive is complete
1.Endpointx data buffer0 ready interrupt
2.Endpointx data buffer1 ready interrupt
3.Error interrupt

♣ Conditions for accepting a USB function/endpointx interrupt

A USB function/endpointx interrupt will be generated when all of the following conditions are fulfilled:

- I Flag (Interrupt Disable Flag) of the processor status register is “0” (interrupt enabled).
- The USB device interrupt enable bit of ICON1 (Interrupt Control Register) is “1” (interrupt enabled).
- The USB device interrupt source bit of IREQ1 (Interrupt Request Register) is “1” (interrupt requested)
- EP0xE (USB Function/Endpointx Interrupt Enable Bit) which corresponds to the USBICON (Interrupt Source Enable Register) endpoint is “1” (enabled state).
- EP0x (USB Function/Endpointx Interrupt Bit) which corresponds to the USBIREQ (Interrupt Source Register) endpoint is “1” (interrupt requested).
  *This bit is set when at least one bit of EP0x is set to “1”. This cannot be set or cleared by software.
- The interrupt bits that correspond to the endpoint (value specified by USBINDEX (Endpoint Index Register)) and EP0xREQ (EP0x Interrupt Source Register) are “1” (interrupt requested).
  (When referencing EP0xREQ, set the endpointx that corresponds to USBINDEX.)

♣ USB function/endpointx interrupt processing

- Refer to [Chapter 3.2.3 Endpoint0 Interrupt] and [Chapter 3.3.3 Endpointx Interrupt] for examples of interrupt processing.
- When a USB function/endpointx interrupt is accepted, the USB Device Interrupt Request Flag (the root flag) is cleared as soon as the interrupt is accepted. Therefore, there is no need to clear the flags when processing. EP0x of USBIREQ cannot be cleared by software. By clearing the EP0xREQ that corresponds to the endpoint (the value specified in USBINDEX) to “00”, the endpoint will be cleared by hardware.

*1 “x” indicates Endpoints 1, 2, and 3.

2.4.2. USB Suspend Interrupt

The USB suspend interrupt occurs when an idle state is detected on the USB up port for 3.0ms or more.

In the USB suspend state, the USB bus can only bring the total drive current to 500µA or less. Therefore, when in bus-powered operations, the MCU must be put in the low-power consumption mode after suspend is detected.

In order to reactivate the device from the suspend state, a request must be sent to the host via a bus activity on the USB up port or resume request a remote wake-up function.

In the suspend state, the USB clock will not oscillate but the USB block will remain enabled, and therefore, bus activity can be detected by a resume interrupt. (For more details concerning the resume interrupt refer to [Chapter 2.4.3 USB Resume Interrupt].)

If the device supports remote wake-up, a remote wake-up signal can be delivered according to user system specifications. For more details concerning remote wake-up, refer to [Chapter 2.4.3.1 Remote Wake-up].

Table 2.5 shows a list of registers related to USB suspend interrupt.

(1) Cause of USB suspend detection

USB suspend is detected when the bus lines are idle (D+ line is “H”, the D- line is “L”) for a period of 3.0ms or more.

(2) Action when a USB suspend is detected

When a USB suspend is detected as described above, bit SUS (USB Suspend Interrupt Request Bit) of USBIREQ (USB Interrupt Request Register) is set to “1”.

(3) USB suspend interrupt settings

Set bit SUSE (Suspend Interrupt Enable Bit) of USBICON (USB Interrupt Source Enable Register) to “1” (enabled state).

(4) Conditions for accepting a USB suspend interrupt

A USB suspend interrupt will be generated when all of the following conditions are fulfilled:

- I Flag (Interrupt Disable Flag) of the processor status register is “0” (interrupt enabled).
- The USB device interrupt enable bit of ICON1 (Interrupt Control Register) is “1” (enabled state).
- The USB device interrupt request bit of IREQ1 (Interrupt Request Register) is “1” (requested).
- Bit SUSE of USBICON is “1” (enabled state).
- Bit SUS of USBREQ (USB Interrupt Source Enable Register) is “1” (requested).

(5) Recovery from the USB suspend status

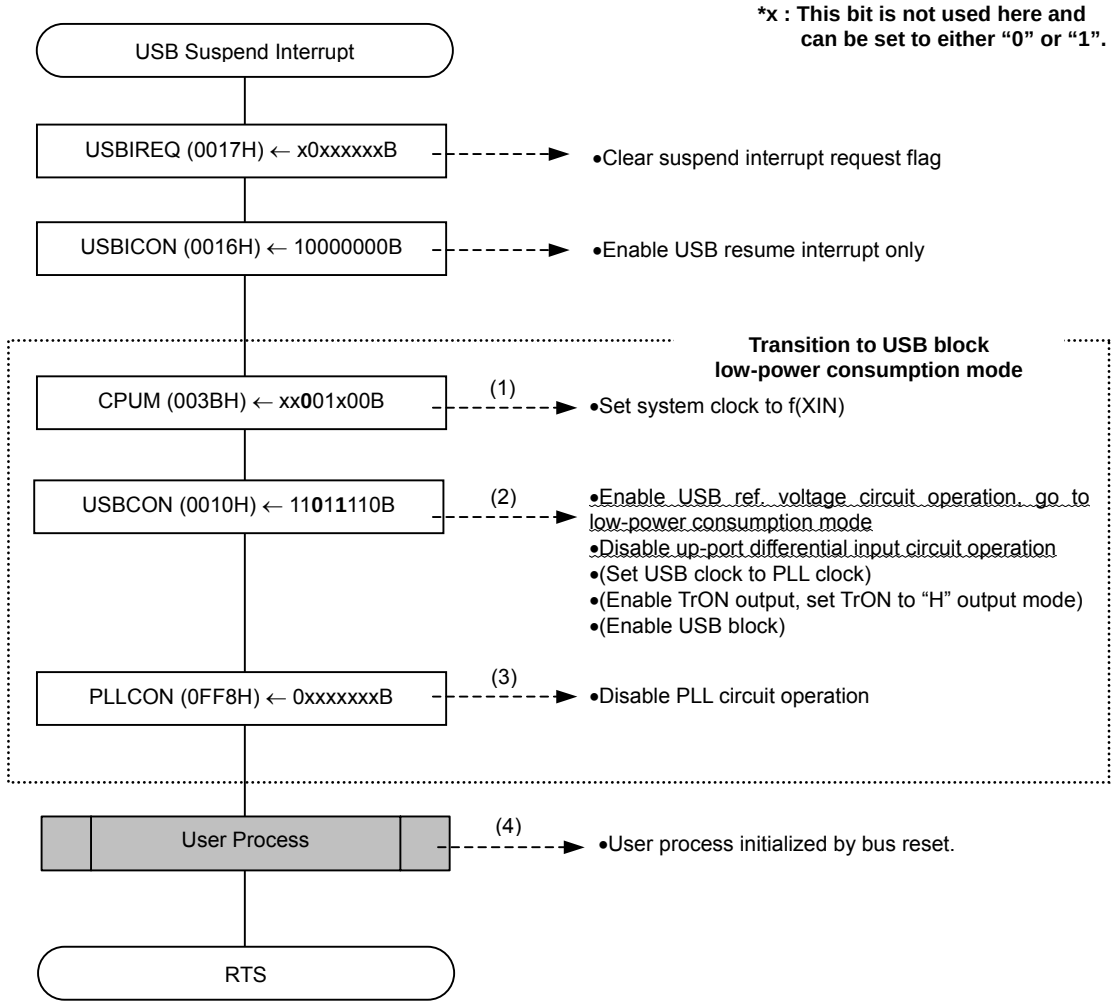
The MCU is recovered from the USB suspend status by a USB resume interrupt or remote wake-up.
For more details concerning remote wake-up signals, refer to [Chapter 2.4.3.1 Remote Wake-Up].
Set one of wake-up sources in the USB suspend interrupt routine.

(6) USB suspend interrupt processing

- An example of the processing routine executed when a USB suspend interrupt is received is shown in Figure 2.4.
- When a USB suspend interrupt is accepted, USB Device Interrupt Request Flag (the root flag) is cleared as soon as the interrupt is accepted and does not need to be cleared by software during the interrupt routine. However, bit SUS of USBIREQ must be cleared by software.

Figure 2.5 USB Suspend Interrupt Registers

Address	Symbol	Register Name
0016H	USBICON	USB Interrupt Source Enable Register
0017H	USBIREQ	USB Interrupt Source Register
003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1



Note 1: This flowchart only shows steps that are related to the USB function.
Note 2: This routine is a subroutine called up in [Figure 2.3 Example of USB Device Interrupt Routine].
Note 3: Execution of STP instruction (Stop mode: oscillation STOP state) is performed in the main routine.
Refer to [Figure 2.5 USB Suspend Process Examples (MAIN)]
Note 4: Shaded area indicates User Process.

Figure 2.4 Example of USB Suspend Interrupt Routine

The following are detailed descriptions of the steps shown in [Figure 2.4 Example of USB Suspend Interrupt Routine].

(1) System clock setting
- Since the USB clock will stop, it is necessary to select the main clock f(XIN) with the system clock selection bit of CPU Mode Register (CPUM).

(2) USB Control Register (USBCON)
- Enable the USB ref. voltage circuit operation (VREFE = "1")*1, go to low-power consumption mode (VREFCON = "1"), and input the up-port differential.
- Change the setting to circuit operation disabled (USBDIFE = "0"). All other bits remain in the pre-suspend state.
- Although the USB reference circuit goes to the low-power consumption mode, TrON stays in the 3V state. The difference between low-power consumption mode and normal mode is the drive capacity.

(3) Disable PLL operation
- When Disable PLL circuit operation without changing the PLL operation mode (any setting other than "00") of PLLCON (PLL Control Register), the PLL circuit is stopped, the PLL circuit output clock (fVCO) is fixed to "L".

(4) User system settings when using BUS Power
- The user system peripheral circuit control also needs to be switched to the low-power consumption mode.
- When using a remote wake-up, enable the interrupts that are included in the wake-up conditions. This applies only when the remote wake-up from the host is enabled.

The STP instruction (STOP mode: oscillation STOP state) is executed in the main routine after the USB suspend interrupt processing shown in Figures 2.4.

Examples of USB suspend processes, which are executed in the main routine, are shown in Figure 2.5.

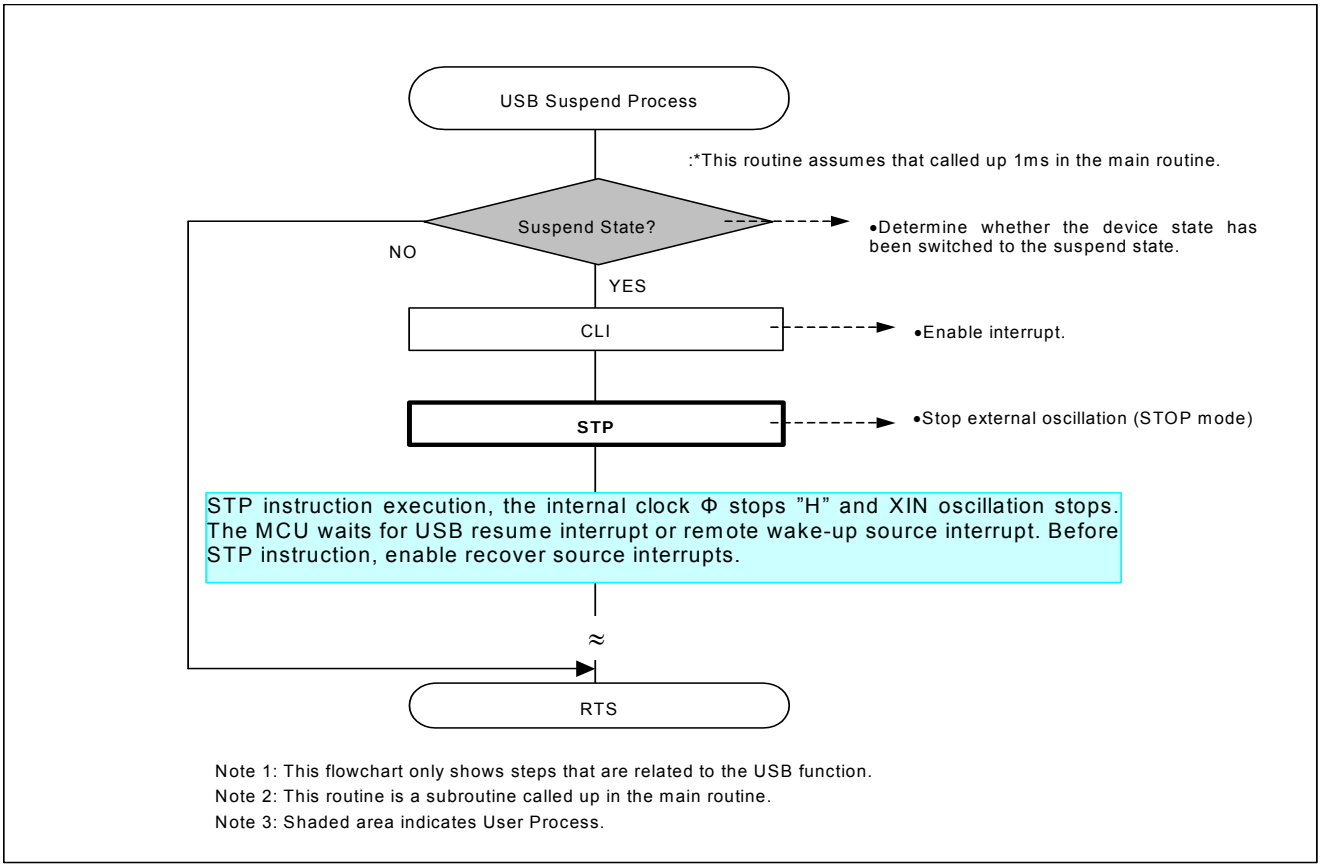


Figure 2.5 USB Suspend Processing Example (Main Routine)

*1 This setting is at Vcc=5V operation. At Vcc=3V operation, USB reference voltage enable bit (VREFE) must be set to disable ("0") (USB reference voltage control bit is ignored).

2.4.3. USB Resume Interrupt

USB resume interrupt occurs when the USB block detects a state change of the USB bus during the suspend state. Because the USB resume interrupt is generated due to a state change of the USB bus, the interrupt will occur even if no clock (USB clock) is supplied to USB block.
Registers related to the USB resume interrupt are listed in Table 2.7.

(1) Cause of USB resume detection

A USB resume is detected when the state of the USB bus changes: when detecting a change of “J” to “K” or “SE0”.

(2) Action when a USB resume is detected

When a USB resume is detected as described above, bit RSM (Resume Interrupt Bit) of USBIREQ (USB Interrupt Source Register) is set to “1”.

(3) USB resume interrupt settings

Set bit RSME (Resume Interrupt Enable Bit) of USBICON (USB Interrupt Source Enable Register) to “1” (enabled state).

(4) Conditions for accepting USB resume interrupt

A USB resume interrupt will be generated when all of the following conditions are fulfilled:

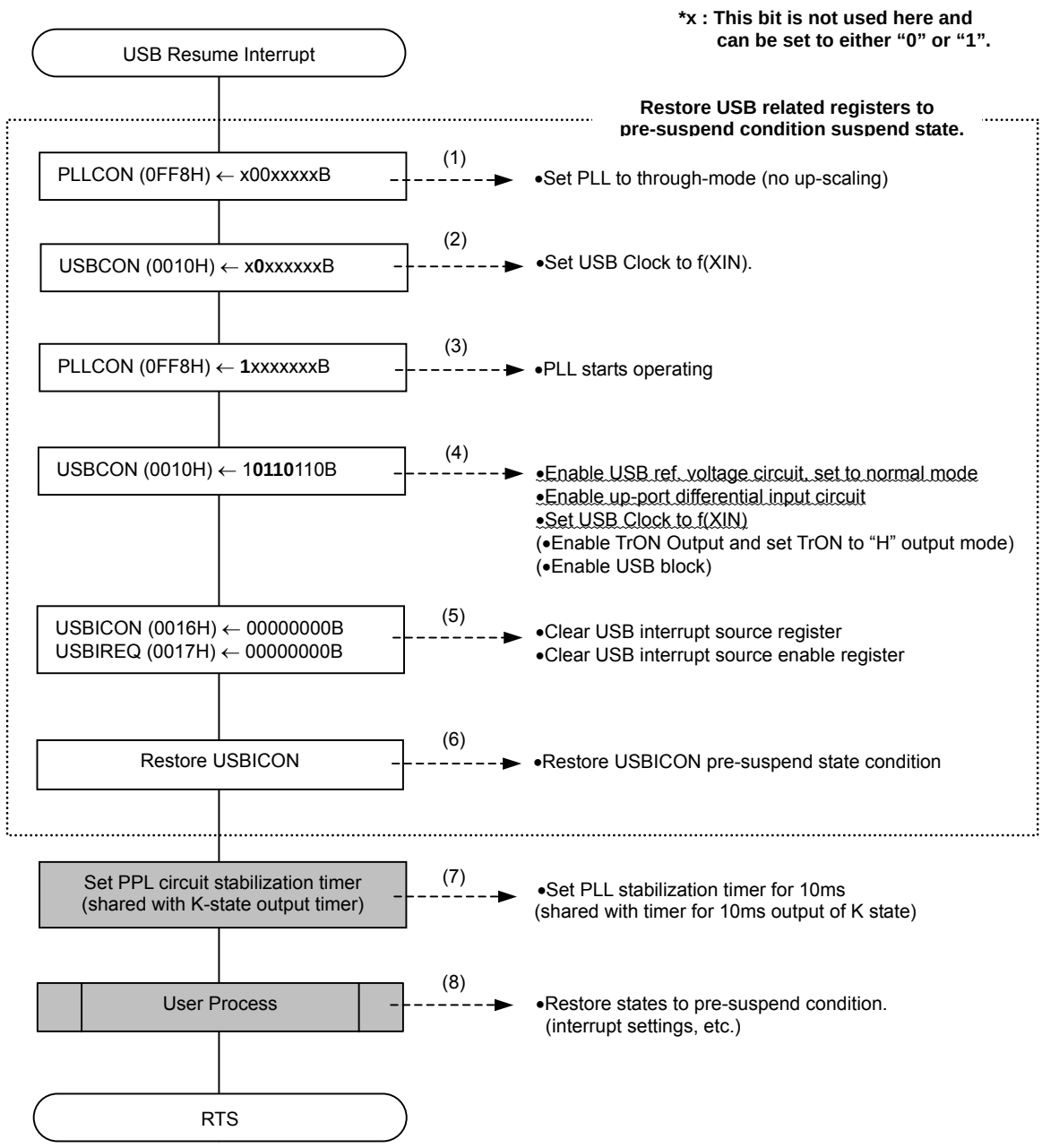
- I Flag (Interrupt Disable Flag) of the processor status register is “0” (interrupt enabled).
- The USB function interrupt enable bit of ICON1 (Interrupt Control Register) is “1” (enabled state).
- The USB function interrupt request bit of IREQ1 (Interrupt Request Register) is “1” (requested)
- Bit RSME of USBICON is “1” (enabled state)
- Bit RSM of USBIREQ is “1” (requested).

(5) USB resume interrupt processing

- An example of the processing routine that is executed when a USB suspend interrupt is accepted is shown in Figure 2.6.
- When a USB resume interrupt is accepted, USB Device Interrupt Request Flag (the root flag) is cleared as soon as the interrupt is accepted and does not need to be cleared by software during the interrupt routine. Please note that bit RSM of USBIREQ cannot be cleared by software. Setting 0 to bit RSME of USBICON will automatically clear bit RSM.

Table 2.6 USB Resume and Remote Wakeup Registers

Address	Symbol	Register Name
0010H	USBCON	USB Control Register
0016H	USBICON	USB Interrupt Source Enable Register
0017H	USBIREQ	USB Interrupt Source Register
003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1



Note 1: This flowchart only shows steps that are related to the USB function.
Note 2: This routine is a subroutine called up in [Figure 2.3 Example Routine of USB Device Interrupt]
Note 3: The shaded area indicates User Process.

Figure 2.6 Example of USB Resume Interrupt Routine

The following are detailed descriptions of the steps shown in [Figure 2.6 Example of USB Resume Interrupt Routine].

(1) Setting the PLL operation mode to through mode
- The PLL circuit output clock (fVCO) is fixed to "L" during the suspend state. The PLL circuit must be released in the following manner. (If the clock remains in the "L" level, the USB clock in Step (2) cannot be switched).
- When Set the PLL operation mode of PLLCON (PLL Control Register) to "no-up scaling" ("00" = through mode), in the through mode, external clock f(XIN) will be output through PLL even if PLL circuit operation is disabled.

(2) USB clock settings
- Set the USB clock to f(SIN) (UCLKCON = "0") in order to initiate PLL clock operation.

*After the PLL circuit is enabled, the output clock needs approximately about 1ms stabilize. Therefore, the USB clock selection bit of USBCON must be set to "0" and f(XIN) (external oscillation) must be used as the initial USB clock.

(3) Starting PLL circuit operation
- Set PLL circuit operation of PLLCON to "1". After the PLL circuit has stabilized (after 1ms) set the USB clock to PLL circuit output clock (fVCO) in the main routine.

(4) USB Control Register (USBCON) settings
- Return the MCU to the pre-USB suspend state settings: USB ref. voltage circuit operation enabled (VREF = "1")*1, normal mode (VREFCON = "0"), and up-port differential input circuit operation enabled (USBDIFE = "1").

(5) Clearing USBIREQ, USBICON
- Clear USBIREQ (USB Interrupt Source Register) and USBICON (USB Interrupt Source Enable Register).
- Clear the interrupt request bit by setting bit RSME (Resume Interrupt Enable Bit) of USBICON to "0" (disabled), This will clear bit RSM (Resume Interrupt Source Bit) of USBIREQ by hardware. This bit cannot be cleared by software.

(6) Recovering USBICON (USB Interrupt Source Enable Register)
- Return the contents of USBICON to its pre-USB suspend state settings.

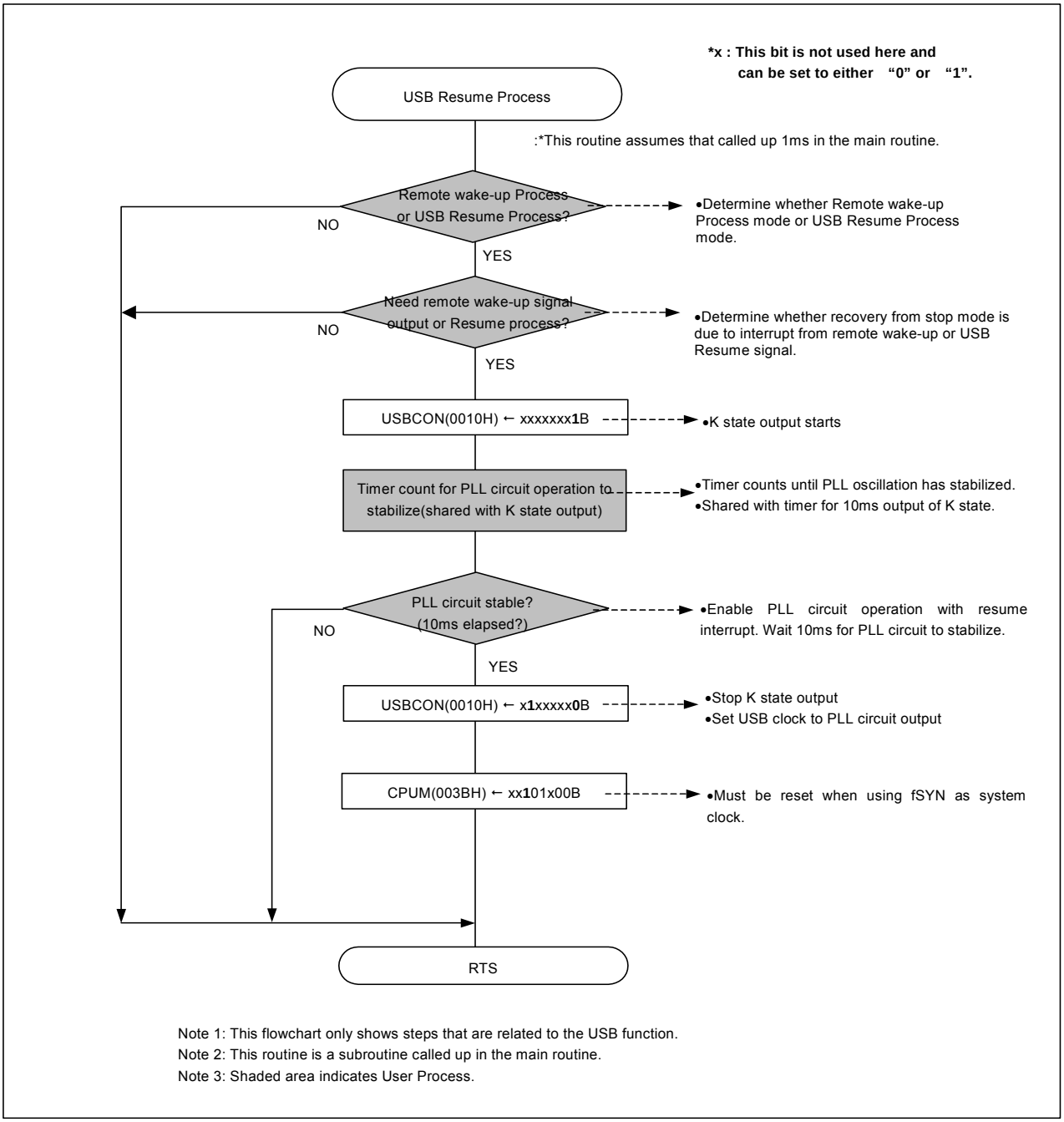
(7) Setting PLL circuit operation stabilization timer and remote wake-up signal "K" state output timer
- Set PLL circuit oscillation stabilization wait timer count value.
- For a case that a remote wake-up signal "K" state output is required, set the "K" state output time counter.

◆38K0 group sample firmware sets the timer count value above, which is also used as the main counter, to 12ms.

(8) Setting bus-powered user system
- Interrupts, etc., set by the user must be restored to their pre-USB suspend state.
- Restore peripheral circuit control and low-power consumption mode to normal mode.

Examples of USB resume processes, which are executed in the main routine, are shown in Figure 2.7. For more details on the resume interrupt and remote wake-up, refer to [Chapter 2.4.3.1 Remote Wake-up].

*1 This setting is at Vcc=5V operation. At Vcc=3V operation, USB reference voltage enable bit (VREFE) must be set to disable ("0") (USB reference voltage control bit is ignored).



Note 1: This flowchart only shows steps that are related to the USB function.
Note 2: This routine is a subroutine called up in the main routine.
Note 3: Shaded area indicates User Process.

Figure 2.7 USB Resume Processing Example (Main Routine)

2.4.3.1.Remote Wake-up

When reactivating the MCU in the suspend state with a source from the device side, send out a remote wake-up signal which will trigger a request for the host to reactivate operations.

The remote wake-up function in the 38K0 Group, outputs K state to the up-port for 10ms, and then stops the K state output.(10ms output time must be cleared by F/W.)

To reactivate the MCU in the suspend state using a device source, after the remote wake-up interrupt is generated, execute the device interrupt process at the same time the resume interrupt is generated. Then process the remote wake-up output. Figure 2.8 shows an example of the remote wake-up process routine.

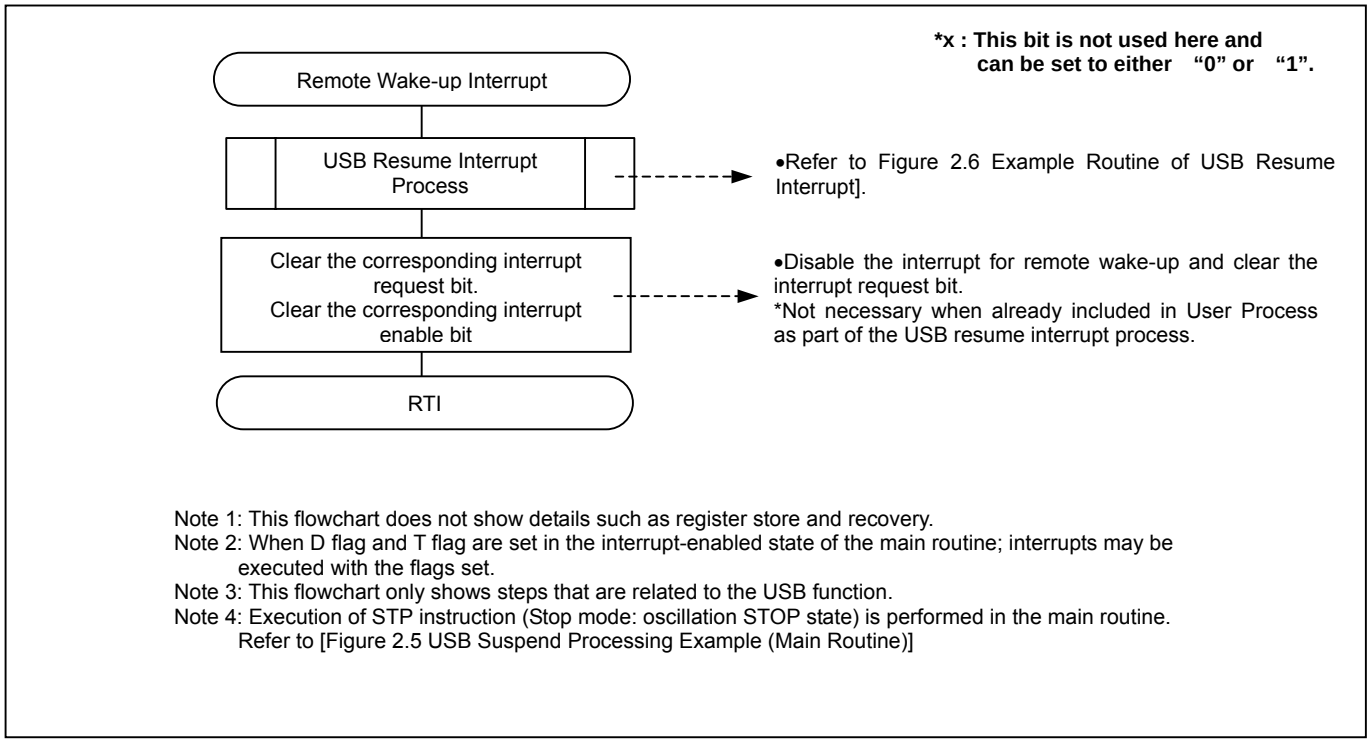


Figure 2.8 Example of Remote Wake-Up Interrupt Routine

2.5.USB SOF Interrupt

The USB SOF interrupt is used for isochronous transfers.

(1) Cause of USB SOF interrupt request

•The USB SOF interrupt request is generated when an SOF packet is received from the host by the USBDCU.

•If an SOF packet is sent from the host PC when the USB SOF interrupt enable bit of ICON1 (Interrupt Control Register) is “1”, a USB SOF interrupt is generated. If the SOF packet is has an error for some reason and cannot be received successfully within 250ns of the frame opening, a USB SOF interrupt will not be generated.

(2) Action when a USB SOF interrupt is detected

The frame numbers (11 bits) of the SOF packet received from the host are stored in frame number registers Low and High (FNUML, FNUMH) automatically by hardware.

(3) USB SOF interrupt settings

Set USB SOF interrupt enable bit of ICON1 to “1”.

(4) Conditions for accepting a USB SOF

A USB SOF interrupt will be accepted if all of the following conditions are fulfilled:

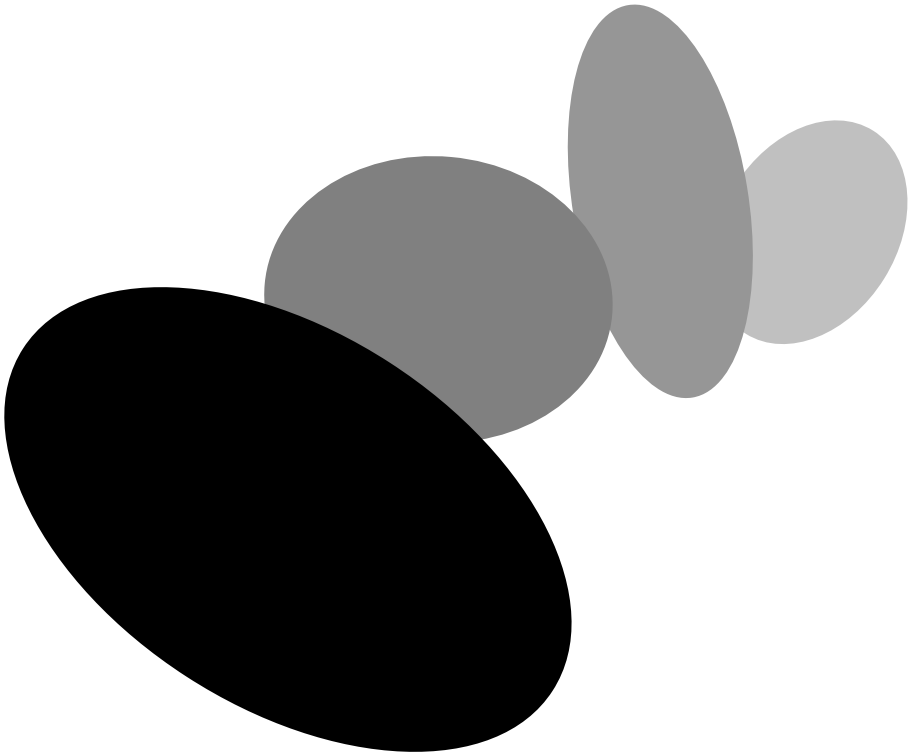
•I Flag (Interrupt Disable Flag) of the processor status register is “0” (interrupt enabled).

•The USB SOF interrupt enable bit of ICON1 “1” (enabled state).

•The USB SOF interrupt request bit of IREQ1 is “1” (interrupt requested).

Table 2.8 USB SOF Interrupt Registers

Address	Symbol	Register Name
003CH	IREQ1	Interrupt Request Register 1
003EH	ICON1	Interrupt Control Register 1



Chapter 3
USB Transference

This Chapter explains each transfer type.

3.1. Endpoint Setup Register

The 38K0 Group uses the following endpoints for USB transfer/receive operations: Endpoint0 for control transfers, Endpoints 1 to 3 for interrupt, bulk and isochronous transfers.

USB transfer/receive (endpoint) related registers are described in Tables 3.1 to 3.3. When using Endpoint0 or Endpoints 1 to 3 for USBINDEX (Endpoint Index Register), set the values indicated in Figure 3.1.

Table 3.1 Endpoint Index Register

Address	Symbol	Register Name
0018H	USBINDEX	Endpoint Index Register

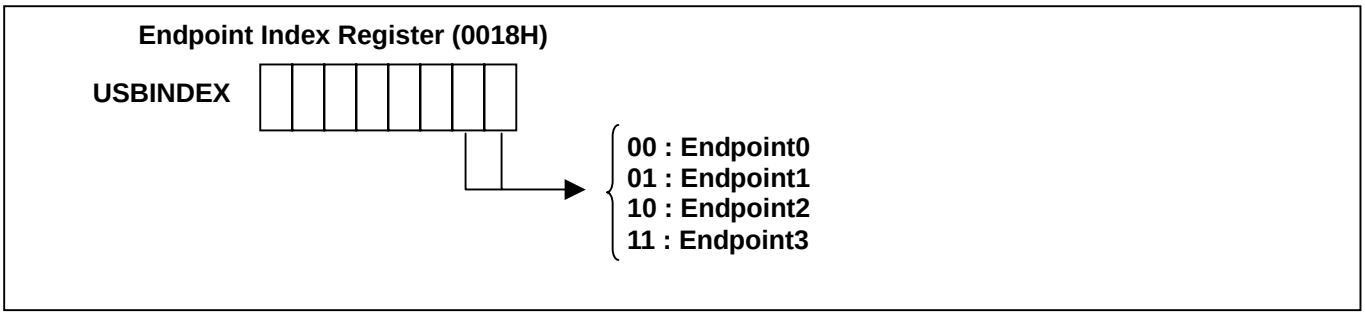


Figure 3.1 Endpoint Index Register Settings

Table 3.2 shows the registers required for setting Endpoint0 (control transfers).

The maximum packet size for control transfers is always set at 8 bytes. Set the top address of the Endpoint0 buffer in EP00BUF (EP00 Buffer Area Setup Register). The buffer consists of 8 bytes each of control command buffer and data buffer. For more details refer to [Chapter 3.2.2 Endpoint0 Buffer Area Setup].

When setting/referencing Endpoint0 registers, set “00” in USBINDEX before accessing the registers.

Table 3.2 USB Endpoint0 Registers

Address	Symbol	Register Name
0019H	EP00STG	EP00 Status Register
001AH	EP00CON1	EP00 Control Register 1
001BH	EP00CON2	EP00 Control Register 2
001CH	EP00CON3	EP00 Control Register 3
001DH	EP00REQ	EP00 Interrupt Source Register
001EH	EP00BYT	EP00 Transfer/Receive Byte No. Register
001FH	-	-
0FECH	-	-
0FEDH	EP00BUF	EP00 Buffer Area Setup Register

Registers necessary for setting Endpoints 1 to 3 (IN/OUT interrupt, bulk and isochronous transfers) are listed in Table 3.3.

Perform the transfer/receive settings with the EP0xCFG (EP0x Setup Register) in accordance with the descriptor settings of Endpoints 1 to 3. The buffer has 2 settings: single buffer mode and double buffer mode (alternating transfer of Data0 and Data1). Set the top address of Buffer 0 with EP0xBUF (EP0x Buffer Area Setup Register). Set the top address of Buffer 1 bit with BSIZ01 (Double Buffer Top Address Setup Bit of EP0xCFG) as the relative address. Refer to [Chapter 3.3.2 Endpoints 1 to 3 Buffer Area Settings] for more details.

Use EP0xCON1 (EP0x Control Register 1) to set responses for transfer/receive transmissions. Use EP0xCON2 and EP0xCON3 (EP0x Control Registers 2 and 3) to enable the buffers.

"x" represents either 1, 2, or 3. When setting/referencing an endpointx register, access the endpointx register after setting the endpoint value in USBINDEX (Endpoint Index Register).

Table 3.3 USB Endpointx Registers

Address	Symbol	Register Name
0019H	EP0xCFG	EP0x Setup Register
001AH	EP0xCON1	EP0x Control Register 1
001BH	EP0xCON2	EP0x Control Register 2
001CH	EP0xCON3	EP0x Control Register 3
001DH	EP0xREQ	EP0x Interrupt Source Register
001EH	EP0xBYT0	EP0x Transfer/Receive Byte No. Register 0
001FH	EP0xBYT1	EP0x Transfer/Receive Byte No. Register 1
0FECH	EP0xMAX	EP0x MAX Packet Size Register
0FEDH	EP0xBUF	EP0x Buffer Area Setup Register

3.2. Endpoint0

Endpoint0 is used to perform control transfers. Data is transferred or received in response to a device request from the host.

Endpoint0 has a control command buffer for the SETUP stage and a data buffer for the DATA stage. Refer to [Chapter 3.2.2 Endpoint0 Buffer Area] for more details.

A USB Endpoint0 interrupt (5 sources) is generated during Endpoint0 control transfers. Refer to [Chapter 3.2.3 Endpoint0 Interrupts] for more details.

3.2.1. Control Transfer Formats

The control transfer is a bi-directional transfer mainly used with setup commands. The transfer consists of a least two transaction-stages (SETUP, STATUS). A control transfer may also include a DATA stage between the SETUP and STATUS stages.

In USB transmissions, Endpoint0 has a response mechanism for various requests that is sent from the host through control transfers.

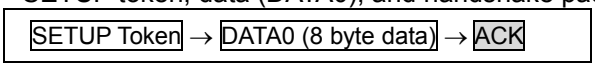
A control transfer consists of SETUP, DATA and STATUS stages. Data transfer and receive is performed in the DATA stage based on a SETUP stage request sent from the host. The control transfer ends when the STATUS stage is completed.

♦Control Transfer Transactions

The control transfer consists of the following three transaction types*1. The shaded blocks indicate data packets transmitted by a device.

(1) SETUP Stage:

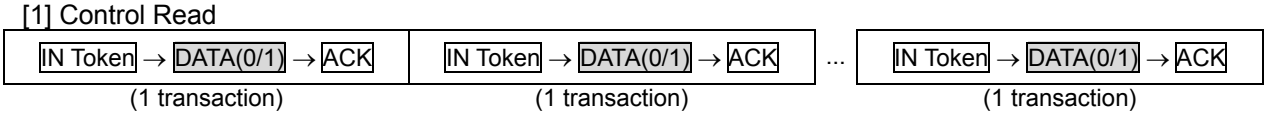
SETUP token, data (DATA0), and handshake packets.



(2) DATA Stage:

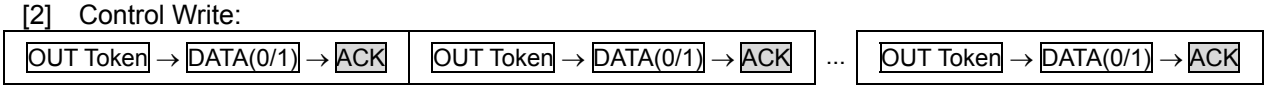
As in bulk transfers, the DATA transaction is repeated as many times as necessary.

[1] Control Read



(1 transaction) (1 transaction) (1 transaction)

[2] Control Write:

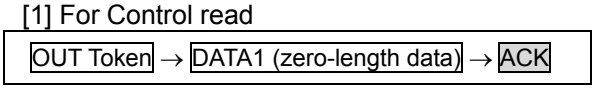


(1 transaction) (1 transaction) (1 transaction)

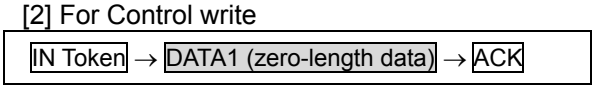
(3) STATUS Stage:

This transaction consists of an opposite-of-data-direction token packet and a zero-length DATA packet (DATA1).

[1] For Control read



[2] For Control write

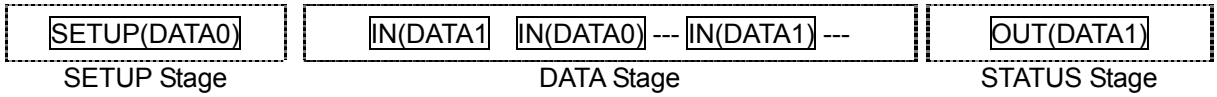


*1 (1),(2) and (3) is an example in normal transfer.

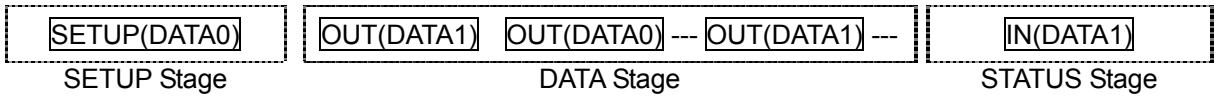
♦Control Transfer Sequences

The following three sequences are used for control transfers.

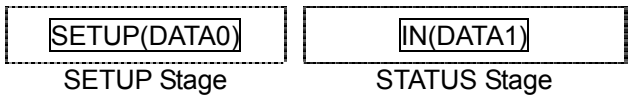
(1) Control read transfer:



(2) Control write transfer:



(3) Control write/no data transfer:



3.2.2. Endpoint0 Buffer Area Setup

The user needs to assign a buffer area for each endpoint in order to perform data transfer/receive.

Endpoint0 (control transfer) has a SETUP token control command buffer and an IN/OUT token data buffer. Each buffer (8 bytes) is stored in the RAM according to the values set by EP00BUF (EP00 Buffer Area Setup Register). Set the control command buffer top address in EP00BUF, as shown in Figure 3.2., and store the area in the RAM. An example of the setup is shown in Figure 3.3.

The top address in the control command buffer is 20H times the value set in EP00BUF. The top address in the data buffer is 20H times the value set in EP00BUF plus 8H.

See Figure 3.4 for an image of buffer access.

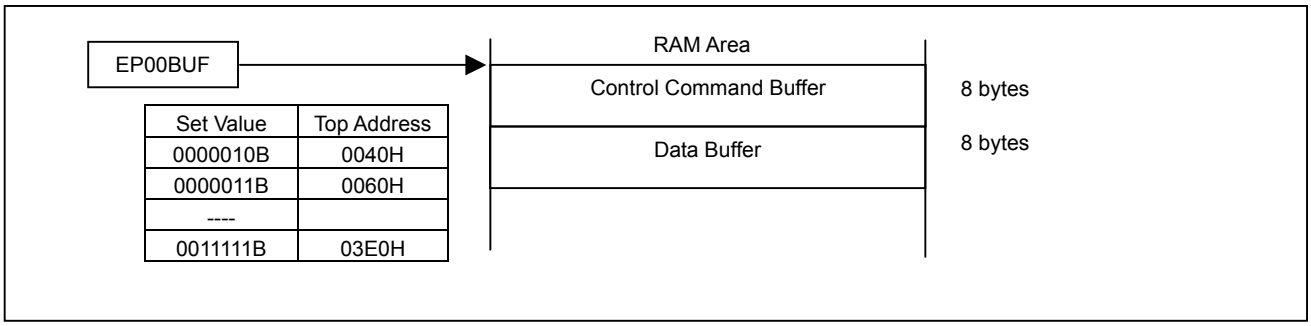


Figure 3.2 Endpoint0 Buffer

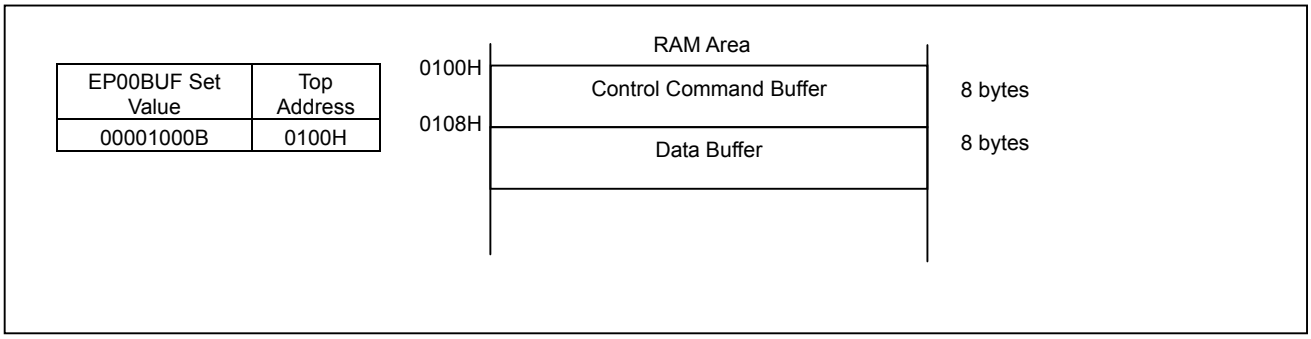


Figure 3.3 Example of Endpoint0 Buffer Setup

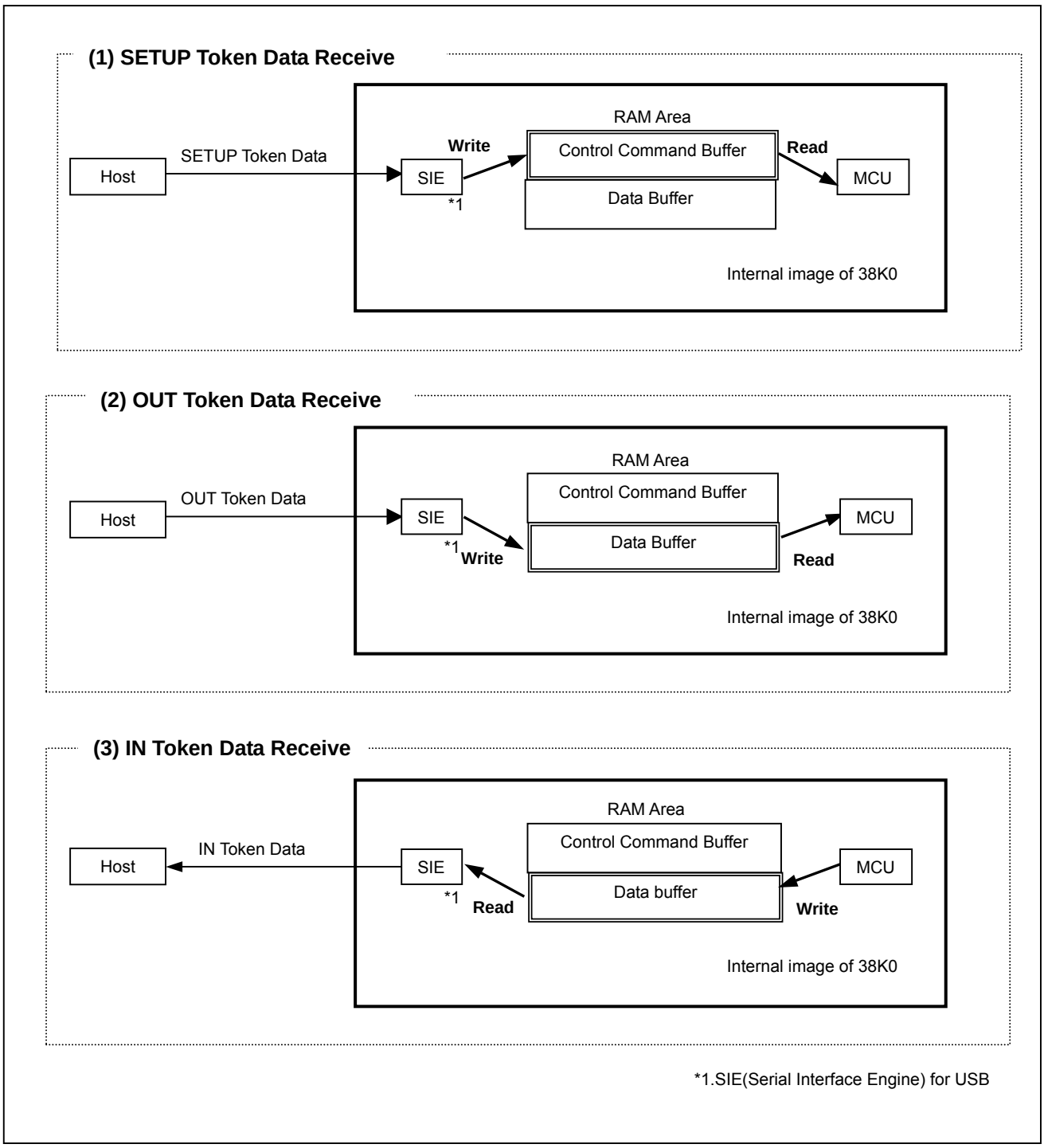


Figure 3.4 Endpoint0 Buffer Area Access

3.2.3. Endpoint0 Interrupts

Endpoint0 interrupts are used to control data flow during control transfers. Endpoint0 Interrupt Source Register is shown in Figure 3.5.

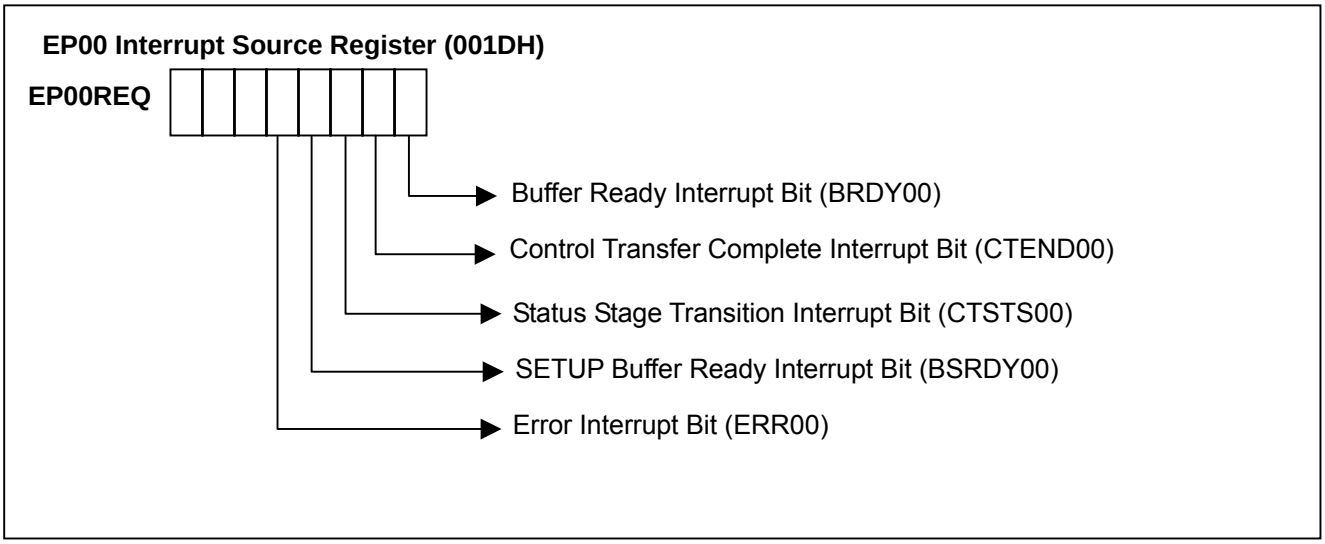


Figure 3.5 SEP00 Interrupt Source Register (EP00REQ)

(1) SETUP Buffer Ready Interrupt Bit (BRDY00)
This bit goes to “1” (H/W set) when the SETUP token buffer is in the ready state (read enabled). This bit must be cleared by F/W when an interrupt occurs. (this bit not cleared to “0” automatically by H/W.)

(2) Buffer Ready Interrupt Bit (BRDY00)
This bit goes to “1” (H/W set) when the data buffer is in the ready state (read/write enabled). This bit must be cleared by F/W when an interrupt occurs. (this bit not cleared to “0” automatically by H/W.)

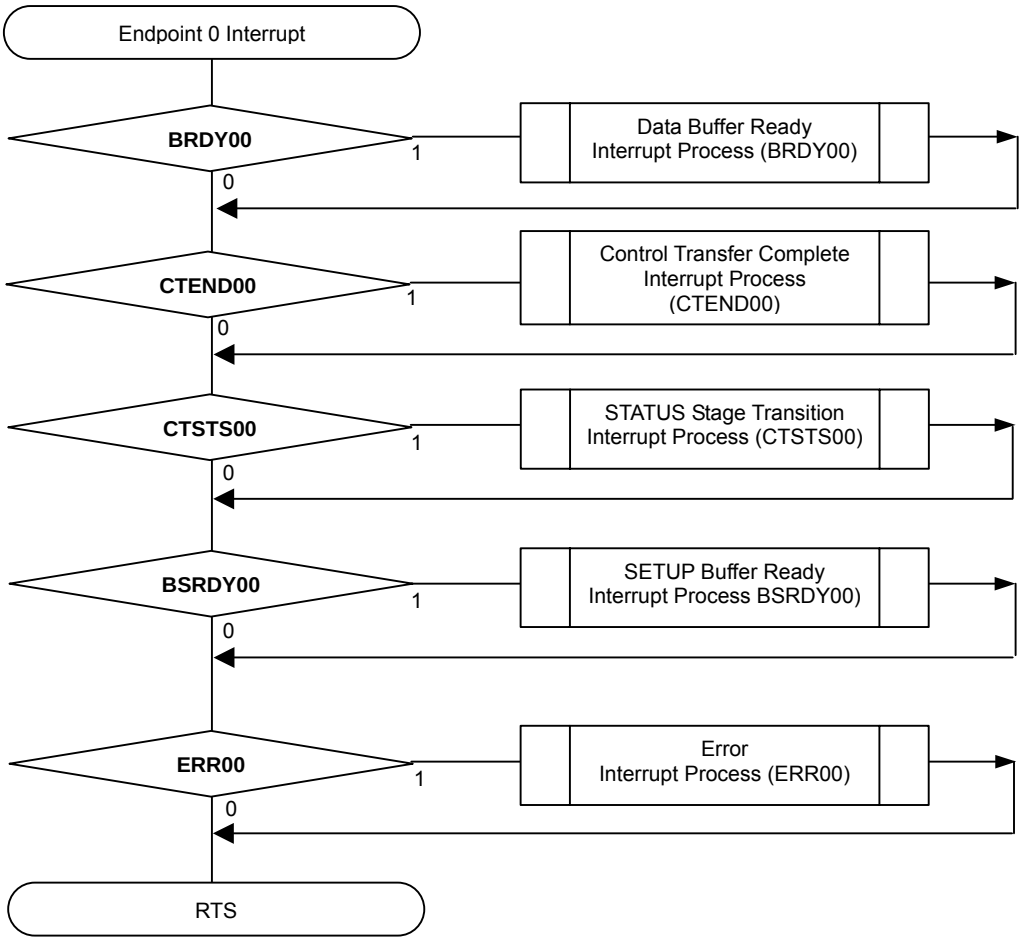
(3) Control Transfer Complete Interrupt Bit (CTEND00)
This bit goes to “1” (H/W set) when the control transfer is completed (NULL/ACK response in STATUS stage). This bit must be cleared by F/W when an interrupt occurs. (this bit not cleared to “0” automatically by H/W.)

(4) Status Stage Transition Interrupt Bit (CTSTS00)
This bit goes to “1” (H/W set) when CTENDE00 (Control Transfer Complete Enable Bit) of EP00CON3 (EP00 Control Register 3) is “0” (disabled).
Interrupt generation conditions:
- When an IN token is received in response to DATA stage (OUT) during a control transfer.
- When an OUT token is received in response to a DATA Stage (IN) during a control transfer.

*An interrupt will not be generated during a no-data transfer.
This bit must be cleared by F/W when an interrupt occurs. (this bit not cleared to “0” automatically by H/W.)

(5) Error Interrupt Bit (ERR00)
This bit goes to “1” (H/W set) when a control transfer error occurs.
This bit must be cleared by F/W when an interrupt occurs. (this bit not cleared to “0” automatically by H/W.) However, it is automatically cleared by H/W when a SETUP token is received.

Figure 3.6 shows Endpoint0 interrupt processing. Determine the interrupt source at each stage and then perform receive/transfer setup and buffer read/write. In the SETUP stage, each request is processed after the data is read out.



Note 1: Always judge the interrupt source bit in the order indicated above.
Note 2: This routine is a subroutine called in [Chapter 2.3 USB Device Interrupt Routine Example].

Figure 3.6 Example of Endpoint0 Interrupt Processing

3.2.4.Control Transfer Data Receive (Control Write Transfer)

When a request is received for a control write transfer, a SETUP token is received in the SETUP stage, followed by an OUT token in the DATA stage, ending with an IN token in the STATUS stage. An example of data receive (normal transfer) in a control transfer is shown in Figure 3.7. The following is a detailed explanation of the figure.

(1) Receiving a SETUP token in the SETUP stage

When a BSRDY00 interrupt is generated, read the data from the control command buffer. After the data is read, set CTENDE00 (Control Transfer Complete Enable Bit) of EP00CON3 (EP00 Control Register 3) to “1” and BVAL00 (Buffer Enable Bit) of EP00CON2 (EP00 Control Register 2) to “1”*[1]. BVAL00 must be enabled by setting PID00 (Response PID Bit) of EP00CON1 (EP00 Control Register 1) to “01” (auto response).

(2) Receiving an OUT token in the DATA stage

When a BRDY00 interrupt is generated, read the data from the control command buffer. After the data is read, set BVAL00 of EP00CON2 to “1”. (The BVAL00 bit sends a normal response (an ACK in response to the OUT token) and is automatically cleared by H/W..

(3) Receiving an IN token in the STATUS stage

The CTEND00 interrupt is generated. At this time, the CTENDE00 (Control Transfer Enable Bit) of EP00CON3 sends a response (sends an ACK in response to the IN token) and the bit is cleared automatically by H/W.

♦ Error during data receive from Host (for control write/read transfers)

An ERR00 interrupt is generated. At this time, PID00 of EP00CON1 is automatically set to “1x” (STALL response) by H/W. The STALL response is continuously sent in response to IN/OUT tokens in the DATA and STATUS stages. However, when the next SETUP stage starts, PID00 is automatically set to “00” (NAK response) by H/W, and the STALL is cancelled. ERR00 (Error Interrupt Bit) is cleared automatically by H/W when the SETUP token is received.

♦ Receiving an unsupported request (for control write/read transfers)

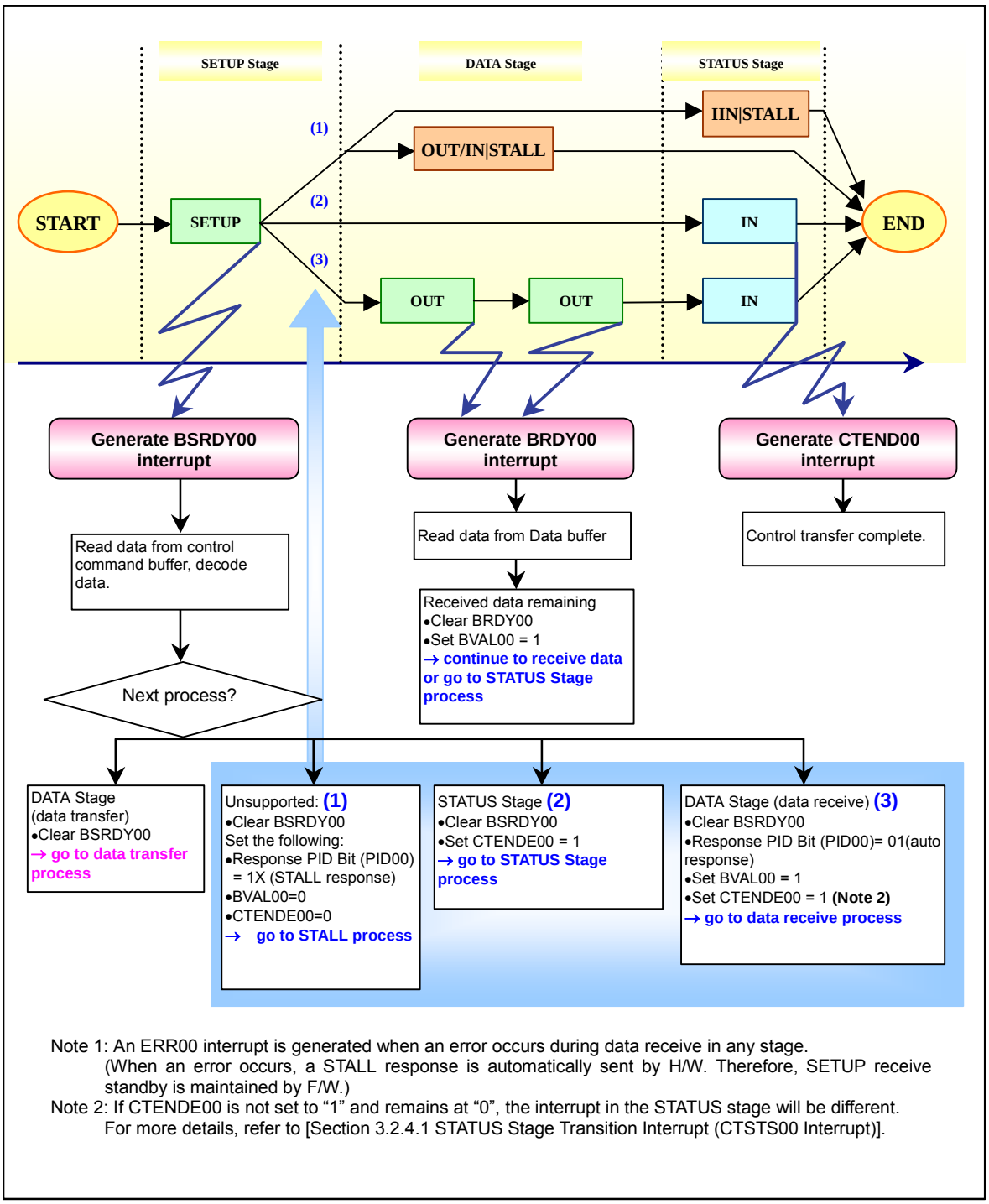
SetPID00 of EP00CON1 to “1x”. The STALL will continue to be sent in response to IN/OUT tokens in the DATA and STATUS stages. However, when the next SETUP stage starts, PID00 is automatically set to “00” (NAK response) by H/W, and the STALL is cancelled. ER00 is cleared automatically by H/W when the SETUP token is received.

♦ Receiving a SETUP token (for control write/read transfers)

The following bits are automatically set (cleared to “0”) by H/W when a SETUP token is received.

- PID00 (Response PID Bit) of EP00CON1 = “00”
  *An ACK is automatically sent in response to the SETUP token.
- BVAL00 (Buffer Enable Bit) of EP00CON2 = “0”
- CTENDE00 (Control Transfer Complete Enable Bit) of EP00CON3 = “0”
- ERR00 (Error Interrupt Bit) of EP00REQ (EP00 Interrupt Source Register) = “0”

*[1] “38K2 group USB sample firmware” has sample procedures (1) and (2).



Note 1: An ERR00 interrupt is generated when an error occurs during data receive in any stage.
(When an error occurs, a STALL response is automatically sent by H/W. Therefore, SETUP receive standby is maintained by F/W.)
Note 2: If CTENDE00 is not set to "1" and remains at "0", the interrupt in the STATUS stage will be different.
For more details, refer to [Section 3.2.4.1 STATUS Stage Transition Interrupt (CTSTS00 Interrupt)].

Figure 3.7 Example of Data Receive in Control Transfer (normal transfer)

3.2.4.1. STATUS Stage Transition Interrupt (CTSTS00 Interrupt)

The CTSTS00 interrupt is generated one time when the STATUS stage transition from Control stage is detected. By setting CTENDE00 (Control Transfer Complete Enable Bit) of EP00CON3 to “0”, the CTSTS00 (STATUS Stage Transition Interrupt Bit) interrupt will be generated.

Figure 3.8 shows an example of a control transfer receive when the CTSTS00 interrupt is generated. The following is a detailed explanation of the figure.

(1) Receiving a SETUP token in the SETUP stage

When a BSRDY00 interrupt is generated, read the data from the control command buffer. Set BVAL00 (Buffer Enable Bit) of EP00CON2 (EP00 Control Register 2) to “1”. BVAL00 must be enabled by setting PID00 (Response PID Bit) of EP00CON1 (EP00 Control Register 1) to “01” (auto response). In addition, BSRDY00 (SETUP Buffer Ready Interrupt Bit) must be cleared by F/W. By not setting CTENDE00 (Control Transfer Complete Enable Bit) of EP00CON3 to “1”, the CTSTS00 (STATUS Stage Transition Interrupt Bit) interrupt will be generated.

(2) Receiving an OUT token in the DATA stage

When a BRDY00 interrupt is generated, read the data from the control command buffer. After the data is read, set BVAL00 of EP00CON2 to “1”. (The BVAL00 bit sends a normal response (an ACK in response to the OUT token) and is automatically cleared by H/W. However, BRDY00 (Buffer Ready Interrupt Bit) must be cleared by F/W.

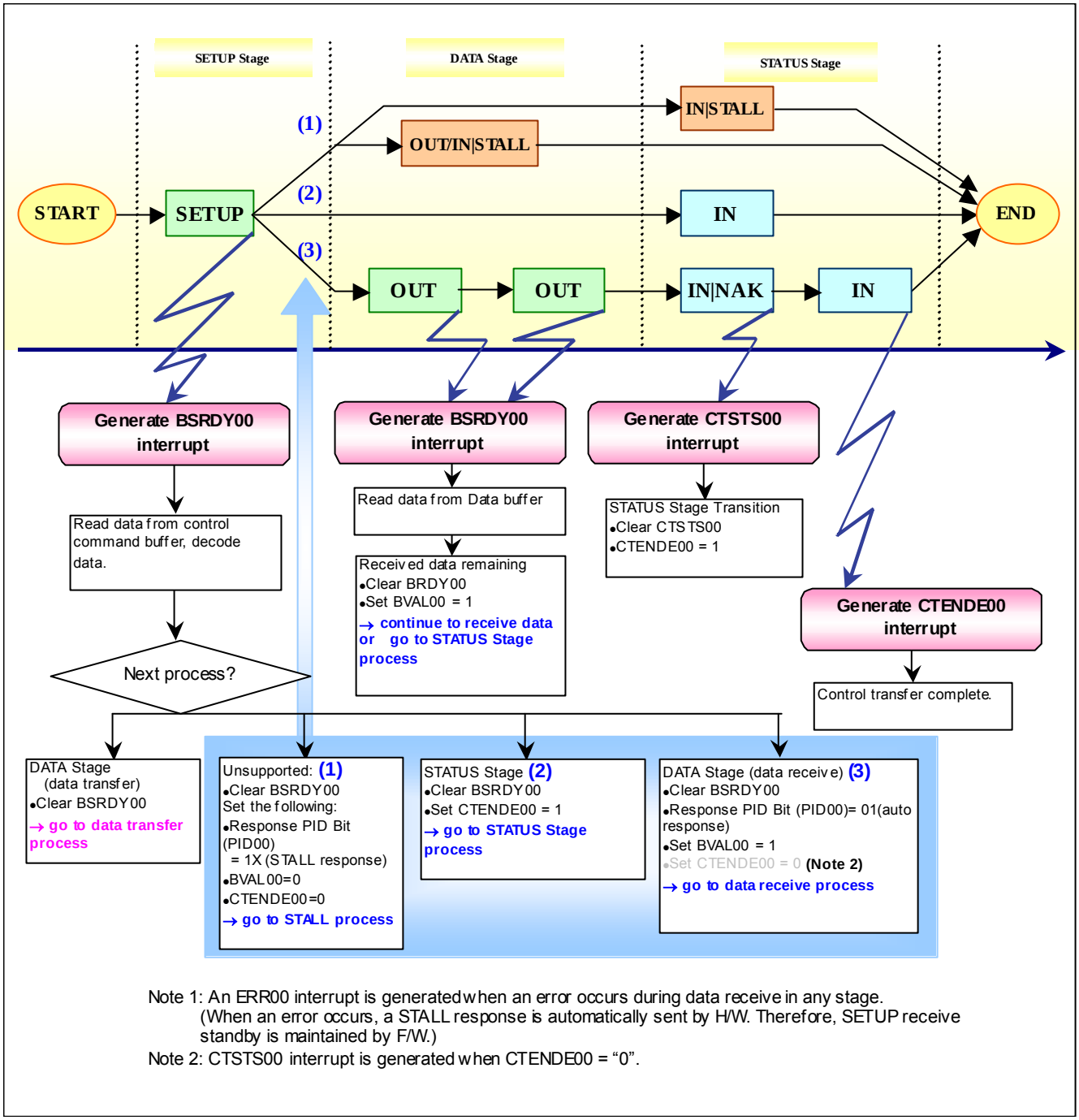
(3) Receiving an IN token in the STATUS Stage (send NAK)

The CTSTS00 interrupt is generated. Interrupt generation conditions require that the CTENDE00 is “0” and a NAK is sent in response to the IN token (sending a NAK indicates that the STATUS stage is not yet complete). However, even if these conditions continue, the CTSTS00 interrupt will only be generated in response to the first IN token. At this time, if the CTENDE00 (Control Transfer Enable Bit) of EP00CON3 is set to “1”, the CTEND00 interrupt will be generated at the next IN token. As mentioned above, the CTSTS00 interrupt is only generated once per data transfer sequence. To confirm the completion of a control transfer, a CTEND00 interrupt should be generated.

In addition, CTSTS00 (STATUS Stage Transition Interrupt Bit) must be cleared by F/W.

(4) Receiving an IN token in the STATUS stage (send ACK)

The CTEND00 interrupt is generated. At this time, the CTENDE00 (Control Transfer Enable Bit) of EP00CON3 sends a normal response (sends an ACK in response to the IN token) and the bit is cleared to “0” automatically by H/W.



Note 1: An ERR00 interrupt is generated when an error occurs during data receive in any stage.
(When an error occurs, a STALL response is automatically sent by H/W. Therefore, SETUP receive standby is maintained by F/W.)
Note 2: CTSTS00 interrupt is generated when CTENDE00 = "0".

Figure 3.8 Example of Data Receive in Control Transfer (normal transfer/CTSTS00 interrupt)

3.2.5. Control Transfer Data Send (Control Read Transfer)

When a request is received for a control read transfer, a SETUP token is received in the SETUP stage, followed by an IN token in the DATA stage, ending with an OUT token of the STATUS stage. An example of data receive in a control transfer is show in Figure 3.9. The following is a detailed explanation of the figure.

(1) Receiving a SETUP token in the SETUP stage

When a BSRDY00 interrupt is generated, read the data from the control command buffer. After the data is read, set CTENDE00 (Control Transfer Complete Enable Bit) of EP00CON3 (EP00 Control Register 3) to “1” and BVAL00 (Buffer Enable Bit) of EP00CON2 (EP00 Control Register 2) to “1”. BVAL00 must be enabled by setting PID00 (Response PID Bit) of EP00CON1 (EP00 Control Register 1) to “01” (auto response).

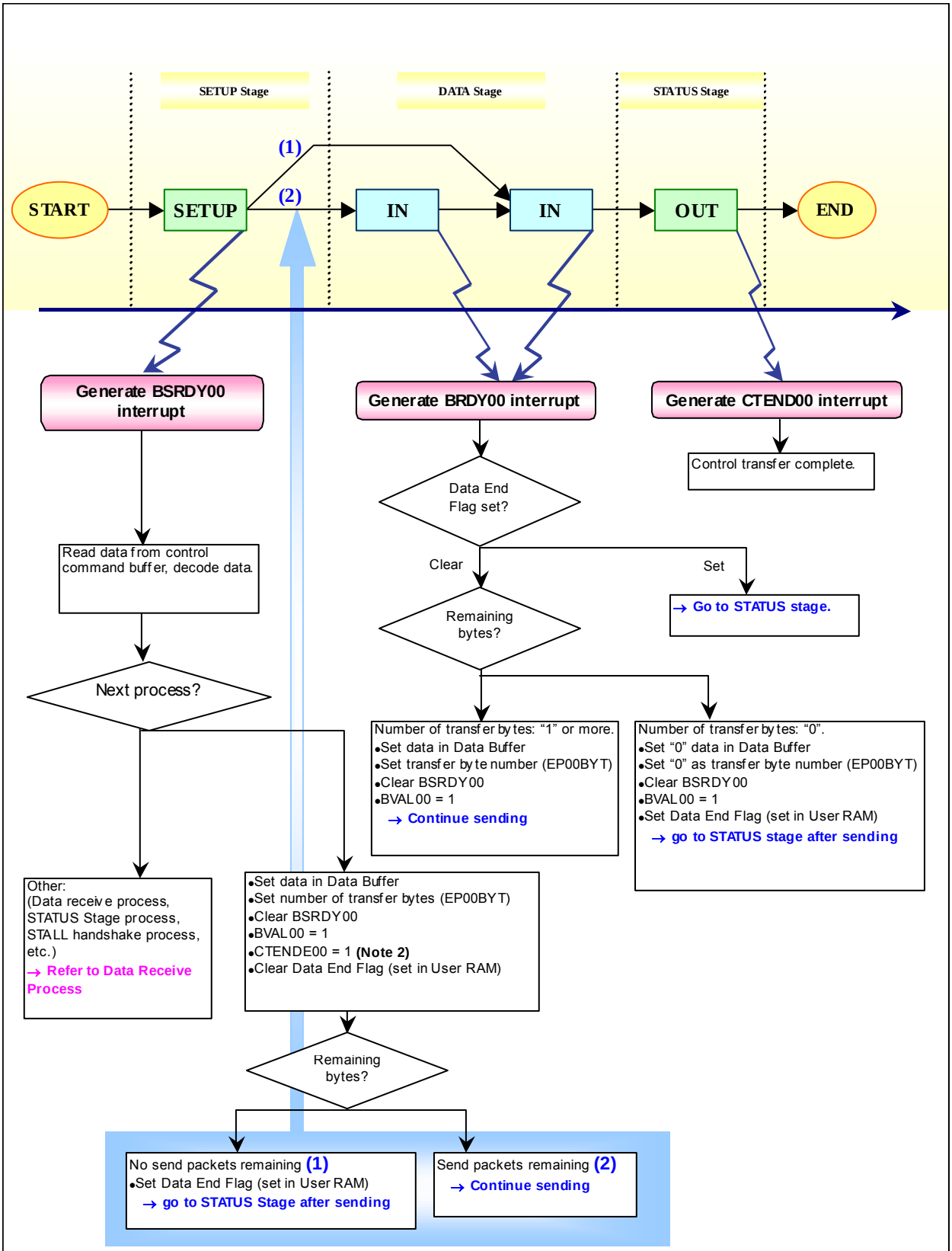
(2) Receiving an IN token in the DATA stage

When a BRDY00 interrupt is generated, write the data to the control command buffer. After the data is written, set BVAL00 of EP00CON2 to “1”. (The BVAL00 bit performs normal transmissions (receives an ACK in response to the OUT token) and is therefore automatically cleared by H/W.

Because there is no more data to be written when the BRDY00 interrupt of the last IN token is received, the BVAL00 does not need to be set to “1”.

(3) Receiving an OUT token in the STATUS stage

The CTEND00 interrupt is generated. At this time, the CTENDE00 (Control Transfer Enable Bit) of EP00CON3 performs normal transmissions (sends an ACK in response to the OUT token) and the bit is cleared to “0” automatically by H/W.



Note 1: An ERR00 interrupt is generated when an error occurs during data receive in any stage.
(When an error occurs, a STALL response is automatically sent by H/W. Therefore, SETUP receive standby is maintained by F/W.)
Note 2: If CTENDE00 is not set to "1" and remains at "0", the interrupt in the STATUS stage will be different.
For more details, refer to [Section 3.2.5.1 STATUS Stage Transition Interrupt (CTSTS00 Interrupt)].

Figure 3.9 Example of Data Send in Control Transfer (normal transfer)

3.2.5.1. STATUS Stage Transition Interrupt (CTSTS00 Interrupt)

For more details of CTSTS00 interrupt, refer to [Section 3.2.4.1 STATUS Stage Transition Interrupt (CTSTS00 Interrupt)]. Figure 3.10 shows an example of a control transfer data send when the CTSTS00 interrupt is generated. The following is a detailed explanation of the figure.

(1) Receiving a SETUP token in the SETUP stage

When a BSRDY00 interrupt is generated, read the data from the control command buffer. Set BVAL00 (Buffer Enable Bit) of EP00CON2 (EP00 Control Register 2) to “1”. BVAL00 must be enabled by setting PID00 (Response PID Bit) of EP00CON1 (EP00 Control Register 1) to “01” (auto response). In addition, BSRDY00 (SETUP Buffer Ready Interrupt Bit) must be cleared. By not setting CTENDE00 (Control Transfer Complete Enable Bit) of EP00CON3 (EP00 Control Register 3) to “1”, the CTSTS00 interrupt will be generated.

(2) Receiving an IN token in the DATA stage

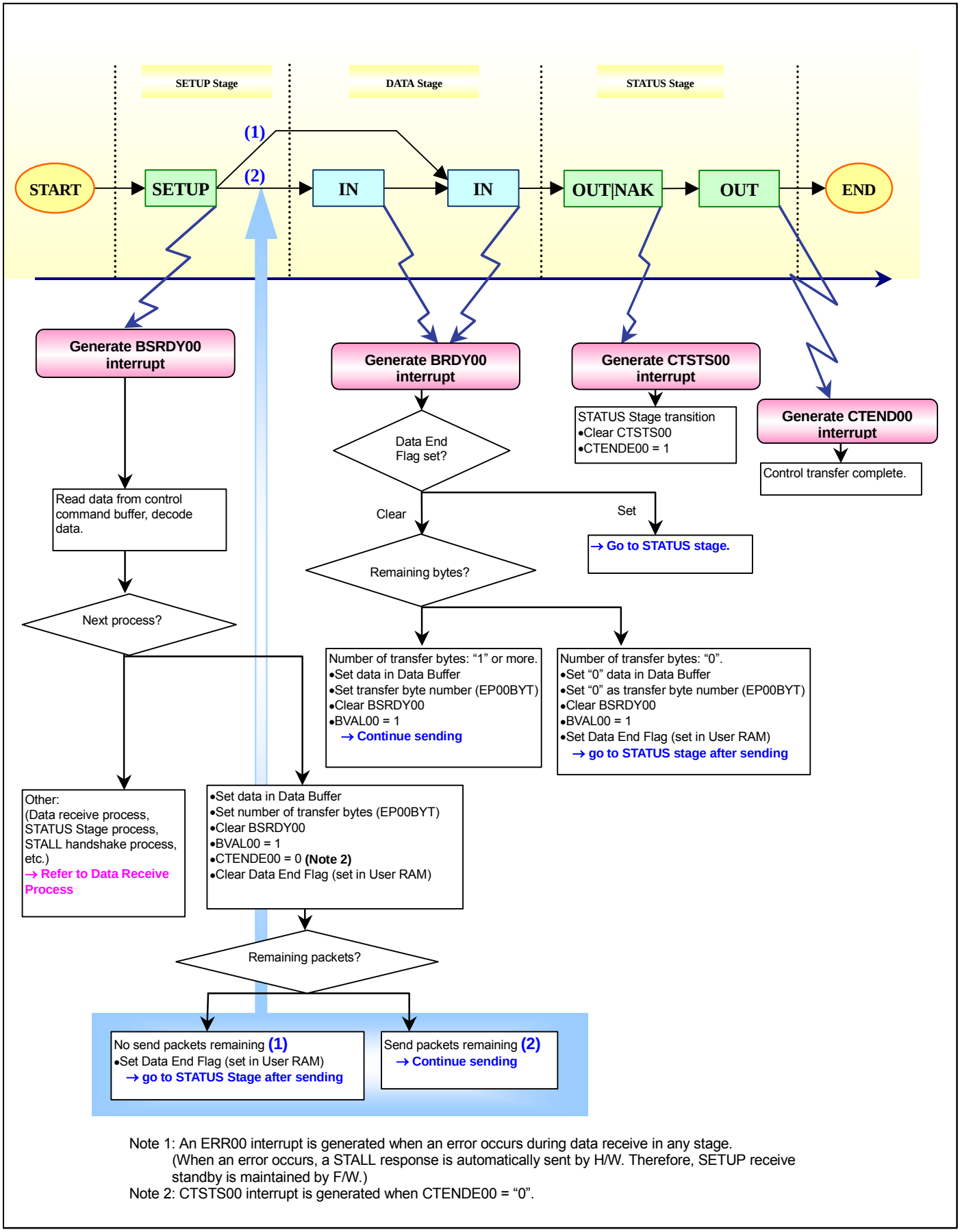
When a BRDY00 interrupt is generated, write the data to the data buffer. After the data is written, set BVAL00 of EP00CON2 to “1”. (The BVAL00 bit sends a normal response (an ACK in received in response to the IN token) and is therefore automatically cleared by H/W.

(3) Receiving an OUT token in the STATUS stage (send NAK)

The CTSTS00 interrupt is generated. Interrupt generation conditions require that the CTENDE00 is “0” and a NAK is sent in response to the OUT token (the NAK handshake indicates that the STATUS stage is not yet complete). However, even if these conditions continue to be met, the CTSTS00 interrupt will only be generated in response to the first IN token. At this time, if the CTENDE00 of EP00CON3 is set to “1”, a CTEND00 interrupt will be generated at the next IN token. As mentioned above, the CTSTS00 interrupt is only generated once per data transfer sequence. To confirm the completion of a control transfer, a CTEND00 interrupt should be generated.

(4) Receiving an OUT token in the STATUS stage (send ACK)

The CTEND00 interrupt is generated. At this time, the CTENDE00 of EP00CON3 performs normal transmissions (receives ACK in response to the OUT token) and the bit is cleared to “0” automatically by H/W.



Note 1: An ERR00 interrupt is generated when an error occurs during data receive in any stage.
(When an error occurs, a STALL response is automatically sent by H/W. Therefore, SETUP receive standby is maintained by F/W.)
Note 2: CTSTS00 interrupt is generated when CTENDE00 = "0".

Figure 3.10 Example of Data Send in Control Transfer (normal transfer/CTSTS00 interrupt)

3.3. Endpoints 1-3

Endpoints 1 to 3 manage three transfer types: interrupt, bulk, and isochronous. Each endpoint can handle bi-directional transfers: OUT (for receiving) and IN (for sending).

The user needs to assign data buffers in the RAM for Endpoints 1 to 3. Specify the top address of each data buffer with EP0xBUF (EP0x Buffer Area Setup Register). For more details, refer to [Chapter 3.2.2 Endpoint0 Buffer Area].

In order to configure the IN/OUT settings of Endpoints 1 to 3, the user must specify the transfer direction, transfer type, and MAX packet size for each endpoint descriptor. The transfer direction and type can be set with EP0xCFG (EP0x Set Register). The MAX packet size can be set with EP0xMAX (EP0x MAX Packet Size Register).

USB Endpointx interrupts (three sources) will occur when Endpointx is in any type of transfer operation. For more details, refer to [Chapter 3.3.3 Endpointx Interrupts].

3.3.1. Data Transfer Format

The USB transfer uses a half-duplex transfer and consists of at least two packets (token packet and data packet) per transfer. Transfers that support the retry function, guaranteeing valid data transfer between the Host and the device, consist of three packets: a handshake packet following the token and data packets. The three types of transfer supported by the USB function offer distinct characteristics. Isochronous transfer, which consists of 2 packets, does not detect a transfer error but does guarantee the transfer rate. Bulk transfer, which consists of 3 packets, detects a transfer error but does not guarantee the transfer rate. Interrupt transfer, which consists of 3 packets, detects a transfer error and guarantees the transfer rate.

♦ Data Transfer Transactions

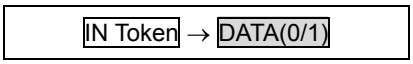
The following types of transactions classify data transfer*1. The shaded blocks indicate a packet transmitted by a device.

(1) Bulk IN and Interrupt IN:

This transaction consists of an IN token packet, data packets (DATA0/1), and a handshake packet.

(2) Isochronous IN:

This transaction consists of an IN token packet and a data packet (DATA0/1).

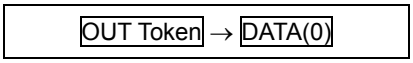


(3) Bulk OUT and Interrupt OUT:

This transaction consists of an OUT token packet, data packets (DATA0/1), and a handshake packet.

(4) Isochronous OUT

This transaction consists of an OUT token packet and a data packet (DATA0).



♦ Transactions according to Data Transfer Type

The following types of transactions are used to perform transfer data*2.

(1) Bulk IN and Interrupt IN Transfers:

(2) Isochronous IN Transfer:

(3) Bulk OUT and Interrupt OUT Transfers:

(4) Isochronous OUT Transfers:

*1 (1),(2),(3) and (4) is an example in normal transfer.

*2 (1),(2),(3) and (4) is an example in normal transfer and Handshake omits.

3.3.2. Buffer Area Setup for Endpoints 1– 3

The user needs to assign a data buffer in the RAM area for each endpoint in order to perform data transfer.

Endpoints 1 to 3 have two buffer modes: single buffer mode and double buffer mode. The buffer mode is selected by DBLB0x (Buffer Mode Setup Bit) of EP01CFG (EP0x Setup Register).

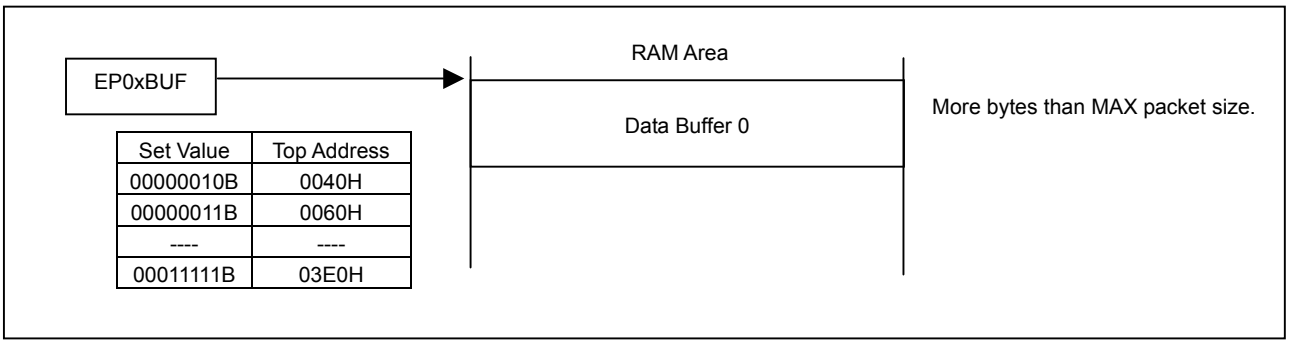
The data buffer area of each respective endpoint to be used must be assigned in the RAM area and the size (number of bytes) of the buffer must be larger than the MAX packet size of the respective endpoint descriptor.

The data buffer size of each endpoint, both IN and OUT, must be MAX 64 bytes(Single Buffer Mode).

[1] Single Buffer Mode

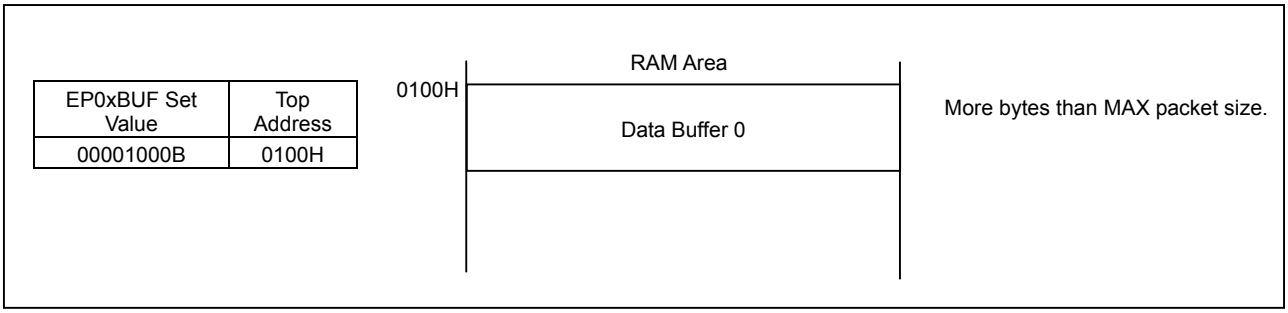
In the single buffer mode, Data Buffer 0 handles both DATA0 and DATA1, which are transferred alternately.

The Data Buffer 0 area of each respective endpoint to be used must be assigned in the RAM area and the size of the buffer must be larger than the MAX packet size of the respective endpoint descriptor. Figure 3.11 shows how to assign the Data Buffer 0 area in the RAM by setting the top address of the buffer in EP0xBUF (EP0x Buffer Area Setup Register). Figure 3.12 shows a setup example. The actual top address of the Data Buffer 0 area is 20H times the contents of EP0xBUF. Figure 3.13 shows an access model of the buffer.



Set Value	Top Address
00000010B	0040H
00000011B	0060H
----	----
00011111B	03E0H

Figure 3.11 Endpointx Data Buffer 0



EP0xBUF Set Value	Top Address
00001000B	0100H

Figure 3.12 Example of Endpointx Data Buffer 0 Setting

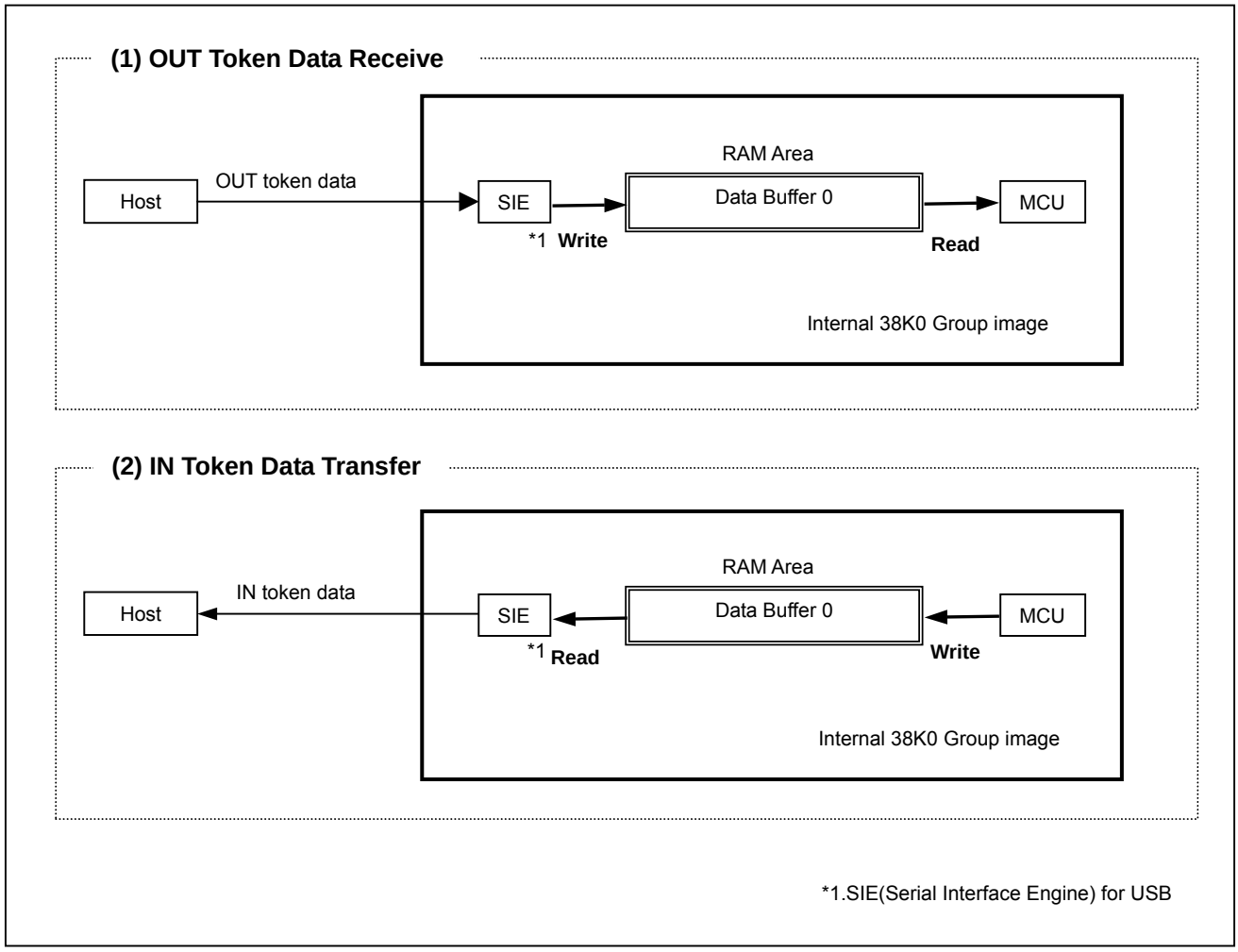


Figure 3.13 Endpointx Data Buffer 0 Access

[2] Double Buffer mode

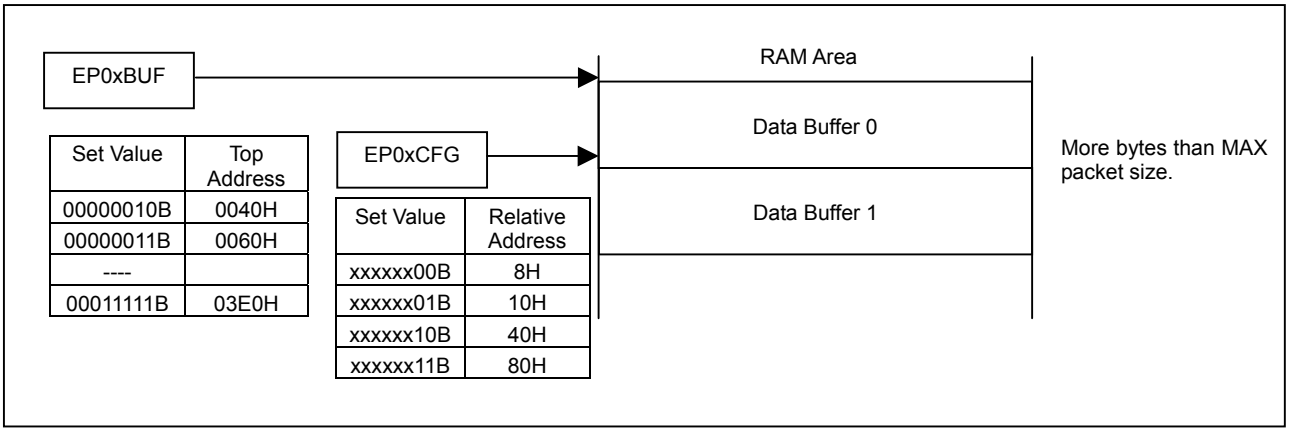
In the double buffer mode, data transfers are handled separately: DATA0 is transferred to Data Buffer 0 and DATA1 is transferred to Data Buffer 1 alternately.

Make sure the areas reserved for Data Buffer 0 and Data Buffer 1 on the RAM are larger than the MAX packet size of the descriptor for the endpoint to be used.

Set the Data Buffer 0 top address in EP0xBUF (EP0x Buffer Area Setup Register), as shown in Figure 3.14, and reserve the area on the RAM. Set the Data Buffer 1 top address in the Double Buffer Address Setup Bit of EP0xCFG (EP0x Buffer Area Setup Register), also shown in Figure 3.14, and reserve the area on the RAM. (See example in Figure 3.15.)

The top address of Data Buffer 0 is 20H times the value set in EP0xBUF. The top address of Data Buffer 1 is 20H times the value set in EP0xBUF plus the value set in EP0xCFG.

See Figure 3.16 for an image of the buffer access.

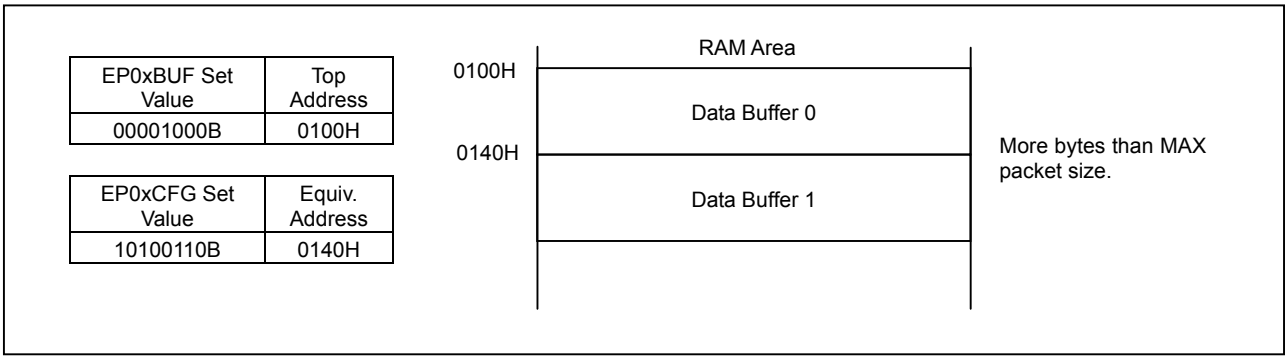


Set Value	Top Address
00000010B	0040H
00000011B	0060H

00011111B	03E0H

Set Value	Relative Address
xxxxxx00B	8H
xxxxxx01B	10H
xxxxxx10B	40H
xxxxxx11B	80H

Figure 3.14 Endpointx Data Buffer 0/1



EP0xBUF Set Value	Top Address
00001000B	0100H

EP0xCFG Set Value	Equiv. Address
10100110B	0140H

Figure 3.15 Example of Endpointx Data Buffer 0/1 Settings

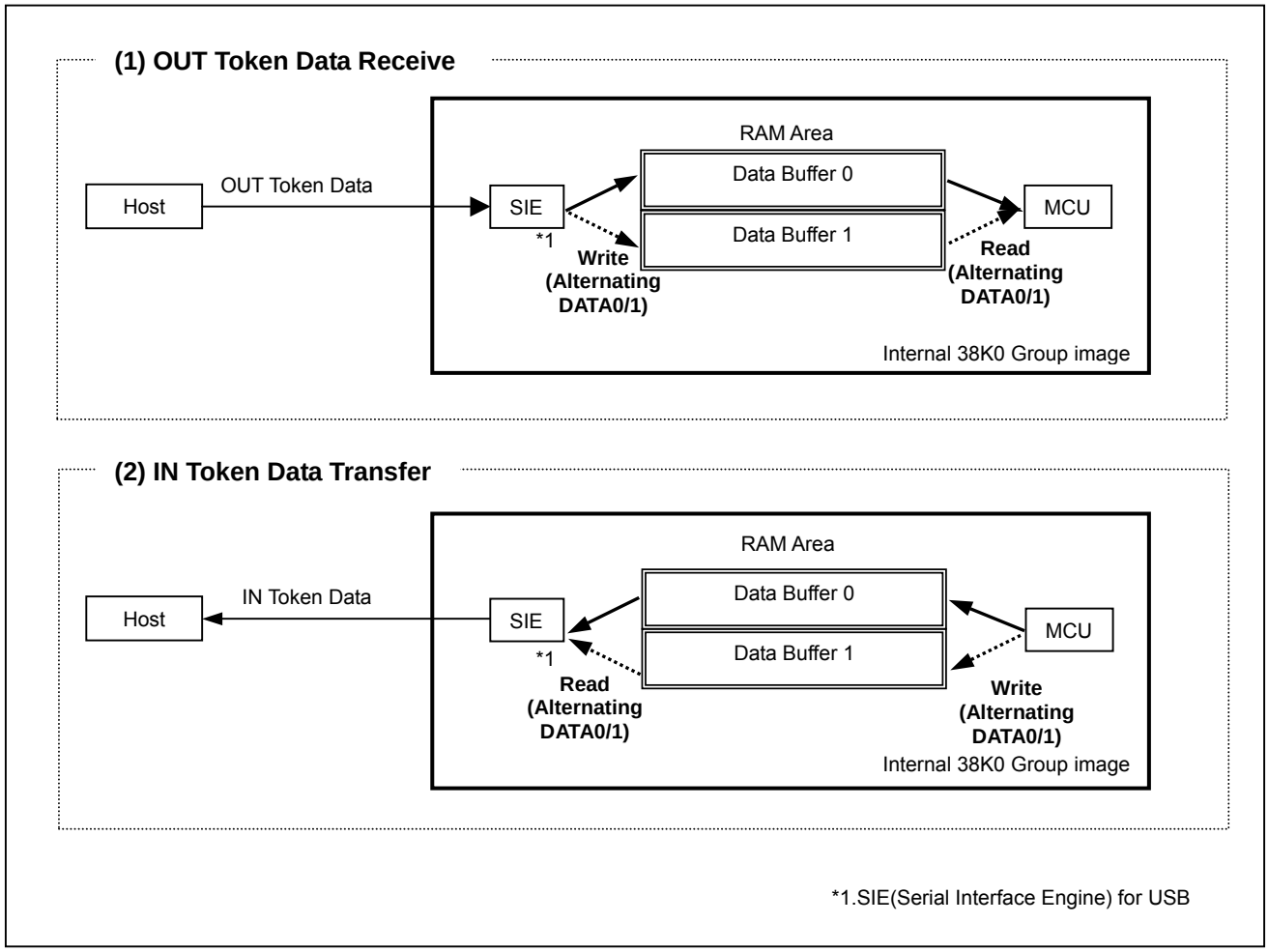


Figure 3.16 Endpointx Data Buffer 0/1 Access

3.3.3. Endpointx Interrupt

The Endpointx interrupt is used to control data flow during all three types of transfers: interrupt, bulk, and isochronous. Endpointx Interrupt Source Register is shown in Figure 3.17.

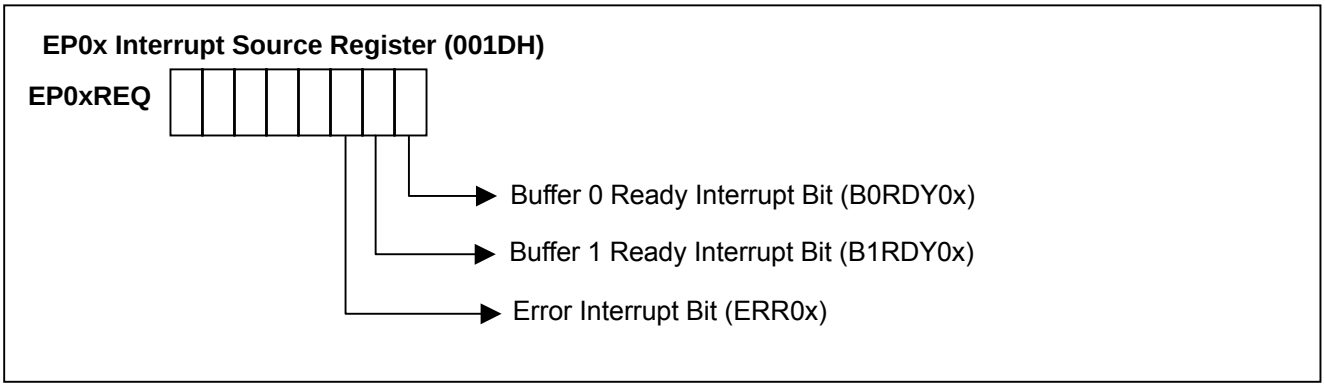


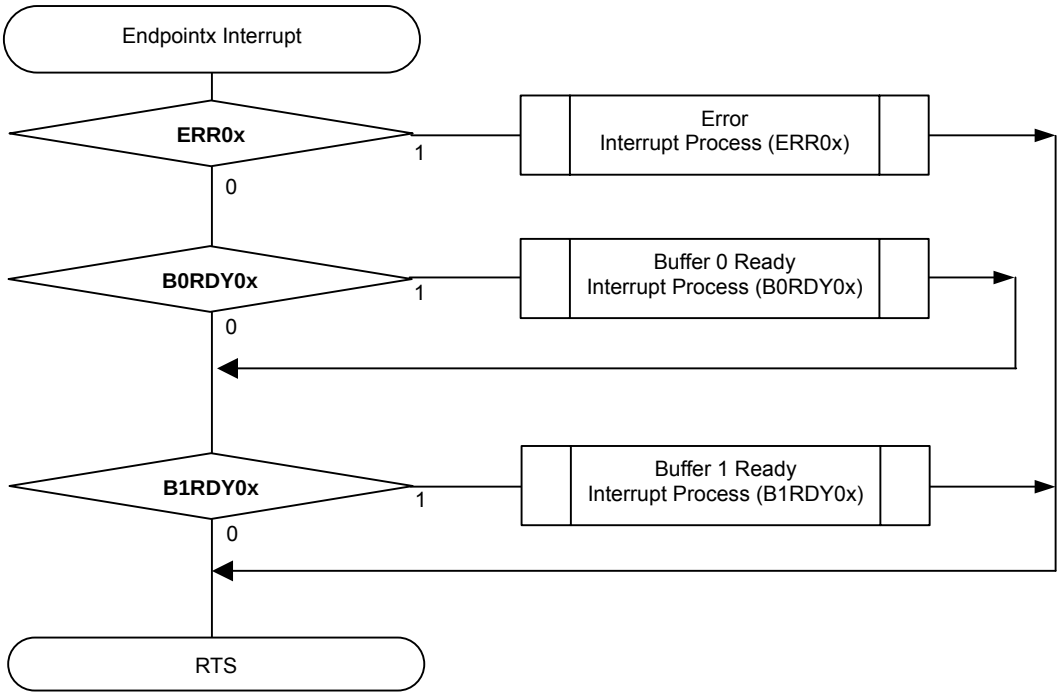
Figure 3.17 EP00 Interrupt Source Register (EP0xREQ)

(1) Buffer 0 Ready Interrupt Bit (B0RDY0x)
When Buffer 0 is in the ready state (read/write enabled state), this bit goes to “1” (set by H/W).
This bit must be cleared by F/W when an interrupt occurs. (this bit not cleared to “0” automatically by H/W.)

(2) Buffer 1 Ready Interrupt Bit (B1RDY0x)
In the double buffer mode, when Buffer 1 is in the ready state (read/write enabled state) this bit goes to “1” (set by H/W). (This bit is not valid in the single buffer mode.)
This bit must be cleared by F/W when an interrupt occurs. (this bit not cleared to “0” automatically by H/W.)

(3) Error Interrupt Bit (ERR0x)
This bit is set under the following conditions:
- When a MAX packet error occurs during a receive (OUT) operation.
  →The response PID is automatically set to STALL handshake (by H/W).
- When an error occurs during an isochronous transfer.

An example of Endpointx interrupt processing is shown in Figure 3.18. Determine the interrupt source ateach stage and then perform the error process, receive/transfer setup and buffer read/write



Note 1: Always determine the interrupt source bit in the order indicated above.
Note 2: This routine is a subroutine called in [Chapter 2.3 USB Device Interrupt Routine Example].

Figure 3.18 Example of Endpointx Interrupt Processing

3.3.4. Data Receive Format

(1) Receive Setup

Configure Endpointx by specifying the transfer direction, transfer type, and MAX packet size for the corresponding endpoint descriptor and matching the endpoint number with the descriptor.

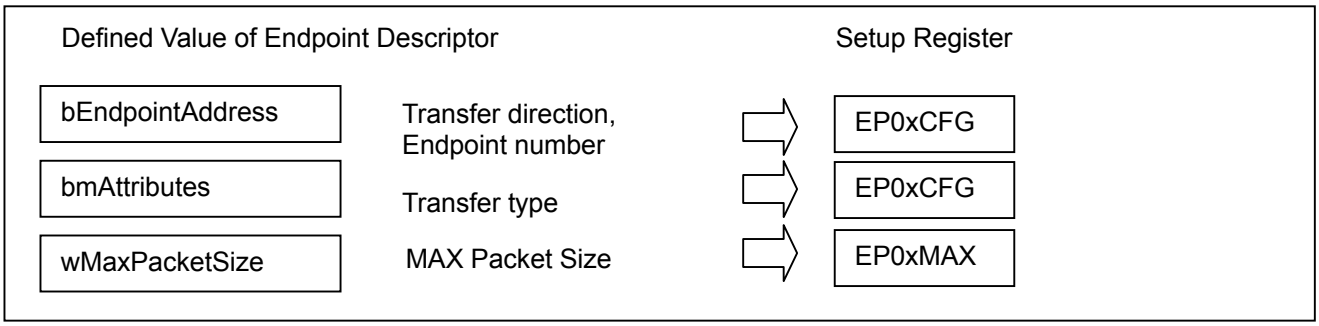


Figure 3.19 Endpoint Descriptor

Figure 3.20 shows an example of an Endpointx receive setup procedure.

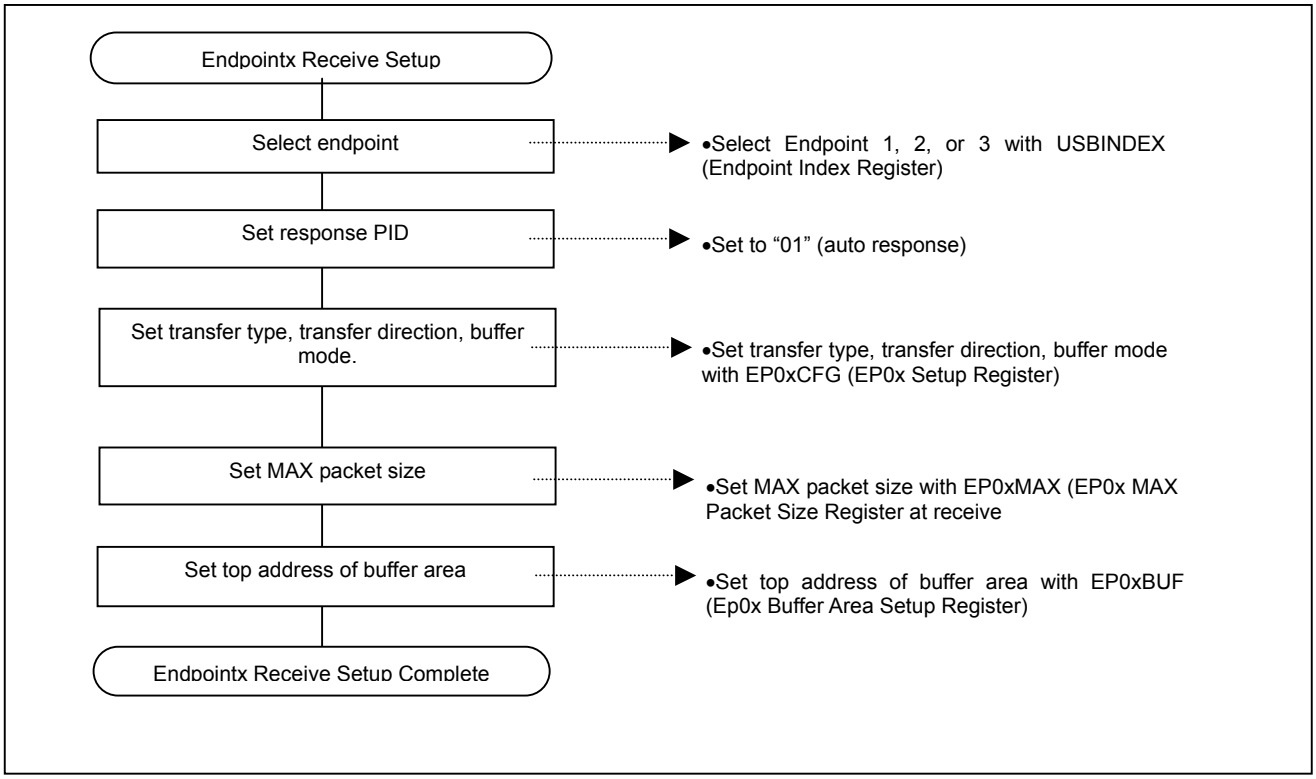


Figure 3.20 Example of Endpointx Receive Setup Procedure

(2) Normal Receive

[1] Single Buffer Mode

In the single buffer mode, the Endpointx Buffer Ready Interrupt is generated when Endpointx receives a valid packet from the Host. The number of bytes of data received is automatically set in EP0xBYT0 (EP0x Byte Number Register 0) by hardware. Read the same number of bytes of data from Data Buffer 0 as received by the endpoint, then set BOVAL0x to “1”. (The B0VAL0x bit is automatically cleared by H/W in normal receive transmissions.)

[2] Double Buffer Mode

When Endpointx receives a valid packet from the Host in the double buffer mode, if the packet is DATA0, the Endpointx Buffer 0 Ready interrupt is generated. The number of bytes of data received is automatically set in EP0xBYT0 by hardware. Read the same number of bytes of data from Data Buffer 0 as received by the endpoint, then set B0VAL0x (Buffer 0 Enable Bit) of EP0xCON2 to “1”. If the packet is DATA1, the Endpointx Buffer 1 Ready Interrupt is generated. The number of bytes of data received is automatically set in EP0xBYT0 by hardware. Read the same number of bytes of data from Data Buffer 1, then set B1VAL0x (Buffer 1 Enable Bit) of EP0xCON3 to “1”. (B0VAL0x/B1VAL0x bits are automatically cleared by H/W in normal receive transmissions.)

(3) Receive Error (when ERR0x interrupt occurs)

When Endpointx receives a packet of data from the Host which is larger than the MAX OUT packet size set in EP0xMAX (EP0x MAX Packet Size Register), a MAX packet error occurs, no handshake is returned, and an ERR0x interrupt is generated. At this time, PID0x (Response PID Bit) of EP0xCON1 is automatically set to “1x” (STALL handshake) by H/W. If a MAX packet error occurs at the next OUT token as well, the same sequence is repeated (no handshake is returned and an ERR0x interrupt is generated). For any other OUT (non-MAX packet error) or IN tokens, a STALL handshake is returned. When a STALL is sent, communications are disabled unless the Host CPU cancels the STALL with the ClearFeature. Even when communications are restarted, the STALL is not cancelled unless the PID0x bit is set to “00” or “01”.

When an error occurs in an isochronous transfer, an ERR0x interrupt is generated regardless of any IN/OUT packets received.

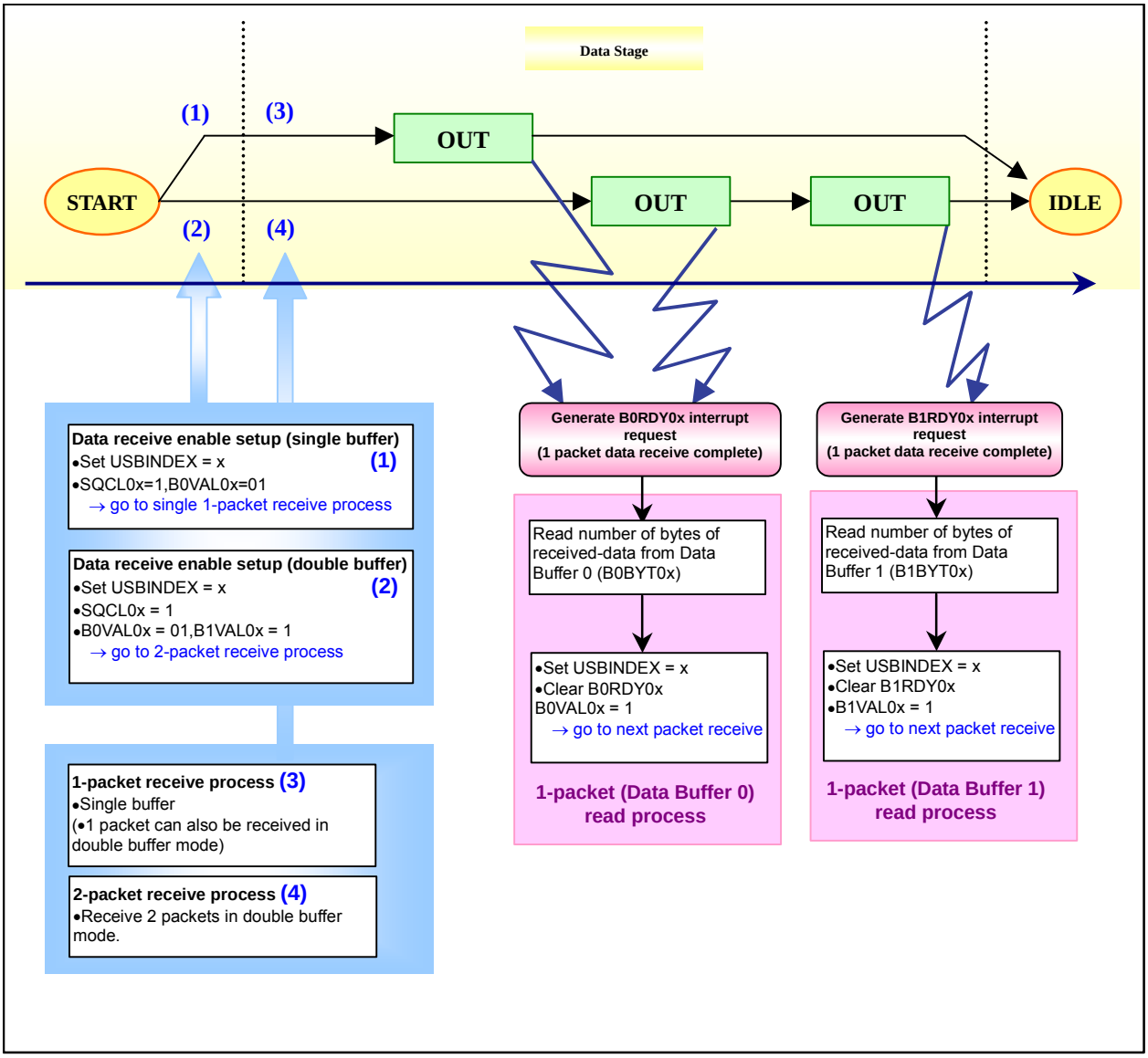


Figure 3.21 Example of Endpointx Data Receive

3.3.5. Bulk Transfer Data Receive

(1) Transfer Type Setup

To use Endpointx OUT for bulk transfers, set the endpoint to bulk transfer with EP0xCFG (EP0x Setup Register). Refer to the data receive setup procedure in [Figure 3.2. Example of Endpointx Receive Setup Procedure].

(2) Data Receive Ready

Set SQCL0x (Sequence Toggle Bit Clear Bit) to "1". By setting this bit to "1", the toggle bit is cleared and the next data PID is initialized to DATA0.

Next, set B0VAL0x (Buffer 0 Enable Bit) to "1" to put the bit in the data receive-enabled state. In the double buffer mode, B1VAL0x (Buffer 1 Enable Bit) also needs to be set to "1" to enable DATA1 receive.

(3) Data Receive Operation

An example of Endpointx bulk data receive is shown in Figure 3.22.

The bulk OUT transfer, which sends data from the Host CPU to the device, repeats the OUT transaction as many times as necessary. When Endpointx receives a valid packet from the Host, the Endpointx Buffer 0 Ready interrupt or Endpointx Buffer 1 Ready interrupt (in double buffer mode only) is generated. In the handshake phase of each transaction, if the send-side successfully receives the ACK packet issued by the receive-side, DATA0 and DATA1 of the data packet in the next data phase are toggled.

However, if the ACK is not received successfully, the following response is generated.

- If the received data includes an error or the MAX packet error is generated, no response is issued.
- If the endpoint is stalled, a STALL handshake is returned.
  (When PID0x (Response PID Bit) is "1x", the endpoint is stalled.)
- If there is a sequence bit mismatch in the received data, an ACK packet is returned.
- If Data Buffer 0 or 1 is full, a NAK packet is returned.

If the Host sends two packets of data from the same toggle, an ACK is returned for both packets, but the second data packet will not be stored in the data buffer. In this case, the ACK returned to the Host for the first packet is dropped and the Host assumes that the same data was sent in both packets.
Error processing covers error checks in accordance with USB Specification Ver.2.0, such as CRC check and bit stuffing. When an error is detected in the bulk OUT transfer, it is ignored. All error processing is performed by hardware and does not need to be controlled by software.

The following are details for operations in single and double buffer modes.

[1] Single Buffer Mode

When Endpointx receives a valid packet from the Host, the Endpointx Buffer 0 Ready interrupt is generated. The number of bytes of received data is automatically set in EP0xBYT0 (EP0x Byte Number Register 0) by hardware. Read the same number of bytes from Data Buffer 0, then set B0VAL0x (Buffer 0 Enable Bit) of EP0xCON2 (EP0x Control Register 2) to "1". (B0VAL0x bit is automatically cleared by hardware in normal receive transmissions.)

When the data is received in the following order, data is read out from Data Buffer 0 alternately. DATA0 → DATA1 → DATA0…

[2] Double Buffer Mode

When Endpointx receives a valid DATA0 packet from the Host in the double buffer mode, the Endpointx Buffer 0 Ready interrupt is generated. The number of bytes of received data is automatically set in EP0xBYT0 by hardware. Read the same number of bytes from Data Buffer 0, then set B0VAL0x of EP0xCON2 to "1". If the received packet is DATA1, the Endpointx Buffer 1 Ready Interrupt is generated. The number of bytes of received data is automatically set in EP0xBYT1 (EP0x Byte Number Register 1) by hardware. Read the same number of bytes from Data Buffer 1, then set B1VAL0x (Buffer 1 Enable Bit) of EP0xCON3 (EP0x Control Register 3) to "1". (B0VAL0x and B1VAL0x bits are automatically cleared by hardware in normal receive operations.)

When the data is received in the following order, DATA0 is read out from Data Buffer 0 and DATA1 is read out from Data Buffer 1 alternately. DATA0 → DATA1 → DATA0…

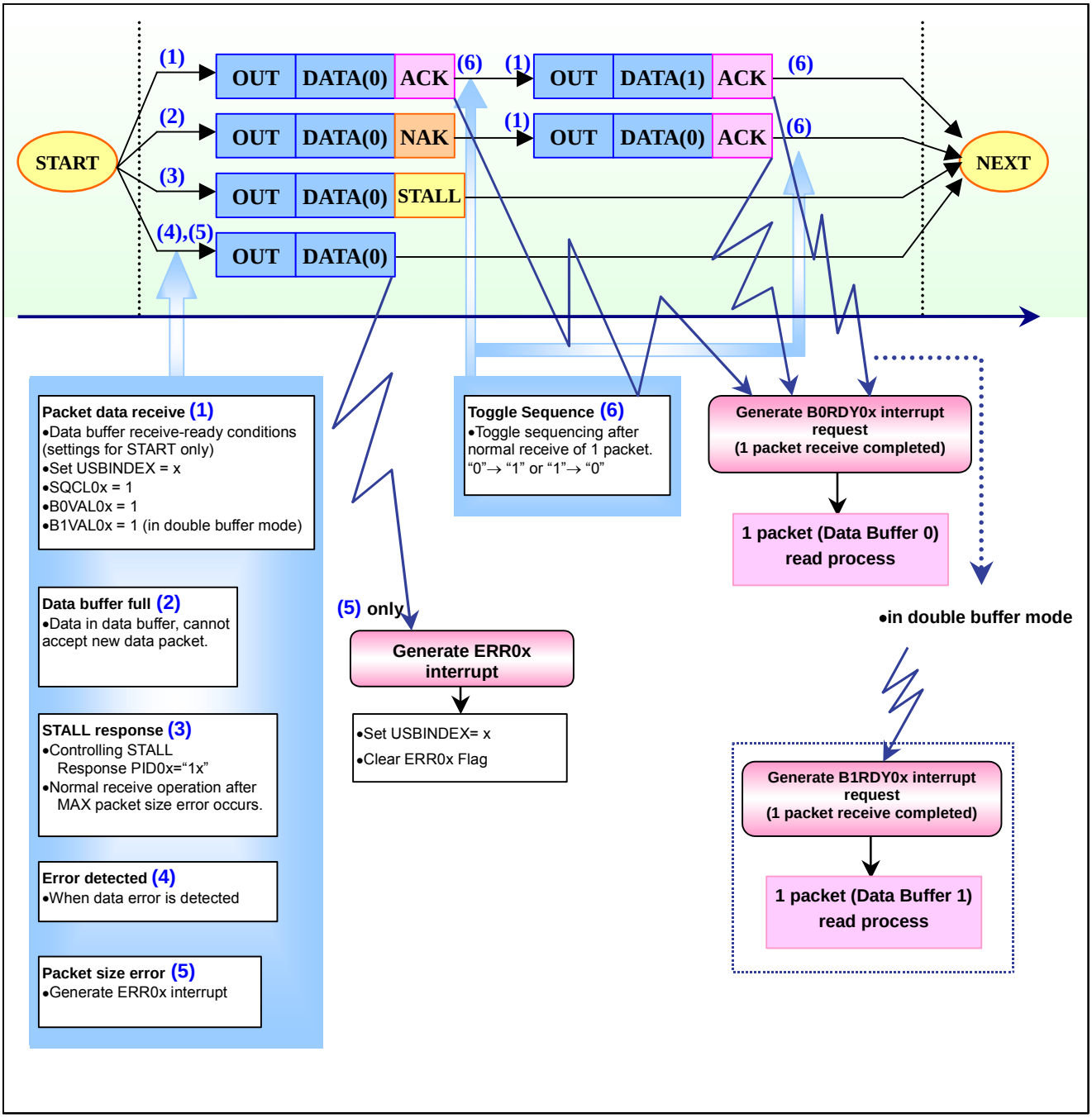


Figure 3.22 Example of Endpointx Bulk Receive

• Example of S/W Process in Double Buffer Mode

As shown in Figure 3.23, when using the double buffer mode, if an interrupt request is generated for the first packet but the interrupt is not processed (the buffer is not read) due to current execution of another process, both interrupt requests, B0RDY0x and B1RDY0x, are generated when an interrupt request is generated for the second packet.
At this time, when processing both interrupt requests, the user needs to toggle DATA0 and DATA1 with software accordingly (DATA0→DATA1 or DATA1→DATA0) so that the data buffers will be read in the appropriate order. See Figure 3.23 for an example of the software processing.

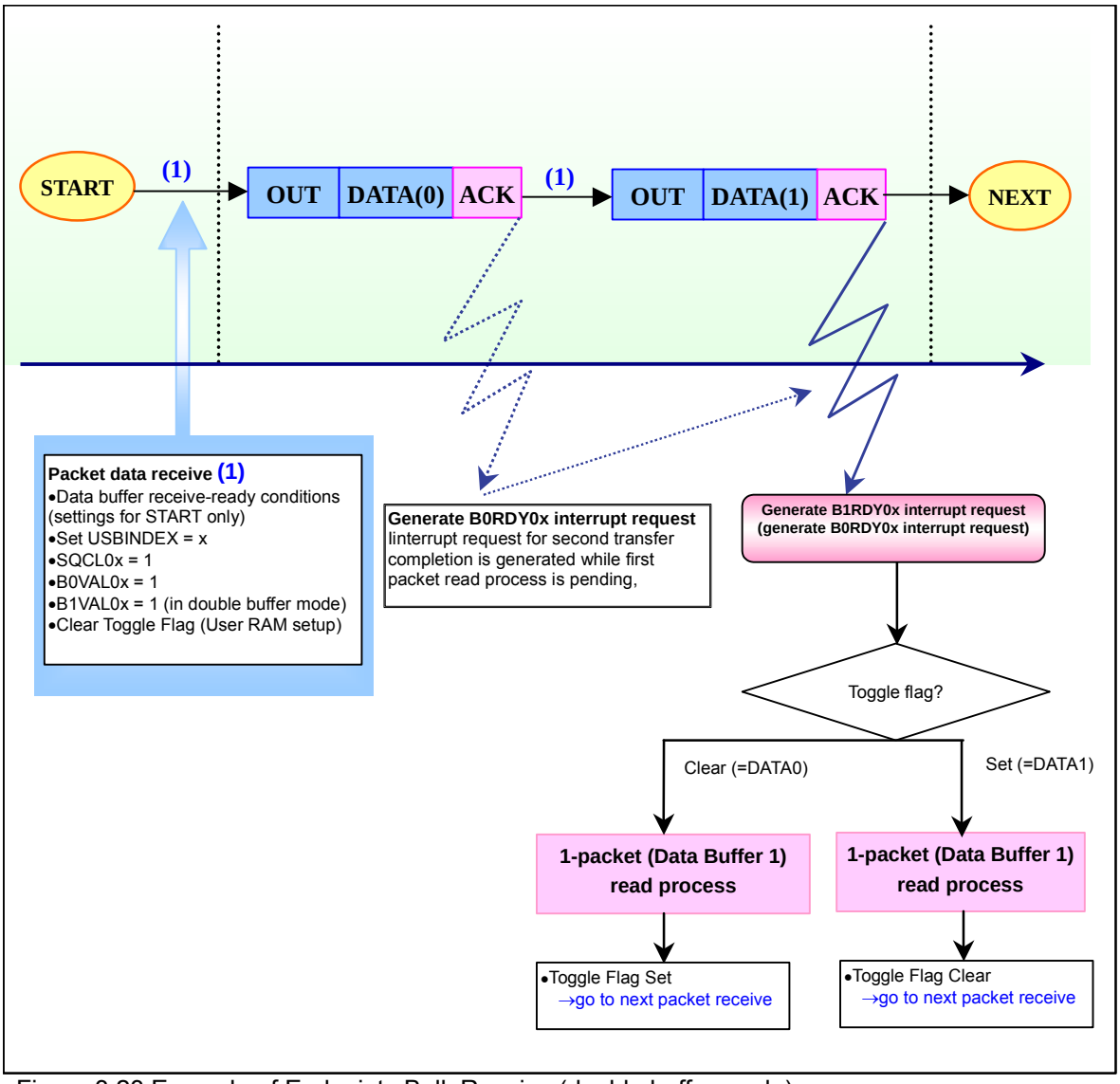


Figure 3.23 Example of Endpointx Bulk Receive (double buffer mode)

3.3.6. Interrupt Transfer Data Receive

(1) Transfer Type Setup

To use Endpointx OUT for interrupt transfers, set the endpoint to interrupt transfer with EP0xCFG (EP0x Setup Register). Refer to the procedure in [Figure 3.20 Example of Endpointx Receive Setup Procedure].

(2) Data Receive Ready

Preparation for interrupt transfer data receive is the same as that for bulk transfers. Refer to [Chapter 3.3.5 Bulk Transfer Data Receive].

(3) Data Receive Operation

Endpointx OUT operation in interrupt transfers is the same as that for bulk transfers. Refer to [Chapter 3.3.5 Bulk Transfer Data Receive].

3.3.7. Isochronous Transfer Data Receive

(1) Transfer Type Setup

To use Endpointx OUT for isochronous transfers, set the endpoint to isochronous transfer with EP0xCFG (EP0x Setup Register). Refer to the procedure in [Figure 3.20 Example of Endpointx Receive Setup Procedure].

(2) Data Receive Prep

Set SQCL0x (Sequence Toggle Bit Clear Bit) to "1". By setting this bit to "1", the toggle bit is cleared and the next data PID is initialized to DATA0.

Next, set B0VAL0x (Buffer 0 Enable Bit) to "1" to put the bit in the data receive-enabled state. In the double buffer mode, B1VAL0x (Buffer 1 Enable Bit) also needs to be set to "1" to enable DATA1 receive.

(3) Data Receive Operation

An example of Endpointx isochronous data receive is shown in Figure 3.24.

The isochronous OUT transfer, which transfers data from the Host CPU to the device, repeats the OUT transaction as many times as necessary. The isochronous transaction does not include a handshake phase (the device does not return an ACK or NAK to the Host). The isochronous transfer only involves data packet DATA0; there is toggle sequence with DATA1.

When Endpointx receives a valid packet from the Host, an Endpointx Buffer 0 Ready interrupt or Buffer 1 Ready interrupt (in double buffer mode only) is generated.

When there is data in Data Buffer 0/1 and a new data packet cannot be accepted, the ERR0x interrupt (as an overrun error) is generated.

Detailed explanations of single buffer and double buffer mode operations are provided below.

[1] Single Buffer Mode

When Endpointx receives a valid packet from the Host, the Endpointx Buffer 0 Ready interrupt is generated. The number of bytes of received data is automatically set in EP0xBYT0 (EP0x Byte Number Register 0) by hardware. Read the same number of bytes from Data Buffer 0, then set B0VAL0x (Buffer 0 Enable Bit) of EP0xCON2 (EP0x Control Register 2) to "1". (B0VAL0x bit is automatically cleared by hardware in normal receive operations.)

[2] Double Buffer Mode

When Endpointx receives a valid packet from the Host, if the packet begins with an even number (starting from packet number 0), the Endpointx Buffer 0 Ready interrupt is generated. The number of bytes of received data is automatically set in EP0xBYT0 (EP0x Byte Number Register 0) by hardware. Read the same number of bytes from Data Buffer 0, then set B0VAL0x (Buffer 0 Enable Bit) of EP0xCON2 (EP0x Control Register 2) to "1". If the next packet is odd-numbered, the Endpointx Buffer 1 Ready interrupt is generated. The number of bytes of received data is automatically set in EP0xBYT1 (EP0x Byte Number Register 1) by hardware. Read the same number of bytes from Data Buffer 1, then set B1VAL0x (Buffer 1 Enable Bit) of EP0xCON3 (EP0x Control Register 3) to "1". (B0VAL0x and B1VAL0x bits are automatically cleared by hardware in normal receive operations.)

• Example of S/W Process in Double Buffer Mode

As shown in Figure 3.23, when using the double buffer mode, if an interrupt request is generated for the first packet but the interrupt is not processed (the buffer is not read) due to current execution of another process, both interrupt requests, B0RDY0x and B1RDY0x, are generated when an interrupt request is generated for the second packet.

At this time, when processing both interrupt requests, the user needs to manage the order in which Data Buffer 0/1 will be read. Although isochronous transfer OUT operations do not support the toggle sequence, use Figure 3.23 as an example of the software processing.

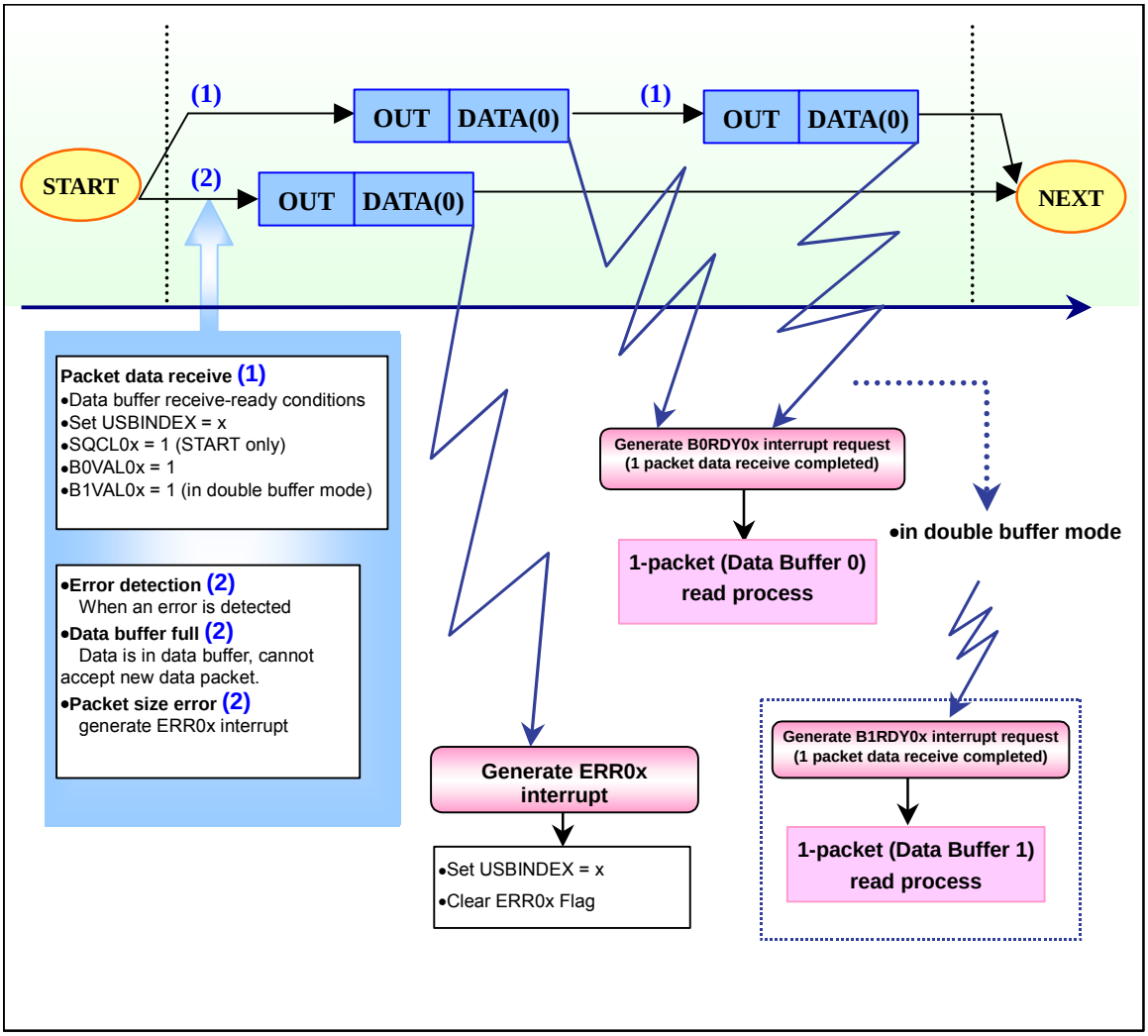


Figure 3.24 Example of Endpointx Isochronous Receive

3.3.8. Data Send Format

(1) Send Setup

Configure Endpointx by specifying the transfer direction, transfer type, and MAX packet size for the corresponding endpoint descriptor and matching the endpoint number with the descriptor.

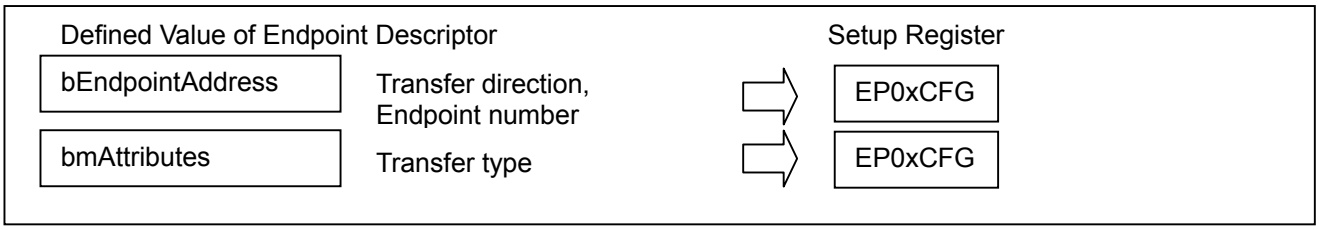


Figure 3.25 Endpoint Descriptor

Figure 3.26 shows an example of an Endpointx send setup procedure.

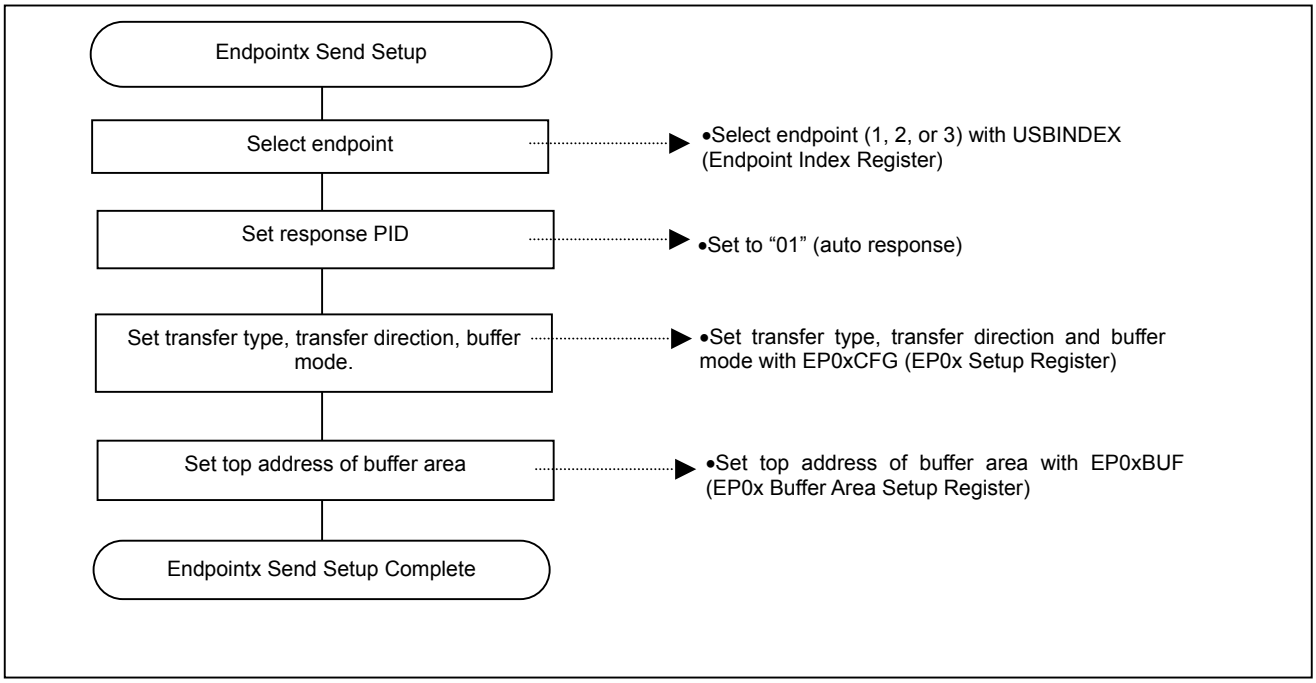


Figure 3.26 Example of Endpointx Send Setup Process

(2) Normal Send

[1] Single Buffer Mode

In the single buffer mode, for Endpointx to send a packet to the Host, prepare the packet data in Data Buffer 0 to be returned with the IN token from the Host.

To prepare one packet of data, confirm that Endpointx is not in the HALT state and that Data Buffer 0 is empty. After writing the data to Data Buffer 0 (the same number of bytes as the packet data to be sent), set B0VAL0x (Buffer 0 Enable Bit) of EP0xCON2 (EP0x Control Register 2) to “1”. (B0VAL0x bit is automatically cleared by H/W in normal receive transmissions.) The number of bytes of packet data to be sent must be set in EP0xBYT0 (EP0x Byte Number Register).

When one packet of data has been prepared, the data is sent with the next IN token from the Host. When this data send is complete, the Endpointx Buffer 0 Ready Interrupt Request is generated and Data Buffer 0 empties by one packet space.

[2] Double Buffer Mode

For Endpointx to send packets to the Host, prepare a packet of data (DATA0 in Data Buffer 0 and DATA1 in Data Buffer 1) to be returned with the IN token from the Host

To prepare the packets of data, confirm that Endpointx is not in the HALT state and that Data Buffer 0 is empty. For DATA0, after writing the data to Data Buffer 0 (the same number of bytes as the packet data to be sent), set B0VAL0x of EP0xCON2 to “1”. (B0VAL0x bit is automatically cleared by H/W in normal receive transmissions.) The number of bytes of packet data to be sent must be set in EP0xBYT0 (EP0x Byte Number Register).

For DATA1, after writing the data to Data Buffer1 (the same number of bytes as the packet data to be sent), set B1VAL0x of EP0xCON3 (EP0x Control Register 3) to “1”. (B1VAL0x bit is automatically cleared by H/W in normal receive transmissions.) The number of bytes of packet data to be sent must be set in EP0xBYT1 (Endpointx Buffer 1 Ready Interrupt).

When one packet of data has been prepared, the data is sent from the Host with the next IN token. When this data send is complete, Endpointx Buffer 0 (or 1) Ready Interrupt Request is generated and Data Buffer 0 (or 1) empties by one packet space.

(3) STALL Response

Set PID0x (Response PID Bit) of EP0xCON1 (EP0x Control Register 1) to “1x”. A STALL handshake is continually returned in response to IN/OUT tokens of the Endpointx in the STALL condition. When a STALL is sent, communications are disabled unless the Host CPU cancels the STALL with the ClearFeature. Even when communications are restarted, the STALL is not cancelled unless the PID0x bit is set to “00” or “01”.

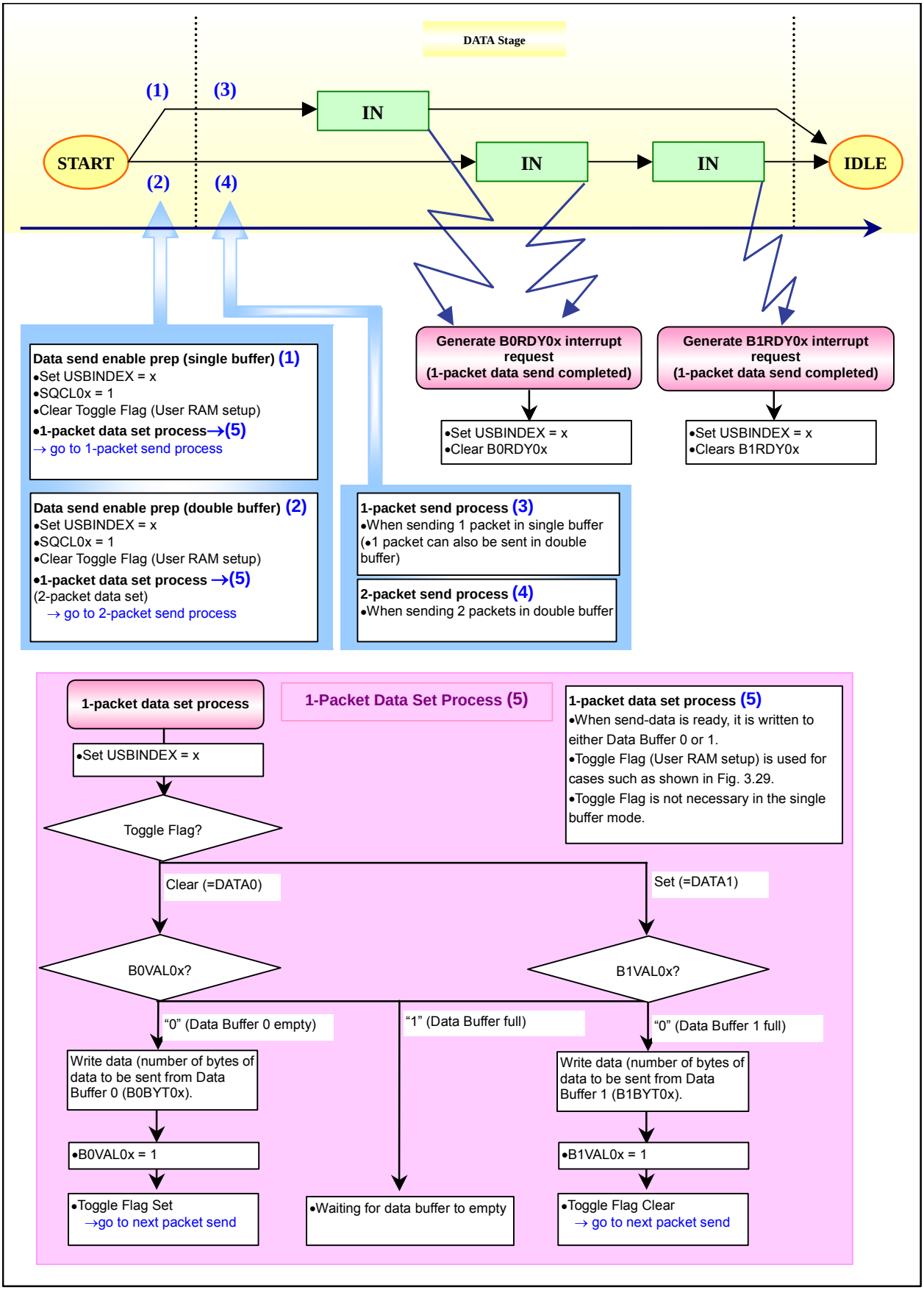


Figure 3.27 Example of Endpointx Data Send

3.3.9.Bulk Transfer Data Send

(1) Transfer Type Setup

To use Endpointx IN for bulk transfers, set the endpoint to bulk transfer with EP0xCFG (EP0x Setup Register). Refer to [Figure 3.26 Example of Endpointx Send Setup Procedure] for details.

(2) Data Send Prep

Set SQCL0x (Sequence Toggle Bit Clear Bit) to “1”. By setting this bit to “1”, the toggle bit is cleared and the next data PID is initialized to DATA0.

(3) Data Send Operation

An example of Endpointx bulk data send is shown in Figure 3.28.

Detailed explanations of single buffer and double buffer mode operations are provided below.

[1] Single Buffer Mode

A NAK handshake is automatically returned when an IN token is received from the Host but data is not yet set in Endpointx Data Buffer 0.

In order to send data, a packet data must be set in Data Buffer 0. Confirm that Endpointx is not in the HALT state and that Data Buffer 0 is empty (B0VAL0x Bit is “0”; write-enabled). Set the send packet data and set B0VAL0x bit to “1”. (B0VAL0x bit is automatically cleared by H/W in normal send transmissions.)
Set the number of bytes of packet data to be sent in EP0xBYT0 (EP0x Byte Number Register 0).

After the data is set, Endpointx IN sends the data to the Host upon receiving an IN token. The Host returns an ACK handshake in response to the data packet, completing the transmission of one packet, and the Endpointx Buffer 0 Ready Interrupt is generated.

In a bulk transfer, when an IN endpoint successfully receives an ACK handshake from the Host, DATA0 and DATA1 are toggled. But if the endpoint does not receive an ACK from the Host, the same data from the same toggle is sent in response to the next IN token.

When the data is to be sent in the following order, DATA0 is sent to Data Buffer 0 alternately. DATA0 → DATA1 → DATA0…

[2] Double Buffer Mode

A NAK handshake is automatically returned when an IN token is received from the Host but data is not yet set in Endpointx Data Buffer 0 or 1.

In order to send DATA0, confirm that Endpointx is not in the HALT state and that Data Buffer 0 is empty (B0VAL0x Bit is “0”; write-enabled). Set the send packet data and set B0VAL0x bit to “1”. (B0VAL0x bit is automatically cleared by H/W in normal send transmissions.)
Set the number of bytes of packet data to be sent in EP0xBYT0 (EP0x Byte Number Register 0).
For DATA1, confirm that Endpointx is not in the HALT state and that Data Buffer 0 is empty (B0VAL0x Bit is “0”; write-enabled), in the same manner as for DATA0. Set the send packet data and set B1VAL0x bit to “1”. (B1VAL0x bit is automatically cleared by H/W in normal send operations.)
Set the number of bytes of packet data to be sent in EP0xBYT1 (EP0x Byte Number Register 1).

After the data is set, Endpointx IN sends the data to the Host upon receiving an IN token. The Host returns an ACK handshake in response to the data packet, completing the transmission of one packet. At this time the Endpointx Buffer 0 (or 1) Ready Interrupt Request is generated and Data Buffer 0 (or 1) empties one packet space.

In a bulk transfer, when an IN endpoint successfully receives an ACK handshake from the Host, the data is toggled. But if the endpoint does not receive an ACK from the Host, the same data from the same toggle is sent in response to the next IN token.

When the data is to be sent in the following order, DATA0 is sent to Data Buffer0 and DATA1 is sent to Data Buffer 1 alternately. DATA0 → DATA1 → DATA0…

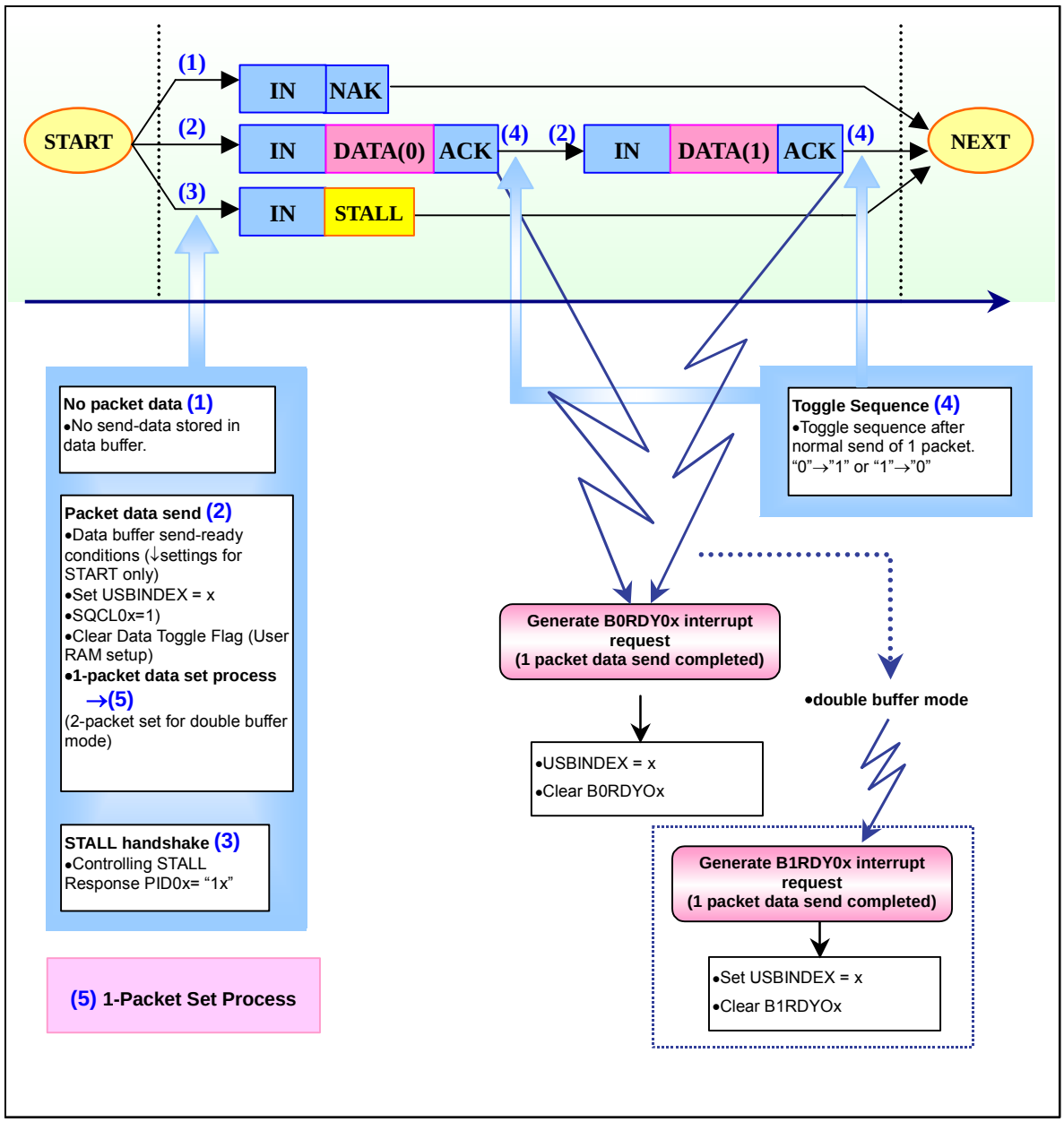


Figure 3.28 Example of Endpointx Bulk Data Send

• Example of S/W Process in Double Buffer Mode

As shown in Figure 3.29, when using the double buffer mode, if an interrupt request is generated for the first packet but the interrupt is not processed (the buffer is not written to) due to current execution of another process, both interrupt requests, B0RDY0x and B1RDY0x, are generated when an interrupt request is generated for the second packet.
At this time, when processing both interrupt requests, because data is sent to data buffers alternately (either DATA0 → DATA1 or DATA1 → DATA0), the user must manage the DATA0/DATA1 toggle sequence with software in order to handle data written to the two buffers. Refer to the example of software processing in Figure 3.29.

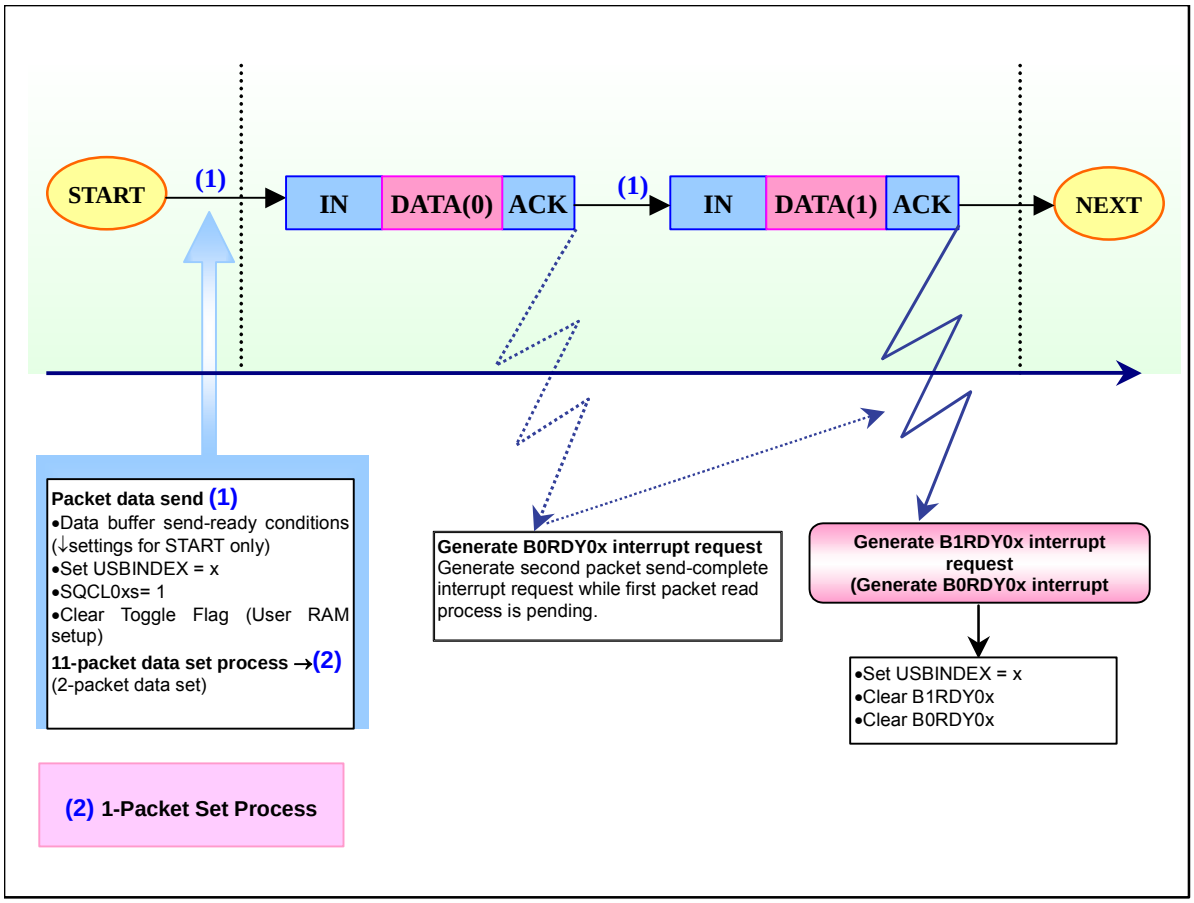


Figure 3.29 Example of Endpointx Bulk Data Send (double buffer mode)

3.3.10.Interrupt Transfer Data Send

(1) Transfer Type Setup

To use Endpointx IN for interrupt transfers, set the endpoint to interrupt transfer with EP0xCFG (EP0x Setup Register). Refer to the procedure in [Figure 3.26 Example of Endpointx Send Setup Procedure] for details.

(2) Data Send Prep

Preparation for interrupt transfers is the same as that of bulk transfers. Refer to [Chapter 3.3.9 Bulk Transfer Data Send] for details.

(3) Data Send Operation

The Endpointx IN operation for interrupt transfers is the same as that of bulk transfers. Refer to [Chapter 3.3.9 Bulk Transfer Data Send] for details.

3.3.11. Isochronous Transfer Data Send

(1) Transfer Type Setup

To use Endpointx IN for isochronous transfers, set the endpoint to isochronous transfer with EP0xCFG (EP0x Setup Register). Refer to the procedure in [Figure 3.26 Example of Endpointx Send Setup Procedure] for details.

(2) Data Send Prep

Set SQCL0x (Sequence Toggle Bit Clear Bit) to “1”. By setting this bit to “1”, the toggle bit is cleared and the next data PID is initialized to DATA0.

(3) Data Send Operation

An example of Endpointx isochronous data send is shown in Figure 3.30.
The isochronous transaction (IN) is repeated until all data is sent to the Host. The isochronous transaction does not include a handshake phase. The data packet is toggled and sent as DATA0 and DATA1.

Note: 38K0 Group MCUs toggle DATA0 and DATA1 in normal transfers.
(Refer to USB Specification Ver. 2.0 [Chapter 8.5.4 Isochronous Transactions].

If an IN token is received from the Host when there is no data in Data Buffer 0/1, the ERR0x interrupt (as an underrun error) is generated. When preparing the packet data, by not setting the data (in other words, set EP0xBYT0/EP0xBYT1 Register to “0”), the ERR0x interrupt will not be generated and an empty data packet (NULL data) can be sent.

Detailed explanations of single buffer and double buffer mode operations are provided below.

[1] Single Buffer Mode

In order to send data in the single buffer mode, the packet data must be set in Data Buffer 0. Confirm that Endpointx is not in the HALT state and that Data Buffer 0 is empty (B0VAL0x bit is “0”; write-enabled). Set the send packet data, then set B0VAL0x bit to “1”. (B0VAL0x bit is automatically cleared by H/W in normal receive transmissions.)

The number of bytes of packet data to be sent must be set in EP0xBYT0 (EP0x Byte Number Register).

After the data is set, Endpointx IN sends the data to the Host upon receiving an IN token. When one packet of data is sent successfully, the Endpointx Buffer 0 Ready interrupt is generated.

[2] Double Buffer Mode

In order to send data in the double buffer mode, if the packet is an even-numbered packet (starting with packet number 0), confirm that Endpointx is not in the HALT state and that Data Buffer 0 is empty (B0VAL0x bit is “0”; write-enabled). Set the send packet data and set B0VAL0x bit to “1”. (B0VAL0x bit is automatically cleared by hardware in normal send transmissions.)

Set the number of bytes of packet data to be sent in EP0xBYT0) (EP0x Byte Number Register 0).

In the same manner, when the packet is odd-numbered, confirm that Endpointx is not in the HALT state and that Data Buffer 1 is empty (B1VAL0x bit is “0”; write-enabled). Set the send packet data and set B1VAL0x bit to “1”. (B1VAL0x bit is automatically cleared by hardware in normal send operations.)

Set the number of bytes of packet data to be sent in EP0xBYT1 (EP0x Byte Number Register 1).

After the data is set, Endpointx sends the data to the Host upon receiving an IN token. When one packet of either DATA0 or DATA1 is sent successfully, Data Buffer 0 or 1 Ready Interrupt Request is generated accordingly.

• Example of S/W Process in Double Buffer Mode

As shown in Figure 3.29, when using the double buffer mode, if an interrupt request is generated for the first packet but the interrupt is not processed (the buffer is not read) due to the current execution of another process, both interrupt requests, B0RDY0x and B1RDY0x, are generated when an interrupt request is generated for the second packet.

At this time, when processing both interrupt requests, the user needs to toggle DATA0 and DATA1 with software accordingly (DATA0→DATA1 or DATA1→DATA0) so that the data buffers will be written to in the appropriate order. See Figure 3.29 for an example of the software processing.

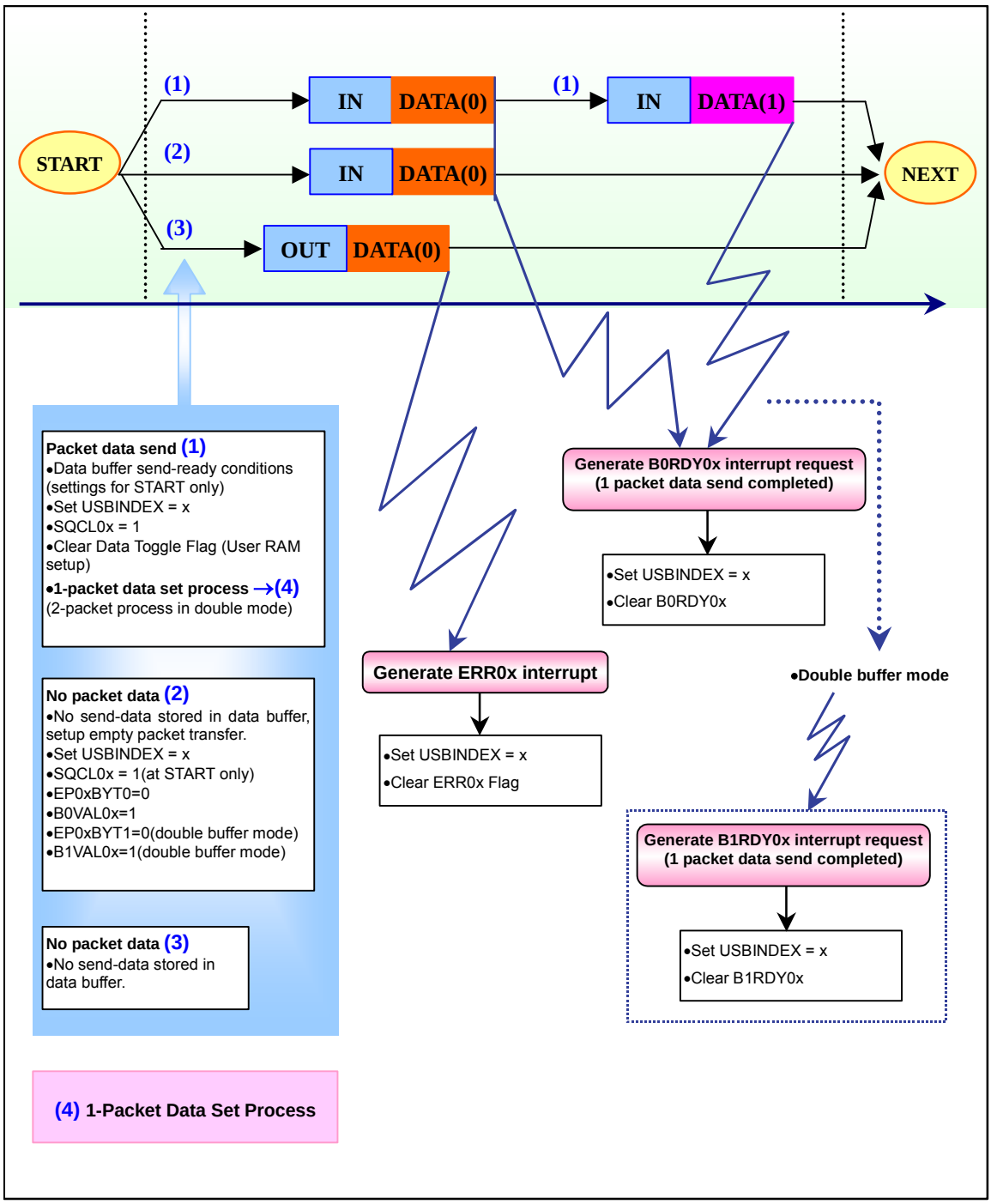
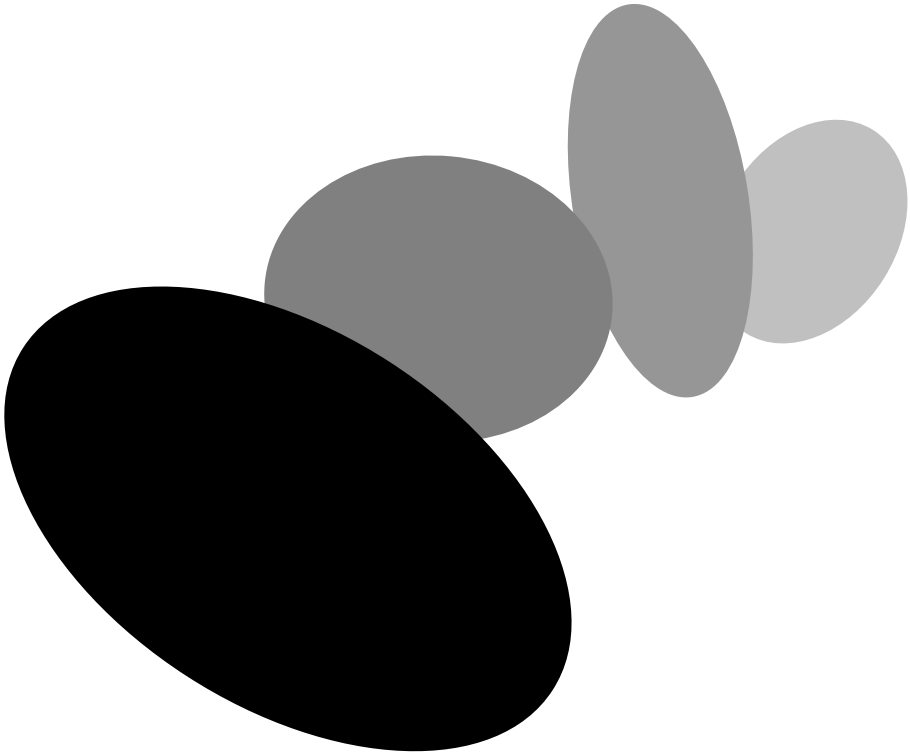


Figure 3.30 Example of Endpointx Isochronous Data Send



Chapter 4
Power Management

This chapter explains external power circuit difference to power supply methods, the USB Vbus detection method and a USB external circuit.

4.1.Power Supply

38K0 group provides the operating voltage (Vcc) 3.00-5.25V (The chip number with “L”).
38K0 group operating voltage (Vcc) differs to the system clock and internal clock (Ø). The correspondence is shown in Table4.1.

Table 4.1 Clock and Power voltage Vcc correspondence

f(Xin)	System Clock	Internal Clock Ø	Power Voltage V_{CC}
6MHz or 12MHz	12MHz	6MHz(2 division)	4.00~5.25
	8MHz	8MHz	4.00~5.25
	6MHz	6MHz	4.00~5.25
			3.00~4.00

The device power supply methods are the following three.

- ♦Self-power Method:
  Chip Vcc is supplied by a DC connector or battery.
- ♦Bus-power Method:
  Chip Vcc is supplied by the host PC through the USB Vbus line.
- ♦Selectable Self/Bus-power Method:
  The Self-power and Bus-power methods are selectable.

4.2.External Power Circuit

The external power circuit should be selected according to the power supply method. Bus-power and selectable Self/Bus-power methods require regulation to the operating voltage, if it is 3.3V, from the host PC power supply so that a regulator should be inserted to drop the USB Vbus voltage (the Bus power voltage supplied by USB up-port) to 3.3V. The selectable self/bus-power method requires a USB Vbus detection circuit and software procedure for the system to detect USB cable attachment or detachment.

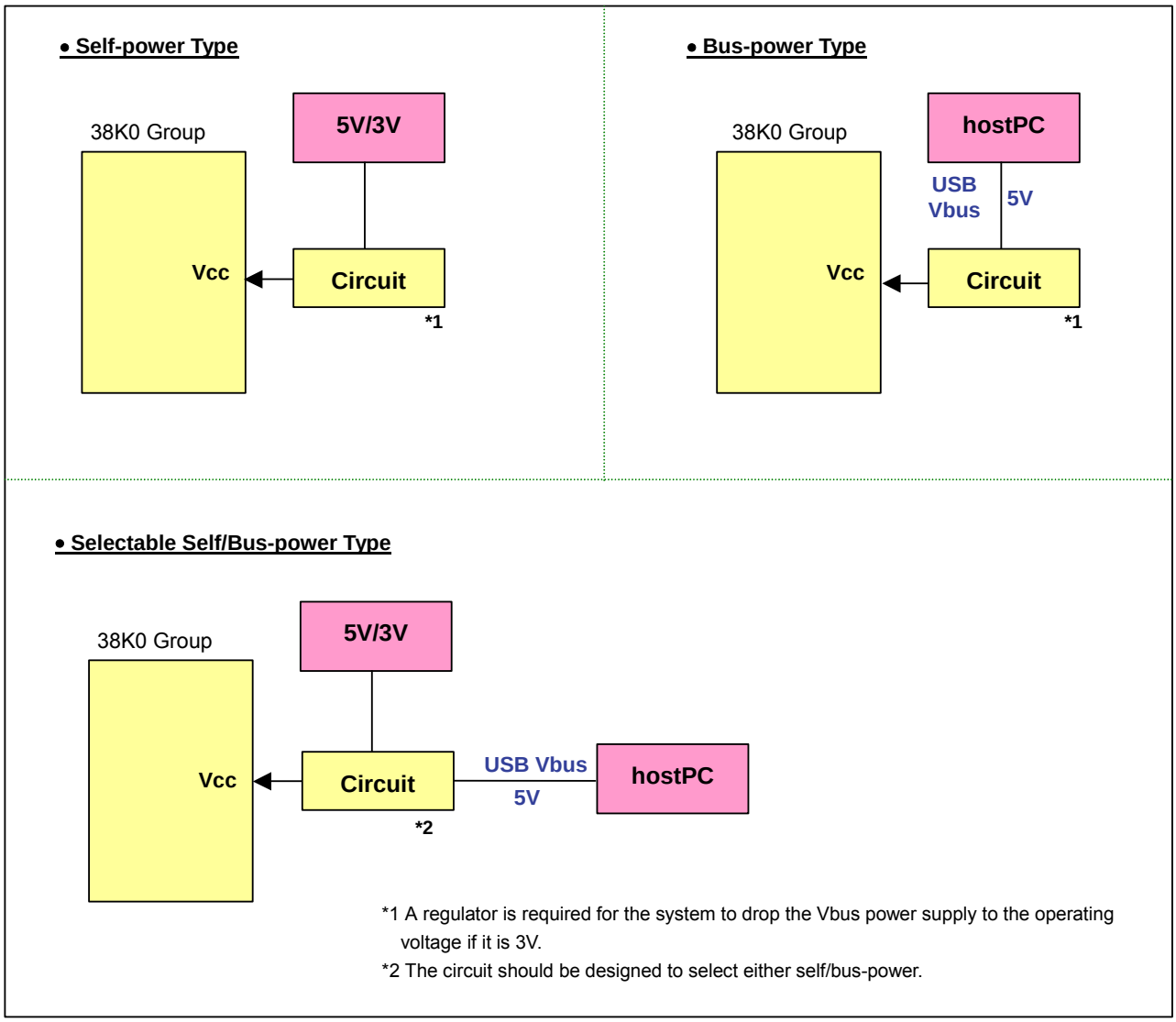


Figure 4.1 Vcc pin external circuit diagram

4.3.USB External Circuit (5V/3V-operation difference)

The USB external circuit and USB control register (USBCON) setting differ according to the operating voltages and power supply types.
38K0 group operating voltage (Vcc) differs to the system clock and internal clock (Ø). The correspondence is shown in Table4.2. The USB reference voltage circuit should be disabled for the USBVref pin to supply 3.00~3.60V when Vcc=3.00~4.00V and the USBVref voltage should not exceed Vcc.

Table 4.2 Clock, Power voltage Vcc and USB reference voltage USBVref correspondence

f(Xin)	System Clock	Internal Clock Ø	Power Voltage V_{CC}	USB reference voltage $USBV_{REF}$
6MHz or 12MHz	12MHz	6MHz(2division)	4.00~5.25	USB reference voltage circuit enabled
	8MHz	8MHz	4.00~5.25	
	6MHz	6MHz	4.00~5.25	
			3.00~4.00	USBreference voltage circuit disabled 3.00~3.60V directly to $USBV_{REF}$

(1) At 4.00~5.25V operation
USB reference voltage circuit may be enabled.
♦At USB block initialization
USB reference voltage enable bit (VREFE) = “1” : USB reference voltage circuit enabled.
USB reference voltage control bit (VRECON) = “0” : Normal mode.
♦In USB suspend interrupt procedure routin
USB reference voltage enable bit (VREFE) = “1” : USB reference voltage circuit enabled.
USB reference voltage control bit (VRECON) = “1” : Low power consumption mode.
♦At resuming interrupt procedure from suspend (USB Resume interrupt/Remote Wake-up)
USB reference voltage enable bit (VREFE) = “1” : USB reference voltage circuit enabled.
USB reference voltage control bit (VRECON) = “0” : Normal mode.

(2) At 3.00~4.00V operation
USB reference voltage circuit must be disabled.
♦At USB block initialization
USB reference voltage enable bit (VREFE) = “0” : USB reference voltage circuit disabled.
USBVref should be connected to Vcc if Vcc=3.00~3.60V.

Figure. 4.2 and Figure. 4.3 show USB external circuit connections.

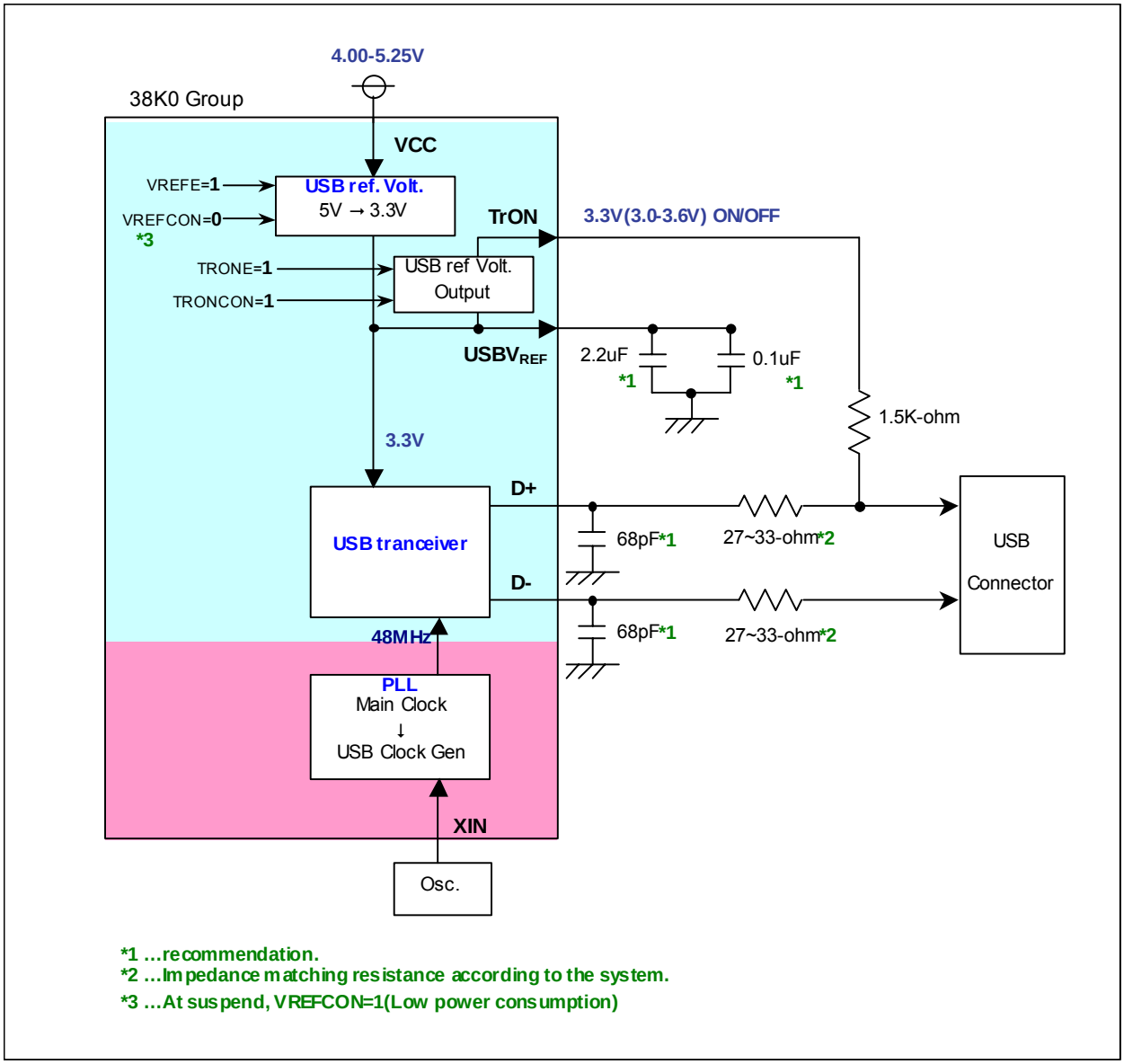


Figure 4.2 Example of USB External Circuit (USB reference voltage circuit enable)

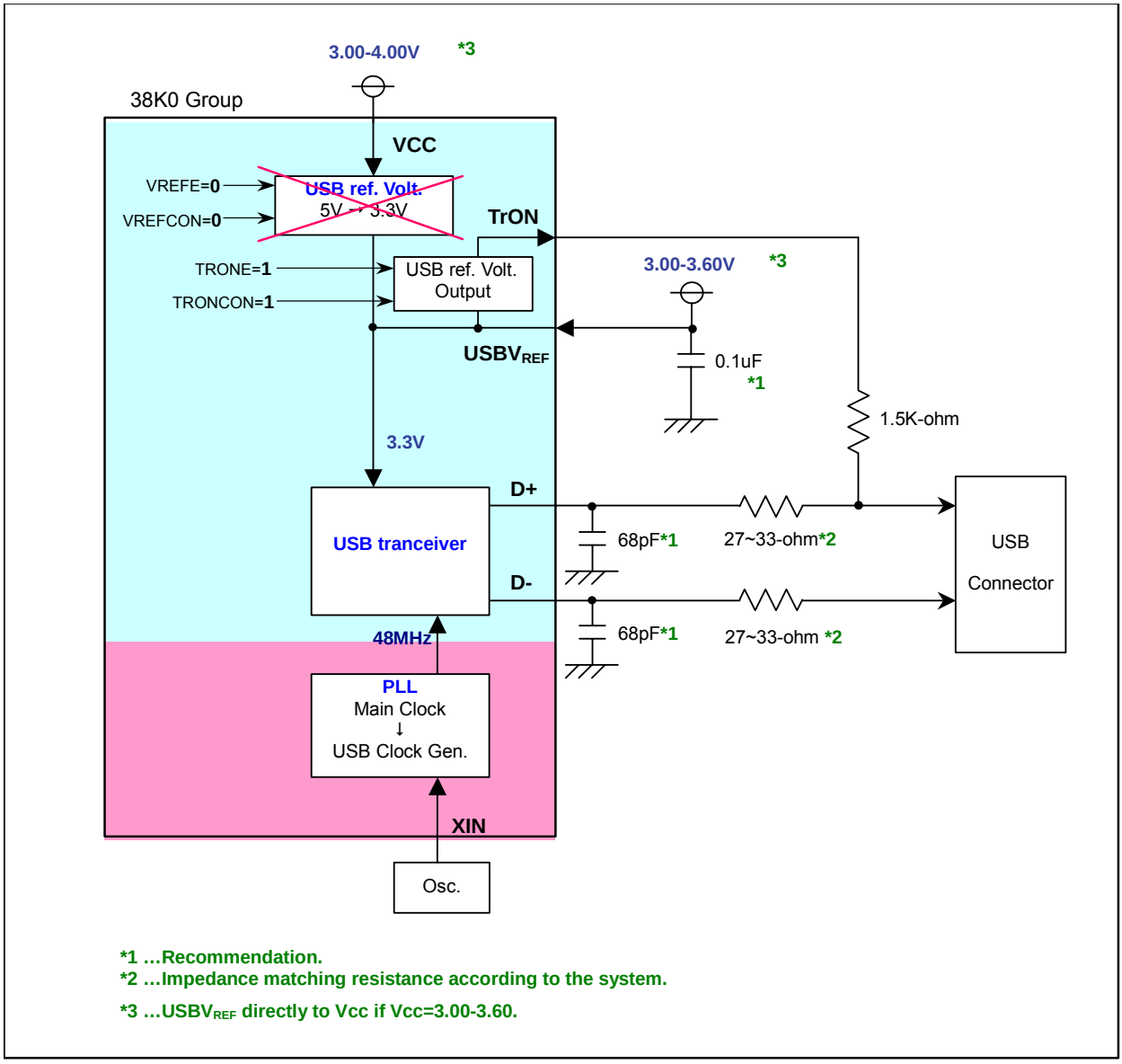


Figure 4.3. 2 Example of USB External Circuit (USB reference voltage circuit disable)

4.4.USB Cable Attachment/Detachment

4.4.1. Cases USB Vbus detection needed

(1) USB reference voltage output (TrON) ON/OFF Control

USB reference voltage output (TrON) is a up-port pull-up voltage output pin. The pin outputs $USBV_{REF}$ voltage which is supplied internally/externally. It is connected to D0+ line with a 1.5k-ohm resistor in series.

The TrON voltage output may be turned ON/OFF by TrOn output control bit (TRONCON), bit 1 of USB Control register (USBCON). TrON is normally turned ON after USB Vbus voltage detection.

(2) Self-power USB Vbus line detection

When microcomputers are in self-power operation, USB Vbus cannot be sustained after the up-port is detached from the host PC. TrON voltage output should be turned OFF and the USB Function should be halted while the situation USB Vbus is not sustained. The USB block may be enabled after the following USB Vbus detection.

38K0 group provides no H/W USB Vbus detection. It requires H/W USB Vbus detection circuits or F/W control with USB Vbus assigned to an interrupt.

4.4.2.USB Vbus Detection Method

This section explains the general method of connecting USB Vbus to the INT interrupt. USB Vbus may be detected by a comparator with monitoring the line.

Figure 4.4 show USB Vbus detection method example by external interrupt.

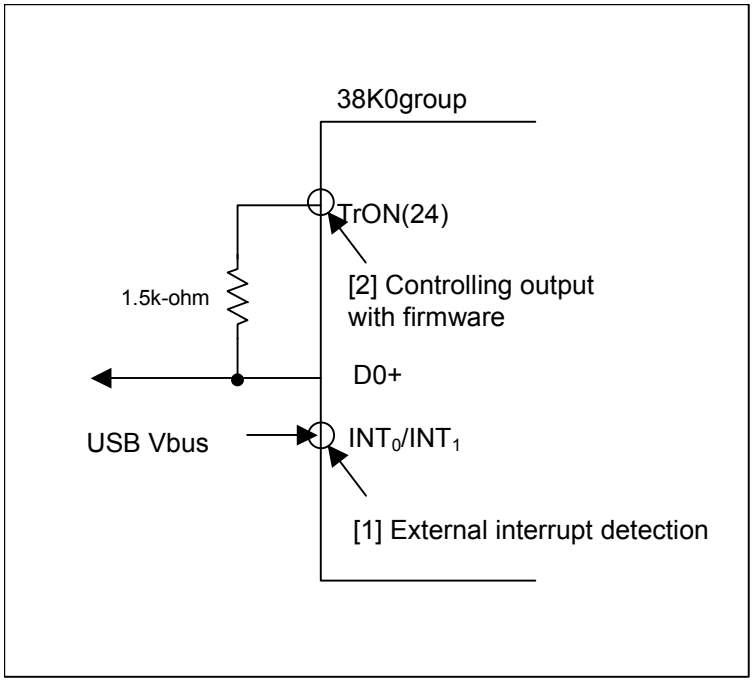


figure 4.4 Example of USB Vbus detection by external interrupt

(1) INT interrupt settings

USB Vbus and INT interrupt should be connected as shown in Figure 4.4. The INT_0 interrupt or INT_1 interrupt (functioning USB Vbus detector) detects USB cable attachment if the edge is “L” to “H” and USB cable detachment if the edge is “H” to “L”. The detection edge may be programmed by INT_0 /INT_1 Interrupt Edge Select Bit of Interrupt Edge Select Register (Address $0FF3_{16}$). Interrupt Request Bit should be cleared before enabling the interrupts.

(2) USB Vbus Detection

USB Vbus Detection must be performed for a few times with 2~3 ms intervals to be consistent.

♦USB Cable Attachment:

USB Vbus power supply should be enabled. The disabled USB block should be enabled and initialized for enumeration.

♦USB Cable Detachment:

The USB block and USB clock supply (PLL) should be disabled.

(3) USB Vbus Detection at USB Suspend

INT interrupt occurs while 38K0 group internal clock supply is stopped. At USB suspend when internal clock supply is stopped, USB Vbus input may be detected after the resume from USB suspend and internal clock supply restart.

INT interrupt settings should be inserted in the USB suspend interrupt routine at the resume from USB suspend (Clear Interrupt Request Bit and Set Interrupt Control Bit).

Revision History	38K0 Group Application Notes

Ver.No.	Date	Contents
1.0	Apr./23/02	First edition issued
1.1	Dec./18/02	*Chapter1 1.1 Introduction is deleted. *USB function control unit → USB device control unit *USB block → USB device block *1.3.1 How to Enable the USB Device Block is revised. *Detail descriptions for figure1.1 is revised. *Notes for 3V operation difference from 5V are added. P6,P8,P15,P23 *Detail descriptions for figure 2.2 are revised *The USB suspend/resume main procedure example is revised. P23,P27 *Notes for SIE figure is added. 3.4,3.13,3.16 *figure 3.18 is revised. *Chapter 4 Power Management is added. *Correction of errors
1.2	Jan./29/03	*Chapter 4 Power Management is revised. *Correction of errors
1.3	Oct./04/06	* Notes on USB Communication is added. * Table 4.1 and Table 4.2 are revised. *Correction of errors

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38K0 Group
USB Application Notes VER.1.3
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