SEQUENTIAL FLOW-CONTROL DEVICE PCB LAYOUT CONSIDERATIONS

APPLICATION NOTE AN-423

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INTRODUCTION

The sequential flow-control device is a revolutionary new product, offering exceptional performance and flexible storage capacity to match any application requirements. The device deploys a patent pending interleaved data path architecture supporting simultaneous multi-port accesses to provide throughput rates of 6.4Gbps*. The flexible storage capability, is provided through external DDR SDRAMs that can be seamlessly connected to the memory interface of the sequential flow-control device. In order to achieve optimum performance between the DDR SDRAM and the sequential flow-control device, customary PCB layout and trace routing of the memory interface signals should be applied. This application note will highlight some design and layout considerations.

*using IDT72T6480L7-5

SFC SEAMLESS INTERFACE TO DDR SDRAM MEMORY

The memory interface highlights of the Sequential Flow-Control device include:

- Supports up to 1Gb of DDR SDRAM memory
- Supports memory device densities of 128Mb and 256Mb
- 16 to 64-bit data interface (1 to 4 DDR SDRAM devices)
- Seamless external memory interface, including automatic refresh generation, differential clock generation.

DESIGN CONSIDERATIONS

Among the design considerations during the Computer Aided Design (CAD)/ Electronic Design Automation (EDA) phase are;

1. Component placement
2. Signal termination
3. PCB signal trace routing
4. Decoupling capacitance

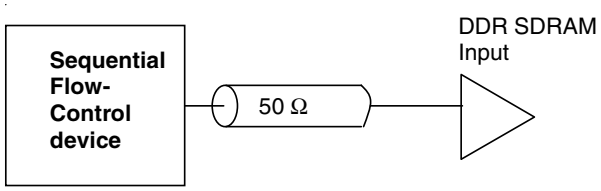
Reasonable analysis regarding the device orientation and trace routing should be conducted prior to commencement of the PCB layout phase.

COMPONENT PLACEMENT

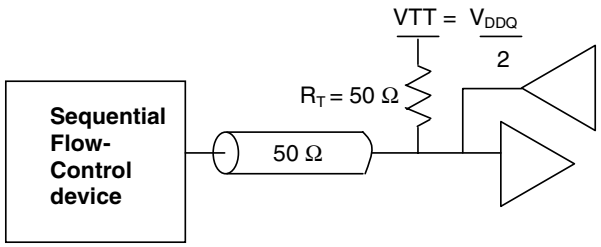
Contained within the IDT design phase aspects are the physical placement and orientation of the sequential flow-control (SFC) device when placed on a printed circuit board. The location of I/O signals on the SFC device have been taken into account to facilitate the connection to the upstream, downstream and the DDR SDRAM devices. In addition, the SFC device input/output signal pin assignments have been determined to enable a straightforward PCB trace routing connection to multiple DDR SDRAMs with minimal effort.

SIGNAL TERMINATION

The SFC device is designed to meet the SSTL_2 specifications of DDR SDRAMs. In general, in a controlled impedance environment signal termination is not required when the output source impedance is matched to the PCB trace impedance. In general, signal termination is not required as long as the interconnections are kept to a minimum. The minimum can be defined as the shortest path limited only by the package and leads of the DDR SDRAM and the sequential flow-control device. With all termination methods, for maximum effectiveness signal stubs should be avoided.



Unterminated Connection



Single Ended Parallel Termination

There are other termination schemes that can be used depending on the application and trace length. Please refer section 4 of the JEDEC JESD8-9B document on SSTL_2 for more information.

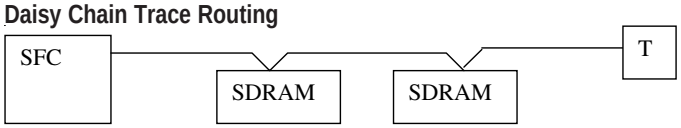
PCB SIGNAL TRACE ROUTING

Here are some guidelines and recommendations to providing trace routing of the memory interface signals. These guidelines will ensure the memory interface can operate at the maximum supported frequency.

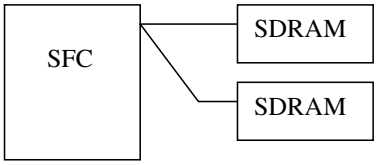
PCB TRACE GENERAL GUIDELINES

- To maximize signal integrity, the use of controlled impedance traces of Z_0 = 50 ohms (±10%) characteristic impedance should be considered.
- Consider routing high frequency signals on layers adjacent to a common reference plane (i.e. power or ground).
- Route each data group (DQS and DQ) on the same layer to match propagation delays and minimize skew.
- Route similar signals (i.e. address bus or data bus) on the same layer to match propagation delays and minimize signal –signal skew.
- Separate low frequency and high frequency signals to minimize crosstalk.
- Traces should be routed in a daisy chain manner versus a star topology to maintain signal integrity and facilitate a termination connection (if required).

Daisy Chain Trace Routing



Star Trace Routing



- Maximized trace spacing to other signals
- Differential clock signals should be routed as a differential pair, the traces should maintain the same length and routing path.
- When connecting multiple DDR SDRAMs, match the trace length and load for CK and $\overline{CK}$. This is necessary to ensure the data setup and hold times to all the DDR SDRAM are met.

ADDRESS AND DATA BUS, DATA STROBE, AND CONTROL SIGNAL GUIDELINES

- Maximize trace spacing to other signal groups:
- Signals should be routed in a daisy chain topology and preferably on the same layer with no vias.
- When connecting two or more memories, make the DDR address and control signals about the same length as the DDR clock traces. This will ensure the data setup and hold times are met.
- To minimize potential timing issues induced by trace routing. The DQ[63:0] and associated DQS[7:0] should have equal trace lengths. The data bus and data strobe should be matched in groups, as shown below:

DQS0 => DQ[7:0]
DQS1 => DQ[15:8]
DQS2 => DQ[23:16]
DQS3 => DQ[31:24]
DQS4 => DQ[39:32]
DQS5 => DQ[47:40]
DQS6 => DQ[55:48]
DQS7 => DQ[63:56]

- Use IBIS models and simulation tools to ensure the setup and hold times are met at maximum operating frequency of the DDR SDRAM.

TERMINATION AND REFERENCE VOLTAGE GENERATION (V_{REF} and V_{TT})

The SSTL_2 I/O standard for DDR SDRAM uses a reference voltage to maintain the DDR signals near their switching levels to increase switching speed. This reference voltage (V_{REF}) must meet several requirements in order for the DDR SDRAM to operate reliably at the maximum supported frequencies. The V_{REF} signal can be generated using a simple resistor divider with 1% or better accuracy, as shown in Figure 1.

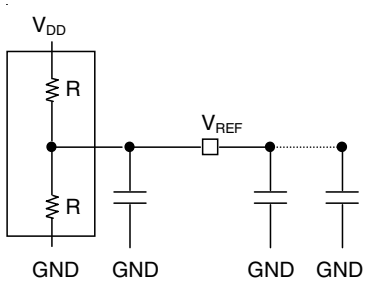


Figure 1. V_{REF} Signal Generation

The V_{REF} voltage signal should meet the following requirements to ensure maximum DDR SDRAM performance:

- Maintain maximum clearance from other nets
- Use a distributed decoupling scheme to minimize ESL and localize transient currents and returns.
- Simplify interface by routing on the top signal trace layer.

The termination voltage supply (V_{TT}) needs to track the DDR SDRAM supply voltage, V_{DDQ}, and it needs to source and sink the load current. Here are some guidelines for V_{TT} layout and implementation:

- Place termination resistors on a top layer V_{TT} (termination voltage supply) which is at the end of the bus.
- Place the V_{TT} generator as close as possible to the termination resistors.
- Its maximum voltage deviation should not exceed 40mV during extreme load transients, from the maximum rated sinking current to the maximum rated sourcing current.

Several solutions exist for generating V_{TT}, they consist of standard analog components (such as Motorola, National, Maxim, etc.), or switching regulator with discrete or integrated MOSFETs. A typical DDR termination regulator scheme using National Semiconductor LP2995 is shown in Figure 2.

DECOUPLING CAPACITANCE

The purpose of decoupling capacitors is to provide local "filtering" of the power/ground at the device within a system. Filtering of the power/ground is needed due to "noise" that is induced in the power/ground system by the transient switching current generated by digital devices. The power/ground decoupling network should be designed to accommodate the transient "noise".

SELECTING THE VALUE OF THE DECOUPLING CAPACITOR NETWORK

Since an individual decoupling capacitor is effective at a specific range of frequencies centered at its resonant frequency, it is important that the resonant frequency be taken into account when choosing a capacitor. To cover a broad range of frequencies, a mixture of capacitor values should be used.

For reference the capacitive reactance is defined by the following formula

$$X_c = \frac{1}{2 \pi fc}$$

Xc - capacitor reactance
π = pie (3.14)
F = frequency
C = Capacitor value

CONCLUSION

The guidelines in this application note are intended to alleviate issues on the printed circuit board, enhance time to market, and ensure optimal performance between the DDR SDRAM and the Sequential Flow-Control device. These guidelines, along with simulation and timing analysis, are recommended for maximum operability for the memory interface of the sequential flow-control device.

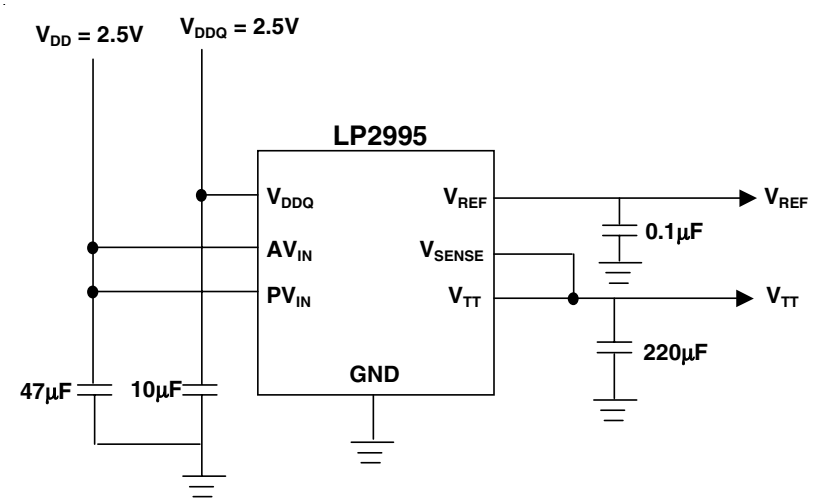


Figure 2. DDR Termination Regulator Scheme