Introduction

Both IDT's 82V2048 and Cortina's LXT384 are 8-channel short haul LIUs. According to the Cortina website, LXT384BE (160-pin BGA) is noted as End of Life (EOL) and LXT384LE (144-pin TQPF) is “Not Recommended for New Designs”. As a result, many existing applications may use 82V2048 to replace LXT384 in both new and existing customer designs. This application note first compares the two devices and then reveals some differences in applications. Overall, 82V2048 is a superset of LXT384 in features, register map and application flexibility. The IDT part is available in production in both BGA and TQFP packages.

Comparisons Between IDT82V2048 and LXT384

Overall Comparison

Table 1 provides an overall comparison between 82V2048 and LXT384 package, pin definitions, register map and some other features.

Table 1: Overall Comparison Between IDT82V2048 and LXT384

Items	IDT82V2048	LXT384
General functions	8-channel short-haul T1/E1 LIU	8-channel short-haul T1/E1 LIU
Pin/Package	TQFP-144 and PBGA-160 Pin-to-pin compatible with LXT384	TQFP-144 and PBGA-160
Voltage Supply	3.3V, line driver can be 3.3V or 5.0V	3.3V, line driver can be 3.3V or 5.0V
Register Map	Primary Registers: 22 (00h~15h) Expanded registers: 16 (00h~0Fh)	22 (00h~15h) None
Transmit Resistors	9.5Ω ±1% in E1 applications	11Ω ±1% in E1 applications
JA Corner Frequencies	Hardware mode (T1/E1): 1.7Hz/2.5Hz Host mode T1: 2.5Hz/5.0Hz, Host mode E1: 1.7Hz/6.5Hz	Hardware mode (T1/E1): 3.5Hz/6.0Hz Host mode T1: 3.0Hz/6.0Hz, Host mode E1: 2.5Hz/3.5Hz
Transmit All Ones when TCLK is logic “high”	MCLK is clocked and TCLK is logic "high". TCLK1 is internally used as MCLK when MCLK is not clocked	MCLK is clocked and TCLK is logic “high”

Hardware Interface Comparison

Both 82V2048 and LXT384 support hardware mode where pin-strapping is used to select different operations of each channel. Table 2 lists pins that are used for selecting functions. Please note some differences are only in the name of the pins, such as pin CODE (82V2048) and pin CODEN (LXT384). They are functionally the same pins.

Table 2: Comparison in Hardware Mode Configuration

Items	IDT82V2048	LXT384
Single Rail Mode Setting	Unipolar/Bipolar Selection: TDN pin = "0" - Dual rail TNN pin = "1" - Single rail	Unipolar/Bipolar Selection: TNEG pin = "0" - Dual rail TNEG pin = "1" - Single rail
Encode/Decoder Setting	Line coding selection: CODE pin = "0" - AMI CODE pin = "1" - B8ZS/HDB3	Line Coding Selection: CODEN pin = "0" - AMI CODEN pin = "1" - B8ZS/HDB3
Clock Recovery Enable/Disable	Pulling MCLK "high" to disable clock recovery function	Same as 82V2048
Power-down Setting for Receiver	Pulling MCLK "low" to set Receiver to power-down	Same as 82V2048
Power-down Setting for Transmitter	Pulling TCLK "low" to set Transmitter to power-down	Same as 82V2048
LP/LOOP Pins Setting in Hardware Mode	Loop-back Selection: LP pin = "0" - Remote Loop-back LP pin = "1" - Analog Loop-back LP pin = VDDIO/2 - No Loop-back	Loop-back Selection: LOOP pin = "0" - Remote Loop-back LOOP pin = "1" - Analog Loop-back LOOP pin = NC - NC Loop-back
JAS/JASEL Pin Setting in Hardware Mode	Jitter Attenuator Selection: JAS pin = "0" - JA in Transmit Path JAS pin = "1" - JA in Receive Path JAS pin = VDDIO/2 - JA disabled	Jitter Attenuator Selection: JASEL pin = "0" - JA in Transmit Path JASEL pin = "1" - JA in Receive Path JASEL pin = High-Z - JA disabled

Note: In 82V2048, when LP pins are not connected, they are internally pulled to VDDIO/2. Therefore they can be used in exactly the same way as LOOP pins in LXT384 for “No Loop-back” operation. Likewise, when JAS pins are not connected, they are internally pulled to VDDIO/2. They can be handled exactly the same way as JASEL pins in LXT384 for “JA disabled” selection.

Host Mode Comparison

Both 82V2048 and LXT384 include internal registers for host-interface mode. 82V2048 includes both a primary register map and an expanded register map while LXT384 includes only a primary register map. Please see Table 3 and Table 4 for primary and expanded register map, respectively.

Table 3: Comparison of Primary Register Map of 82V2048 and LXT384

Registers	IDT82V2048		LXT384	
	Offset address	**Default Value**	**Offset address**	**Default Value**
Device ID	00h	**10h***	00h	**00h or 15h***
Analog Loop-back Configuration	01h	00h	01h	00h
Remote Loop-back configuration	02h	00h	02h	00h
Transmit All Ones configuration	03h	00h	03h	00h
Loss of Signal Status	04h	00h	04h	00h
Driver Fault Status	05h	00h	05h	00h
Loss of Signal Interrupt Mask	06h	00h	06h	00h
Driver Fault Interrupt Mask	07h	00h	07h	00h
Loss of Signal Interrupt Status	08h	00h	08h	00h
Driver Fault Interrupt Status	09h	00h	09h	00h
Software Reset (per channel)	0Ah	FFh	0Ah	FFh
Performance Monitor Control	0Bh	00h	0Bh	00h
Digital Loop-back Configuration	0Ch	00h	0Ch	00h
LOS/AIS Criteria Selection	0Dh	00h	0Dh	00h
Automatic TAOS Configuration	0Eh	00h	0Eh	00h
Global Configuration	0Fh	00h	0Fh	00h
Pulse Shaping Indirect Address	10h	00h	10h	00h
Transmit Template Selection	11h	00h	11h	00h
Output Enable Configuration	12h	00h	12h	00h
Alarm Indication Signal Status	13h	00h	13h	00h
Alarm Indication Interrupt Mask	14h	00h	14h	00h
Alarm Indication Interrupt Status	15h	00h	15h	00h
Address Pointer Control Register	**1Fh***	**00h***	**N/A**	**N/A**

*** Note:** Bold text displays the differences between register maps of 82V2048 and LXT384.

When the Address Pointer Control Register = 0x00, the primary register map is employed in 82V2048. When the Address Pointer Control Register is written with 0xAA, the expanded register map is enabled as shown in Table 4. The LXT384 does not include these registers and uses pin-strapping as discussed in hardware mode to achieve such selections. In this respect, 82V2048 may be more flexible to configure and easier to use in host mode. In addition, the 82V2048 supports Inband loop-back in host mode. LXT384 does not support inband loop-back in either hardware mode or host mode.

Table 4: 82V2048 Expanded Registers

Register Names	IDT82V2048 (n = 0…7 represents each channel)	LXT384
Single Rail Mode Setting Register **SING[7:0]**	SING[n] = "0" - Use TDN pins to select single/dual rail mode SING[n] = "1" - Single rail mode	Not supported in host mode
Encoder/Decoder Selection **CODE[7:0]**	CODE[n] = "0" - B8ZS encoder/Decoder CODE[n] = "1" - AMI encoder/Decoder	Not supported in host mode
Clock Recovery Enable/Disable Selection **CRS[7:0]**	CRS[n] = "0" - Clock recovery enabled CRS[n] = "1" - Clock recovery disabled	Not supported in host mode
Receive Power-Down Control **RPDN[7:0]**	RPDN[n] = "0" - Receiver normal operation RPDN[n] = "1" - Receiver powered down	Not supported in host mode
Transmitter Power-down Control **TPDN[7:0]**	TPDN[n] = "0" - Transmitter normal operation TPDN[n] = "1" - Transmitter powered down	Not supported in host mode
EXZ Error Detection Control **CZER[7:0]**	CZER[n] = "0" - Excessive zero detection disabled CZER[n] = "1" - Excessive zero detection enabled for B8ZS/HDB3 in single rail mode	Not supported in host mode
Equalizer Enable/Disable Control **EQUA[7:0]**	EQUA[n] = "0" - Normal operation EQUA[n] = "1" - Receive equalizer is enabled	Not supported in host mode
In-band Loop-back Configuration **LBCF[7:0]**	Setting LBCF, LBAC, LBDC, LBS, LBM, LBI, LBGS and LBGE registers to enable inband loop-back functions.	Inband Loop-back not supported

Application Considerations When Using 82V2048 to Replace LXT384

In Table 1, it is seen that 82V2048 has the same pin-out in both package types (TQPF and BGA) as LXT384. Replacing LXT384 with 82V2048 requires no board changes. However, depending on different mode of device configuration (hardware mode or host mode), the following application considerations may be considered.

Host Mode

When host mode is selected, the two devices share a common primary register map. LXT384 defines 22 eight-bit registers with offset addresses from 00h to 15h.

82V2048, not counting Expanded Registers, contains the same number of registers with the same offset addresses and bit definitions of each register.

A thorough register access test was conducted in ATE (Automatic Test Equipment) with the test vector designed as follows:

1. After power-up, software reset was issued by writing to 0x0A register;
2. Read all registers and check for register default values;
3. Write all registers with 0xFF data;
4. Read back from all registers again and compare with what was written in (0xFF).
5. The access was made with Intel-multiplexed and non-multiplexed bus mode, Motorola multiplexed and non-multiplexed bus mode.

The test results show that, all registers have the same default values after reset between the two devices. All write-and-read operations were correct with both devices. Please note that reading Device ID register (offset 0x00) will have different values between two devices per each vendor's definition.

MCLK and TCLK

MCLK is the reference clock for the device. TCLK is the system transmit clock for each channel's transmit path. When MCLK is not clocked (in logic “high” or “low”), the receive path of the two devices will respond the same. However, in the transmit path, the two devices respond differently.

In 82V2048, if MCLK is not available, TCLK1 (transmit clock for the first channel) will be internally used as a virtual MCLK in the transmit path. As a result, same operations can be expected as long as TCLK1 is supplied. If neither MCLK nor TCLK1 is supplied, the device will put all TTIP and TRING pairs in high impedance. These operations are tabulated below.

Table 5: Impact of TCLK on IDT82V2048 Transmit Path

MCLK	TCLK1	TCLK0, TCLK2~7	82V2048 Transmit Path Operations
H/L	Clocked	Clocked	Transmit with pulse-shaping
		H/L	Transmit All Ones
H/L	H/L	Don’t care	All TIP/RRING pairs in high-impedance

In LXT384, when MCLK is not available, the status of TCLK has different impacts on the transmit path. The combinations of MCLK and TCLK availability result in the different operations in the transmit path tabulated below.

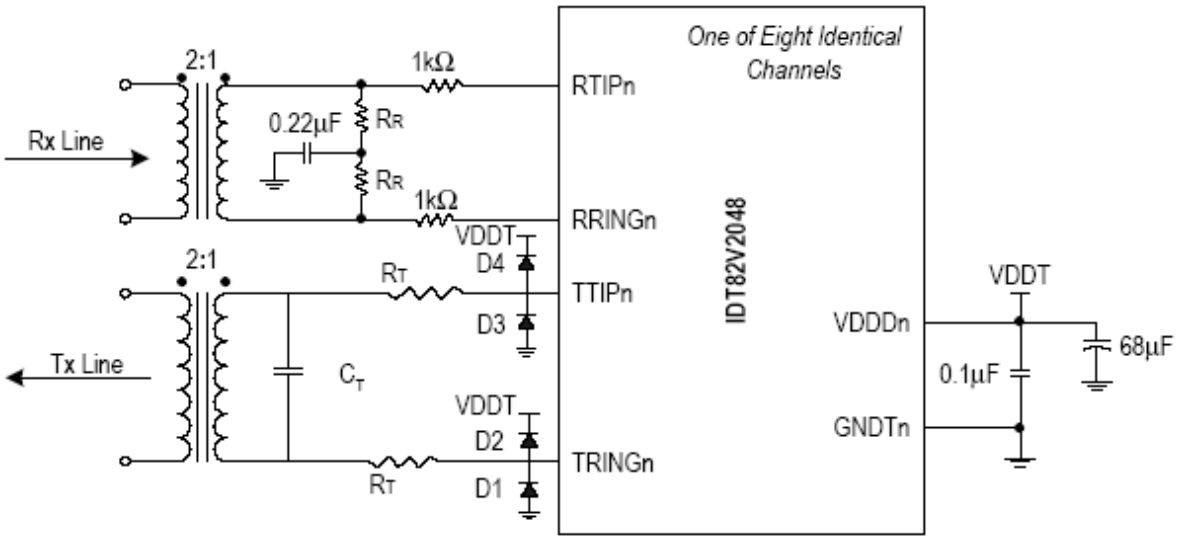
Table 6: Impact of TCLK on LXT384 Transmit Path

MCLK	TCLK0~7	LXT384 Transmit Path Operations
H/L	Clocked	Transmit with pulse-shaping
h H/L	H	Transmit without pulse shaping, TPOS and TNEG control the width and polarity of pulses on TTIP and TRING (clock-less transmission
	L	Transmit path in high-impedance

External Components

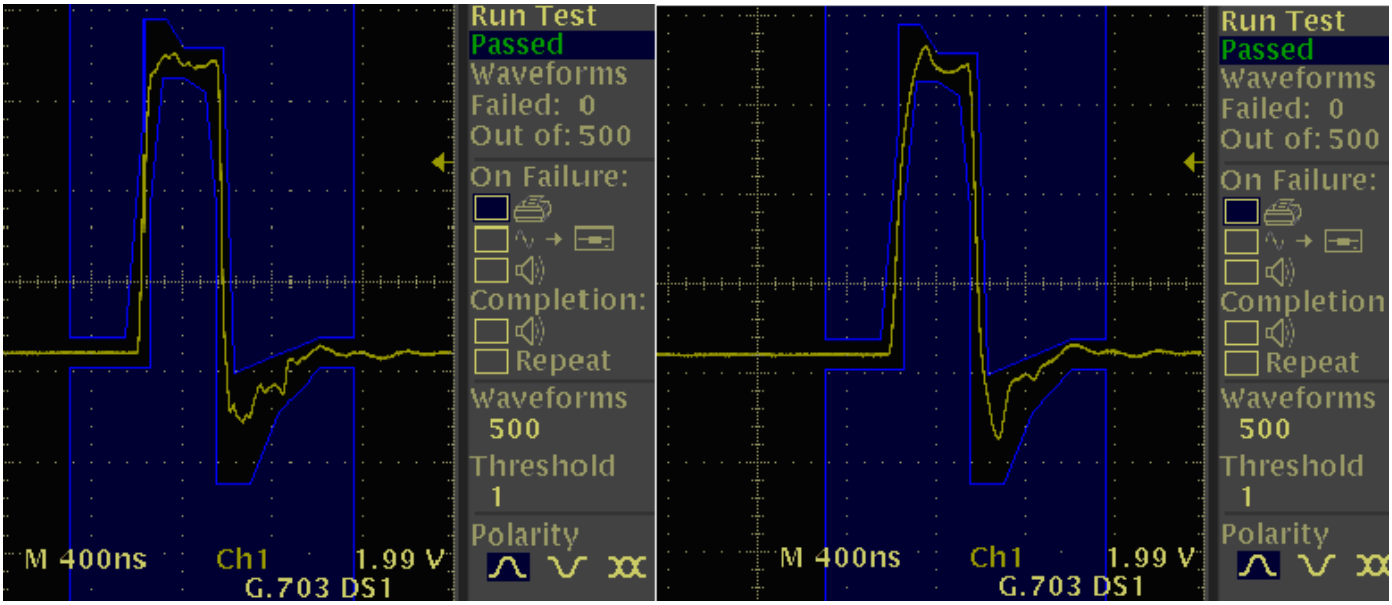
The following diagram shows a typical application diagram for 82V2048. Note that, based on the datasheet of both devices, R_T value is recommended to be 9.5Ω +/-1% for 82V2048, 9.1Ω +/-1% for LXT384 for VDDT = 5.0V. C_T is 1000pF for 82V2048 while 560pF for LXT384.

Figure 1. Line Interface with External Components for Impedance Matching



Transmit pulse shape has been verified with the recommended external components. For simple data pattern (i.e., 1-in-8) it can be observed that transmit pulse shape meets G.703 pulse template as shown below in Figure 2. The following picture shows transmit pulse shape in T1 mode 0ft and 655ft cable configurations, respectively.

Figure 2. Transmit Pulse Shape Of 82V2048 in T1 mode with external components recommended for LXT384. Data pattern:1-in-8 Cable length configurations: 0~133ft (left figure), 533~655ft (right figure)



Note that transmit pulse shape is dependent on the line's overall impedance conditions. In actual applications, the specific values of these external components may need some adjustments to achieve optimal pulse shape.

Appendix: Power Consumption Measurement

Table 7: Device Power Consumption Comparison

Device	Data Pattern	50% Ones		100% Ones	
	Mode	E1	T1	E1	T1
IDT82V2048	VDDA (mA)	25	24	24	24
	VDDD (mA)	33	26	38	29
	VDDT (mA)	55	197	107	344
	Total (mA)	**113**	**247**	**169**	**397**
Cortina LXT384	VDDA (mA)	53	45	52	44
	VDDD (mA)	60	46	61	46
	VDDT (mA)	67	173	136	321
	Total (mA)	**180**	**377**	**249**	**411**

References

[1] IDT82V2048 device datasheet, March 18, 2009

[2] LXT384 Datasheet 248994, Revision 6.0, January 30, 2008

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