Introduction

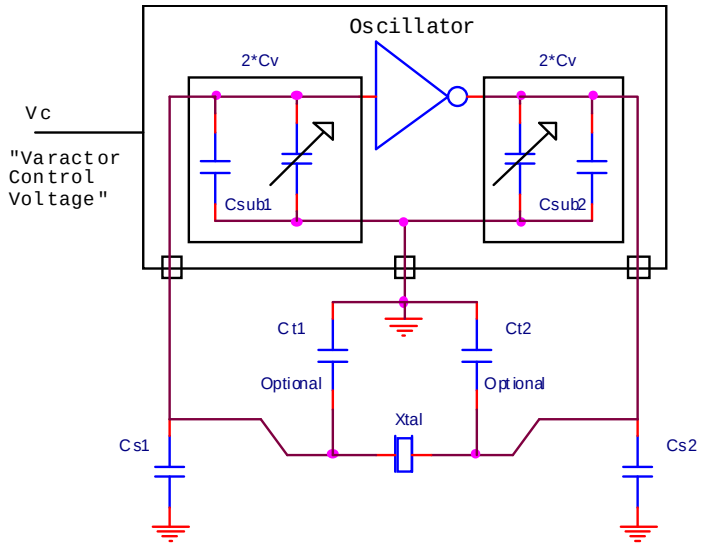
This application note provides some basic guidelines when selecting the proper crystal (XTAL) to work with IDT's family of Synchronization WAN-PLLs™ with low jitter, VCXO-based APLLs. A list of recommended XTAL vendors and parts numbers are provided, and have been categorized based on applicable industry standards.

VCXO Overview and Definitions

The VCXO consists of four basic components which can be identified in Figure 1 below.

- The crystal.
- The IC oscillator with internal voltage variable capacitors and internal wiring capacities.
- The stray wiring capacity between the IC oscillator and the crystal, including the pads for the IC, crystal and tuning capacitors.
- Optional discrete tuning capacitors to decrease the VCXO center frequency to match the specified crystal frequency

Figure 1. VCXO Oscillator Circuit



Where

Vc = Control voltage to change the VCXO frequency.

Csub = Internal VCXO parasitic wiring capacity to the IC substrate.

2*Cv = Varactor Capacity and Csub in parallel on oscillator input and output.

Ct = Tuning capacitors to center the VCXO center frequency.

Cs = Stray capacities of crystal and tuning capacitor pads and wiring.

The frequency of a parallel resonant fundamental mode crystal, such as used in IDT VCXOs, is specified by crystal frequency at a specified CL, which is the total loading capacity across the two terminals of the crystal. However the various capacitors associated with the wiring and the IC oscillators are all referenced to ground as seen in the figure below. Conversion of these grounded capacitors to equivalent capacitors across the terminals of the crystal is required to ensure that the sum of all the VCXO capacitors does not exceed the CL of the crystal.

The IC inverter forces the currents flowing in parallel combination of the grounded capacitors on the inverter input to be 180 degrees out of phase with the current flowing in the parallel combination of the grounded capacitors at the inverter output. Since the currents are the same, the input and output capacities are effectively in series. Using the varactor capacities as an example, the input and output capacities are 2*Cv. The series capacity is half that of each grounded capacitor, or Cv and appears equivalently across the crystal terminals. Similarly for the stray and tuning capacitors, Cs and Ct respectively.

Key Crystal Parameters

Frequency Tolerance

Frequency tolerance, also known as calibration accuracy, is the amount of frequency deviation from a specified center frequency at ambient temperature (referenced at 25°C). It is specified in units of parts-per-million (ppm).

Frequency Stability

Frequency stability is the amount of frequency deviation from the ambient temperature frequency over the operating temperature range. This deviation is associated with a set of operating conditions including: Operating Temperature Range, Load Capacitance, and Drive Level.

This parameter is specified with a maximum and minimum frequency deviation, expressed in percent (%) or parts per million (ppm). The frequency stability is determined by the following primary factors: Type of quartz cut and angle of the quartz cut. Some of the secondary factors include: mode of operation, drive level, load capacitance, and mechanical design.

Aging

Aging is the systematic change in frequency with time due to internal changes in the crystal which is related to the crystal contamination and drive level. Over time, particles drop off or fall onto the quartz surface, hence slightly changing the resonant frequency.

Aging is often expressed as a maximum value in parts per million per year [ppm/year]. The rate of aging is typically greatest during the first 30 to 60 days after which time the aging rate decreases. The following factors effect crystal aging: adsorption and desorption of contamination on the surfaces of the quartz, stress relief of the mounting and bonding structures, material outgassing, and seal integrity.

Hold-In

The hold-in, or frequency accuracy, is a measure of the worst-case offset, in parts-per-million (ppm), one can expect from the nominal frequency over a period of time. This specification is the sum of the maximum static system offset plus the dynamic tracking offset forced upon a PLL by output phase slope limiting system requirements when phase transients are present in the PLL input reference.

For GR-253 Core Issue 5, see Figure 5-18 on page 5-78. The worst case MTIE is required to be equal to (7.6+885*S)nS when S = 0.14 for an offset of 0.94 ppm. The dynamic offset is rounded up to 1ppm.

For G.813 Option 1 and G.8262 Option 1, see G.6262 Opt 1 Section 11.4.1, EEC-Option 1. The 7.5 ppm requirement is stated explicitly. This sum of the static and dynamic is rounded up to 13ppm.

Specifications	Maximum Clock Frequency Offset (ppm)	Phase Slope Limiting Offset (ppm)	PLL Tracking Offset (ppm)
1. GR-253-Core SONET Minimum Clock 2. SONET/SDH 3. G.813 Option 2	20	0.94	21
1. G.813 Option 1 2. G.8262 Option 1	4.6	7.5	13
1. GR1244-Core 2. GR-253-Core Stratum 3 3. G.812 Type IV 4. G.8262 Option 2	4.6	0.94	6

Pull

Crystals in an HC-49S (low profile) package generally don't have as much pulling range as would a crystal in an HC-49U (high profile) package; crystals in a ceramic package generally have even less. Pullability is usually a function of the size of the termination electrode connected to the crystal blank. A bigger crystal blank, of course, can accommodate a larger electrode. Due to its low profile, an HC-49S crystal has a smaller electrode than an HC-49U, thus a reduced pullability.

Cs Requirement

Of the three components of the VCXO shown in Figure 1 above, only the stray wiring capacity is not guaranteed by a component vendor. A maximum stray wiring capacity that appears in parallel with the crystal terminals is specified in Table 1 below. This is the series equivalent capacity of Cs1 and Cs2 as shown in Figure 1.

This maximum capacity will guarantee that the pull range of the VCXO will be symmetric about the nominal center frequency under the condition of the CL and Cv capacities specified in Table 1. It is the responsibility of the board designer to ensure that this maximum is not exceeded. It is preferable that the wiring capacity is less than the maximum, allowing tuning caps to be installed to make a fine adjustment of the VCXO center frequency.

Table 1: WAN-PLL VCXO-based APLL Capacitance Requirements

Symbol	Parameter	Typical (pF)	Max (pF)
Cs	Equivalent Parallel Stray capacity		1.9
CL	Crystal Parallel Load Capacity at the nominal center frequency	10	
C_{V_LOW}	Low Varactor Capacitance	5.4	
C_{V_HIGH}	High Varactor Capacitance	12.7	

CL = 10pF is set for the best match between the varactor capacities and stray capacitances achievable on a printed wiring board. The maximum stray capacitance requirement is determined by the crystal load curve. The interested reader is pointed to IDT AN-841 for the stray capacity limit and to AN-831 for the crystal load curve.

Determination of VCXO Margin Against the Application APR

The application's Absolute Pull Range requirement (APR), is the guaranteed pull range of the VCXO after all crystal tolerances have been accounted for. The accounting begins with the pull range of a properly tuned VCXO and subtracts all the known tolerances as well as the application APR. The remainder is the Margin against APR and must be greater than zero.

Example: Calculating a VCXO's APR Margin Budget

Table 2 shows an example of an HC49S crystal electrical specification. Most manufacturers have similar values and variables. For such a crystal and a VCXO with the capacities shown in Table 1 above, the pull range of the VCXO is ±120 ppm. Since all tolerances and APR are symmetric, it suffices to use only positive values.

Table 2: Example of an HC49S Crystal Electrical Specification

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation		Fundamental			
f_N	Frequency			25		MHz
f_T	Frequency Tolerance	@ 25°C			±20	ppm
f_S	Frequency Stability	-40°C to +85°C			±20	ppm
	Operating Temperature Range		-40		85	°C
C_L	Load Capacitance			10		pF
C_O	Shunt Capacitance			3.3		pF
C_1	Motional Capacitance			12.7		fF
ESR	Equivalent Series Resistance				40	Ω
	Drive Level			100	200	µW
	Aging @ 25°C				±5 over 1 year ±20 over 20 years	ppm

Using the crystal tolerances from the HC49S crystal above in Table 2, the margin against APR is calculated as shown in Table 3 and Table 4 below.

Table 3: HC49S Margin Against APR

	SynchE	SONET/SDH	Units
VCXO Pull Range	120	120	ppm
Crystal Tolerance	-20	-20	ppm
Crystal Stability	-20	-20	ppm
Aging (20 yrs)	-20	-20	ppm
APR	-13	-21	ppm
Margin	**47**	**39**	**ppm**

In the same manner, the margin against APR can be calculated for a 5032 crystal with the same capacities as Table 1, but with C0 = 2.2pF and C1 = 8.4fF. The pull range is ±95 ppm.

Table 4: 5032 Margin Against APR

	SynchE	SONET/SDH	Units
VCXO Pull Range	95	95	ppm
Crystal Tolerance	-20	-20	ppm
Crystal Stability	-20	-20	ppm
Aging (20 yrs)	-20	-20	ppm
APR	-13	-21	ppm
Margin	**22**	**14**	**ppm**

XTAL Layout Considerations

The objective is to avoid adding any noise to the clock between the crystal and XTALn_IN/OUT pins. Below are some guidelines when co-locating the crystal with the PLL.

1. Place tuning capacitors symmetrically across the crystal terminals. Connect the ground terminals together and tie with a single via to the IC ground. See Figure 1 for schematic representation.
2. Keep the crystal bond pads and trace width to the XTALn_IN/OUT pins as small as possible. Routing should be done on top layer with no vias.
3. Clocks and frequently switched signals should not be routed close to the crystals.
4. Digital signals should not be routed directly under the crystal or XTALn_IN/OUT pins.
5. All metal layers in the PCB are recommended to be removed under the XTALn_OUT ball, crystal pad and associated trace.
6. It is recommended to protect crystal traces with ground traces and guard rings.

For ceramic packages, provide an option for load tuning capacitors, in case fine tuning is needed or for centering the nominal frequency.

Example Crystal Layouts

Figure 2. HC49S Layout

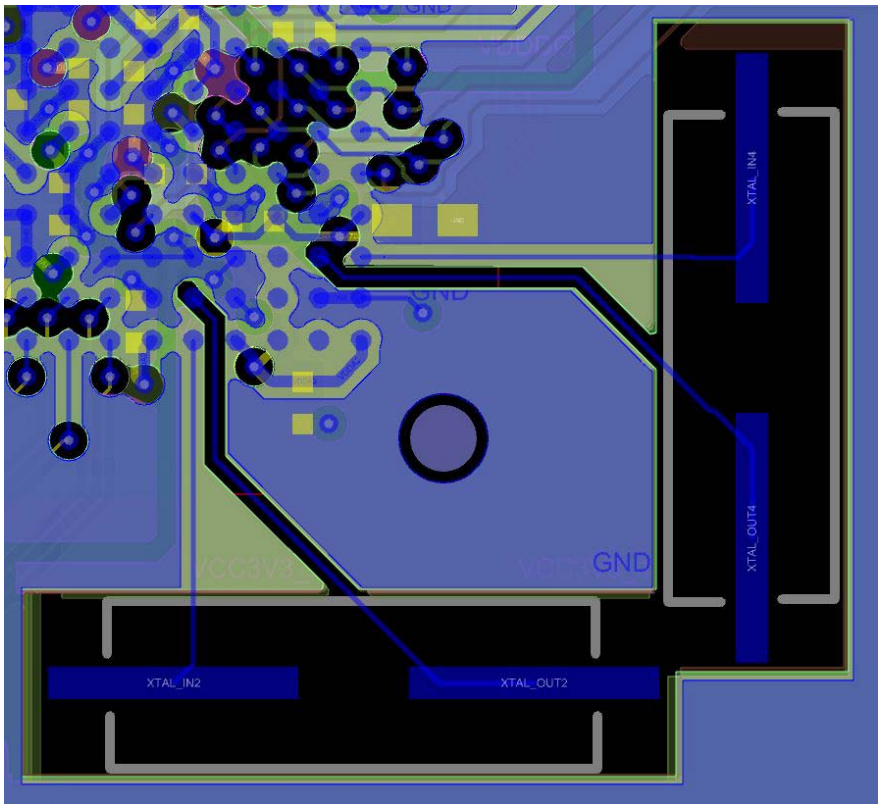
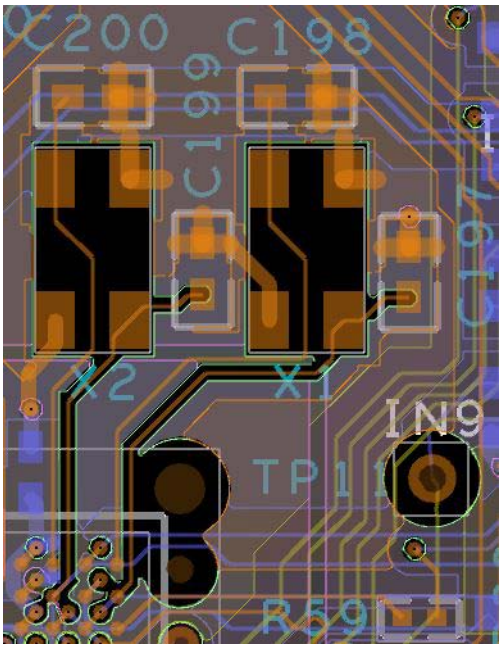


Figure 3. 5032 Layout (with load tuning caps)



Target Standards and Recommended Crystals

This following tables categorize recommended crystal vendors and parts numbers based on applicable industry standards. This is not meant to be an exhaustive list, but does highlight parts that have proven to be suitable with IDT's synchronization WAN-PLLs in meeting applicable industry standards.

GR-253-Core SONET Minimum Clock / G.813 Option 2 / SONET/SDH Line Card

Frequency Accuracy/Hold-In (20 years[1]): ±21ppm

XTAL Vendor	Part Order Number (XTAL Family)	Pkg	Temperature Range	Notes
24.8832 MHz (SONET)				
Fox (www.foxonline.com)	278LF-24.8832-3 (HC49SDLF)	HC-49S SMD	-40°C to +85°C	1
25 MHz (ETH)				
Fox (www.foxonline.com)	278LF-25-336 (HC49SDLF)	HC-49S SMD	-40°C to +85°C	1
25.78125 MHz (ETH LAN)				
Fox (www.foxonline.com)	278LF-25.78125-1 (HC49SDLF)	HC-49S SMD	-40°C to +85°C	1

1. Tested in the lab by IDT

G.813 Option 1 / G.8262 Option 1 / SyncE Line Card

Frequency Accuracy/Hold-In (1 year): ±13ppm

XTAL Vendor	Part Order Number (XTAL Family)	Pkg	Temperature Range	Notes
NOTE: All XTALs listed in previous table(s) are also suitable.				
24.8832 MHz (SONET)				
Fox (www.foxonline.com)	495-24.8832-2 (FX532B)	5032 SMD	-40°C to +85°C	
MtronPTI (www.mtronpti.com)	M1325S141 (M1325)	5032 SMD	-40°C to +85°C	1
Rakon (www.rakon.com)	513810 (IFF10RSX-5)	5032 SMD	-40°C to +85°C	
25 MHz (ETH)				
Fox (www.foxonline.com)	495-25-141 (FX532B)	5032 SMD	-40°C to +85°C	
MtronPTI (www.mtronpti.com)	M1325S139 (M1325)	5032 SMD	-40°C to +85°C	
Rakon (www.rakon.com)	512839 (IFF10RSX-5)	5032 SMD	-40°C to +85°C	1
25.78125 MHz (ETH LAN)				
Fox (www.foxonline.com)	495-25.78125-2 (FX532B)	5032 SMD	-40°C to +85°C	
MtronPTI (www.mtronpti.com)	M1325S142 (M1325)	5032 SMD	-40°C to +85°C	1
Rakon (www.rakon.com)	513805 (IFF10RSX-5)	5032 SMD	-40°C to +85°C	
24.576 MHz (CPRI)				
Rakon (www.rakon.com)	513809 (IFF10RSX-5)	5032 SMD	-40°C to +85°C	

1. Tested in the lab by IDT

GR1244-Core / GR-253-Core Stratum 3 / G.812 Type IV / G.8262 Option 2

Frequency Accuracy/Hold-In (20 years[2]): ±6ppm

XTAL Vendor	Part Order Number (XTAL Family)	Pkg	Temperature Range	Notes
NOTE: All XTALs listed in previous table(s) are also suitable.				

2. Per Telcordia GR-1244-CORE; ITU-T specifies 1 year

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