

## Introduction

Renesas’ Low-Power (LP) HCSL drivers (often referred to as push-pull HCSL, or PCIe drivers) can easily drive a variety of other logic types, in addition to HCSL. A simple, passive network can adjust the swing and common mode voltage to required levels. The LP-HCSL driver can be viewed as a low-power 0–800mV square wave generator terminated to  $50\Omega$  output impedance. It can be used to drive any other logic that requires a swing of 800mVpp or less. With the driver source-terminated to  $50\Omega$ , receiver input terminations are not necessary; yet it is okay if the receiver is also terminated.

Note that we will adopt the convention of referring to the output impedance in a single-ended manner in this application note. A  $100\Omega$  differential impedance transmission line can be treated as two single-ended transmission lines of  $50\Omega$  for termination purposes.

Generic differential inputs can handle a wider range of differential swing and common mode voltages than standard logic families and are becoming more popular. This application note describes how to use LP-HCSL outputs to drive various standard logic types and the newer generic differential inputs. For additional information on LP-HCSL outputs, see Renesas application note ["AN-879 Low-Power HCSL vs. Traditional HCSL"](#).

## Network Overview

Figure 1. Universal Network

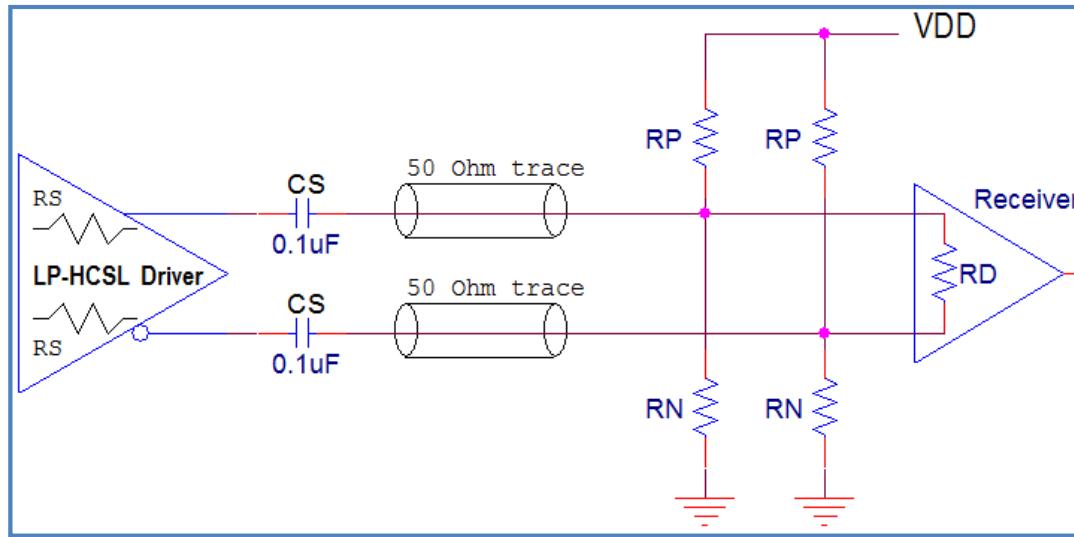


Figure 1 is a schematic of a universal differential clock network. Terminations for each logic type use a subset of this network, and the following paragraphs provide details.

The above schematic uses an LP-HCSL driver with integrated termination resistors (RS). When using a driver where the termination is not integrated, please add an external  $RS = 33\Omega$  in series with each pin to terminate the driver output impedance to  $50\Omega$ . Any external RS should be as close to the driver as possible and be between the driver and any AC coupling capacitor. This allows maximum flexibility in placement of the AC Coupling capacitors along the transmission line. Because the driver side is properly terminated, it is not necessary to terminate at the receiver side. For the receiver side we can focus on creating the proper signal swing and common mode voltage.

CS provides AC coupling so only the signal swing passes to the receiver. RP and RN will re-bias the signal's common mode voltage for the receiver. RP and RN can also attenuate signal swing when smaller resistor values are chosen. This increases the DC current in the network, and if this is unacceptable, an alternative network shown in Figure 2 is recommended.

Some receivers use an integrated differential termination, represented by RD. If RD is integrated in the receiver, we need to include the RD value when calculating the RP and RN values. The most common value for an integrated RD is  $100\Omega$ .

VDD in [Figure 1](#) does not need to be the same VDD value as for the LP-HCSL driver or the Receiver; however RP and RN are assembled near the receiver input, it is usually most convenient to use the receiver VDD.

### Equations for Figure 1:

The Common Mode Voltage depends upon RN, RP and VDD:  $V_{CM} = VDD \times RN / (RN + RP)$

The receiver input signal swing depends upon the additional loading of RN, RP and RD at the receiver input. When RN and RP are much larger than  $50\Omega$  and there is no RD, the single-ended swing at the receiver input will be close to the  $800mV_{pp}$  at the driver. When RP and RN in parallel is  $50\Omega$  or  $RD = 100\Omega$  is present, the single-ended swing will attenuate to  $400mV_{pp}$ .

The following equation calculates the single-ended swing at the receiver input pins:

$$V_{SWING} = 800mV_{pp} \times (RN // RP // \frac{1}{2}RD) / (50 + RN // RP // \frac{1}{2}RD)$$

"//" means "parallel to". This equation assumes a differential signal with equal but opposite waveforms at the two pins of the receiver. The equation can be simplified to the following:

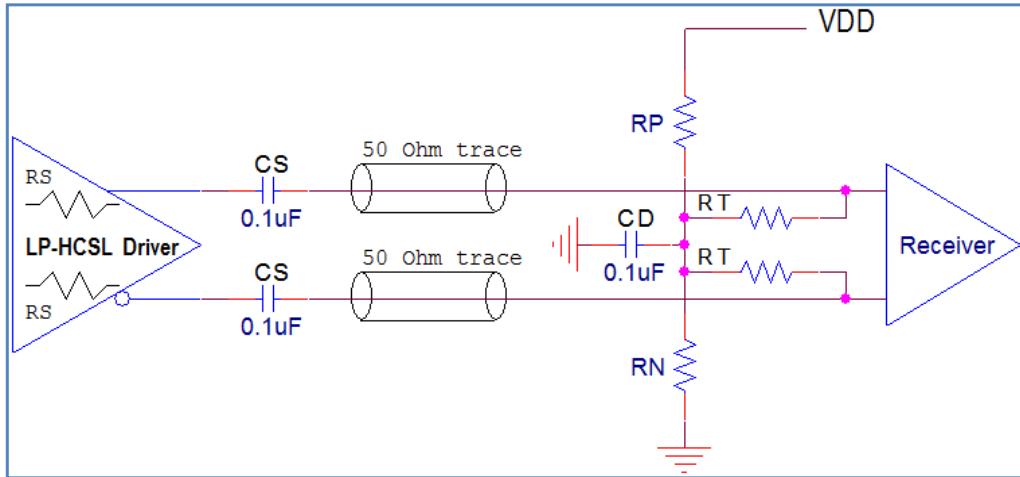
$$V_{SWING} = 800mV_{pp} \times RN \times RP \times RD / (RN \times RP \times RD + 50 \times RN \times RD + 50 \times RP \times RD + 100 \times RN \times RP)$$

When  $RD=100\Omega$ :  $V_{SWING} = 800mV_{pp} \times RN \times RP / (2 \times RN \times RP + 50 \times RN + 50 \times RP)$

When there is no RD:  $V_{SWING} = 800mV_{pp} \times RN \times RP / (RN \times RP + 50 \times RN + 50 \times RP)$

Receivers often specify the required input voltage swing as a differential value. The differential value is two times the single-ended value, so for a differential  $V_{SWING}$  you can multiply the single-ended  $V_{SWING}$  by 2.

### Figure 2. Universal Network with Amplitude Attenuation



[Figure 2](#) shows a slightly modified Universal Network that is most suitable when amplitude attenuation is required and/or reduced DC current is desired. Instead of choosing small values for RP and RN to provide the attenuation as required by the network shown in [Figure 1](#), you can use the RT resistors as a differential load to provide the attenuation. RP and RN can have larger values to limit the DC current in the network.

CD is optional and can help balance the differential waveform at the receiver input. Essentially, CD filters common mode noise that may be present in the VDD.

### Equations for Figure 2:

Common Mode Voltage:  $V_{CM} = VDD \times RN / (RN + RP)$

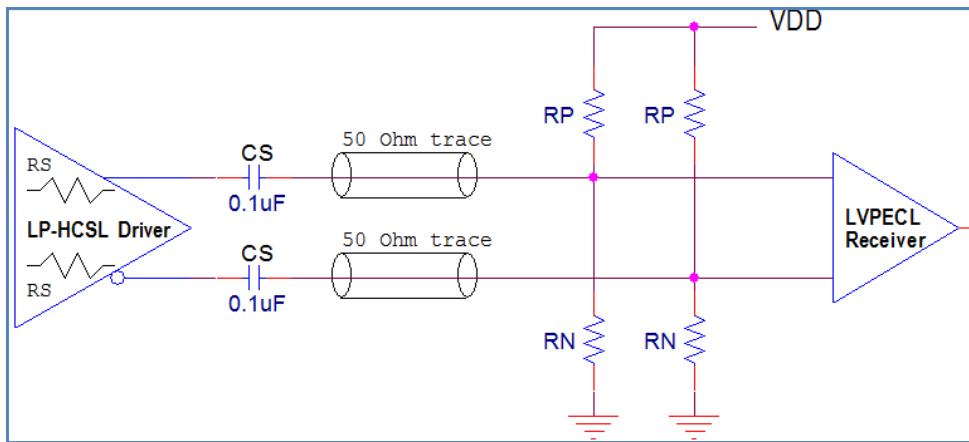
Receiver Input Single-ended Voltage Swing:  $V_{SWING} = 800mV_{pp} \times RT / (50 + RT)$

Rewriting to find RT for the required  $V_{SWING}$ :  $RT = 50 \times V_{SWING} / (800mV_{pp} - V_{SWING})$

## Driving LVPECL

LVPECL needs the full 800mVpp swing, so RP and RN set the common mode voltage while causing as little swing attenuation as possible.

**Figure 3. Terminating LP-HCSL to LVPECL with Network from Figure 1**



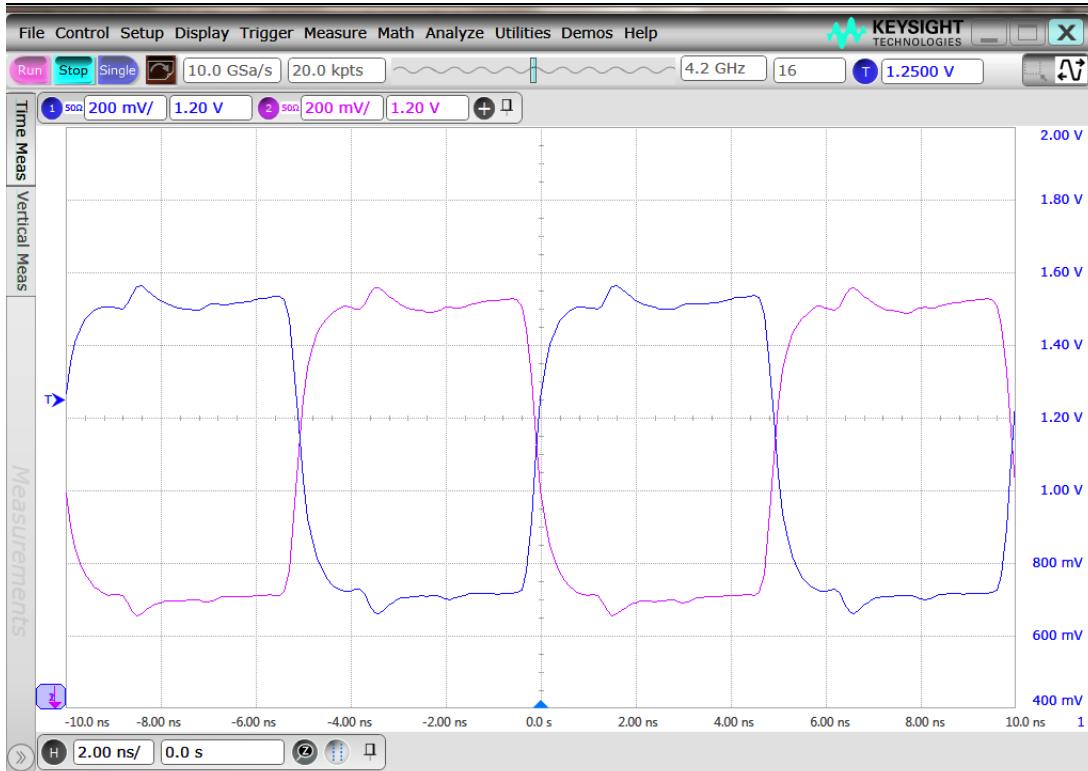
VDD	RP	RN	CS*	V <sub>SWING</sub> **	V <sub>CM</sub>
3.3V	2200 $\Omega$	3300 $\Omega$	0.1 $\mu$ F	771mVpp	1.98V
2.5V	2700 $\Omega$	2400 $\Omega$	0.1 $\mu$ F	770mVpp	1.18V

\* Also add RS = 33 $\Omega$  in series when not integrated in the LP-HCSL driver.

\*\* Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver

Figure 4 shows the measured waveform for the network in Figure 3 with VDD = 2.5V

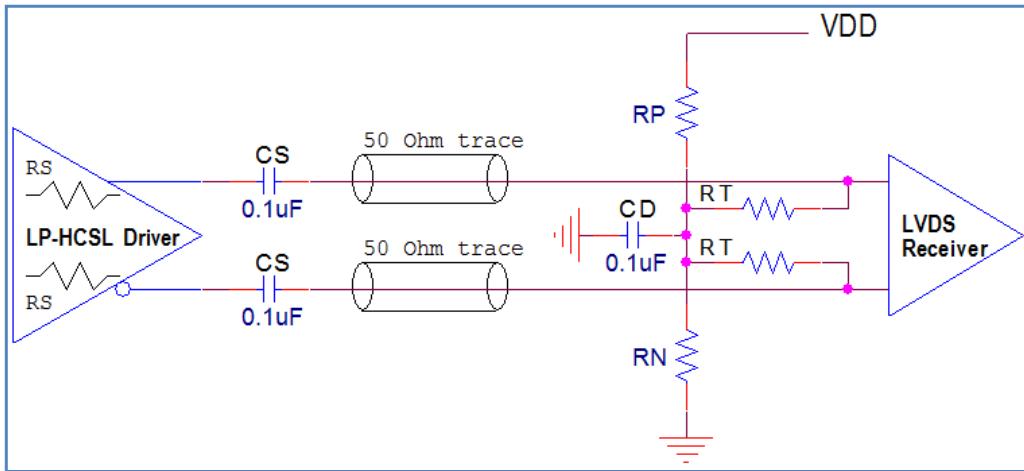
**Figure 4. Measured Waveform at LVPECL Receiver with VDD=2.5V**



## Driving LVDS

LVDS needs 350–400mVpp single-ended swing at each input pin and a common mode voltage of 1.25V. Since LVDS requires both attenuation and a common mode voltage shift, we use the alternate circuit from [Figure 2](#):

**Figure 5. Terminating LP-HSCL to LVDS without Integrated RD**



VDD	RP	RN	RT	CS*	CD**	V <sub>SWING</sub> ***	V <sub>CM</sub>
3.3V	3000Ω	1800Ω	50Ω	0.1μF	0.1μF	400mVpp	1.24V
2.5V	2200Ω	2200Ω	50Ω	0.1μF	0.1μF	400mVpp	1.25V
1.8V	1500Ω	3300Ω	50Ω	0.1μF	0.1μF	400mVpp	1.24V

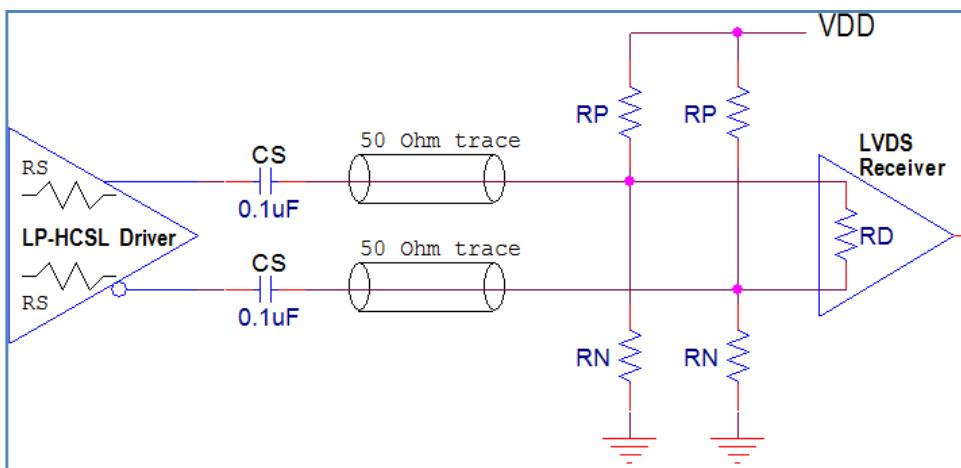
\* Also add  $RS = 33\Omega$  in series when not integrated in the LP-HSCL driver.

\*\* CD is optional for filtering common mode noise in the clock.

\*\*\* Single-ended voltage swing, based upon 800mVpp at the LP-HSCL driver.

If the LVDS receiver has an on-chip differential termination resistor ( $RD = 100\Omega$ ), re-biasing is not necessary and [Figure 1](#) can be used.

**Figure 6. Terminating LP-HSCL to LVDS with Integrated RD**



VDD	RP	RN	RD**	CS*	V <sub>SWING</sub> ***	V <sub>CM</sub>
3.3V	3000 $\Omega$	1800 $\Omega$	100 $\Omega$	0.1 $\mu$ F	391mVpp	1.24V
2.5V	2200 $\Omega$	2200 $\Omega$	100 $\Omega$	0.1 $\mu$ F	391mVpp	1.25V
1.8V	1500 $\Omega$	3300 $\Omega$	100 $\Omega$	0.1 $\mu$ F	391mVpp	1.24V

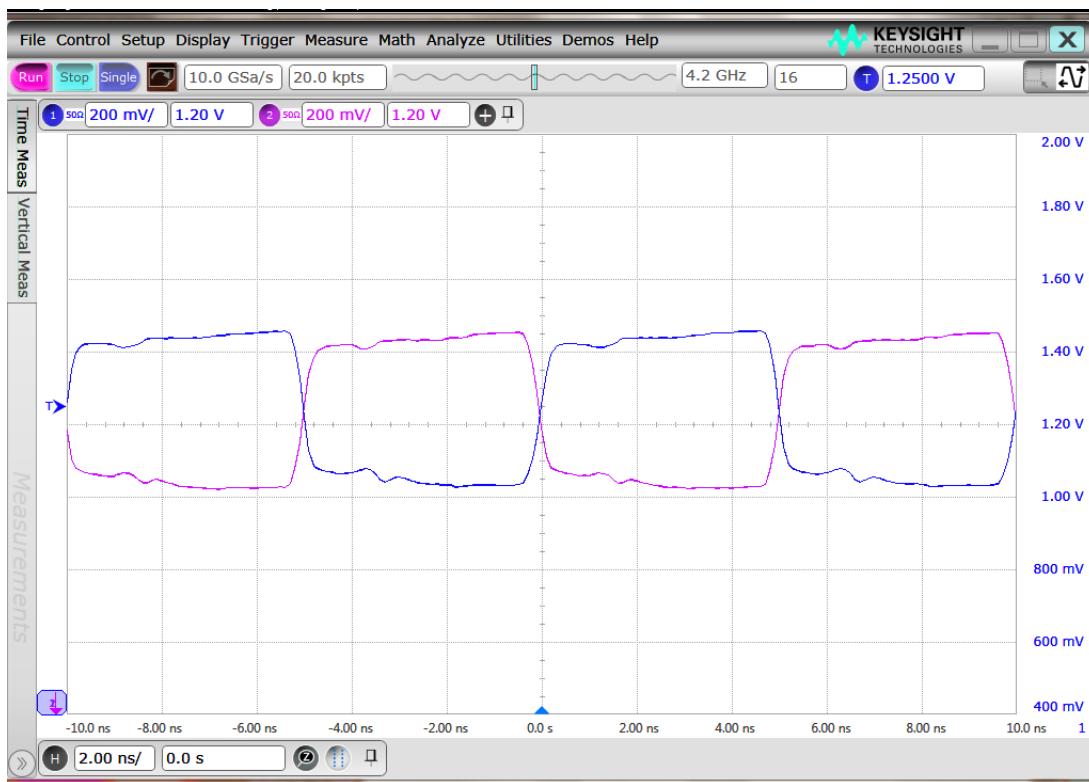
\* Also add RS = 33 $\Omega$  in series when not integrated in the LP-HCSL driver.

\*\* RD is integrated in the receiver so we don't have to assemble it.

\*\*\* Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver

Figure 7 shows the measured waveform for the network shown in Figure 6:

### Figure 7. Measured Waveform at LVDS Receiver



## Driving CML

Normally, CML uses termination resistors connected to VDD at the receiver input. CML needs a single-ended signal swing of 400mVpp and allows the clock to be AC-coupled. Refer to the universal network in [Figure 2](#). RP and RN provide the needed bias since it is AC-coupled.

	VDD***	VDD***	VDD***
Parameter	3.30	2.50	1.80
V <sub>OH</sub>	3.30	2.50	1.80
V <sub>OL</sub>	2.90	2.10	1.40
Common Mode Voltage	3.10	2.30	1.60
RP	2.32K 1%	2.37K 1%	2.49K 1%
RN	36.5K 1%	27.4K 1%	20.0K 1%
RT	50	50	50
V <sub>SWING</sub> **	400mVpp	400mVpp	400mVpp

Also add RS = 33 ohm in series when not integrated in the LP-HCSL driver.

\*\* Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

\*\*\* VDD is the value used for the CML receiver and does not need to be the same as for the LP-HCSL driver.

If the CML receiver has on-chip termination resistors, the 50 ohm RT resistors can not be omitted. Use the RP resistor value for RT to provide the needed biasing.

## Driving SSTL

SSTL signaling is commonly used with DDR memory. SSTL drivers are similar to TTL and CMOS drivers with the exception that SSTL is differential. An SSTL differential input resembles an LVDS or CML input, and can handle large signal swings of up to 0.3V outside the power rails, or small signal swings down to a few hundred millivolts peak-to-peak.

The typical SSTL-driver-to-SSTL-receiver connection is terminated at both the driver side and the receiver side. So, a rail-to-rail swing at the driver will result in a  $0.5 \times \text{VDD}$  peak-to-peak swing at the receiver.

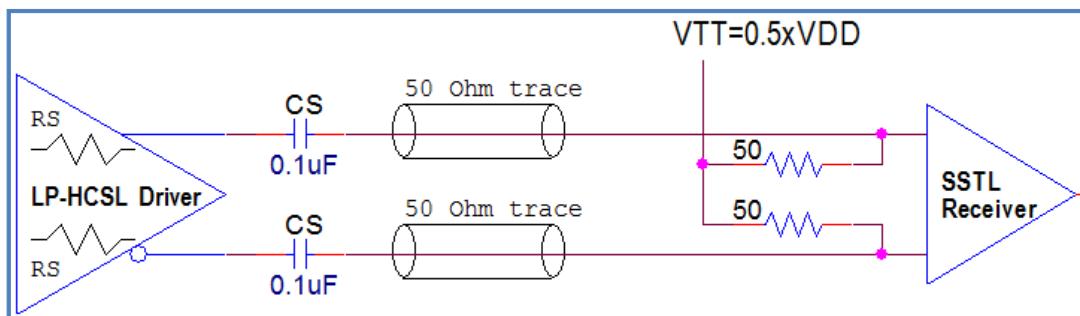
LP-HCSL drivers can drive SSTL receiver inputs. When terminating on both the LP-HCSL driver side and the SSTL receiver side, the typical signal swing at the SSTL receiver input will be 400mVpp. This is enough swing for SSTL-15 (1.5V, DDR3) and SSTL-135 (1.35V, DDR3L). See JESD82-29A for additional DDR3(L) requirements. SSTL-18 (1.8V, DDR2) needs a swing of at least 500mVpp according to JESD8-15A.

When driving actual DDR memory, it is best to follow the JEDEC spec numbers. FPGAs with SSTL compatible inputs can often handle smaller clock signal amplitudes. Please consult the FPGA datasheet for actual clock signal amplitude requirements. For SSTL-18 (DDR2) we can achieve the required amplitude by eliminating the source termination at the LP-HCSL driver side and use only the end termination at the SSTL receiver side. This requires an LP-HCSL driver that does not have the internal termination. With this single termination approach the clock amplitude at the SSTL receiver input reaches 600mVpp.

Logic	VDD1	Application	JEDEC	AC V <sub>SWING</sub> Requirement*
SSTL_18	1.8V	DDR2	JESD8-15A	500mVpp
SSTL_15	1.5V	DDR3	JESD82-29A	350mVpp
SSTL_135	1.35V	DDR3L	JESD82-29A	300mVpp

\* The AC Swing requirement is a larger value than the DC Swing requirement because it includes a margin for noise. When driving a SSTL compatible input on an FPGA, the Swing requirement may be a lower value.

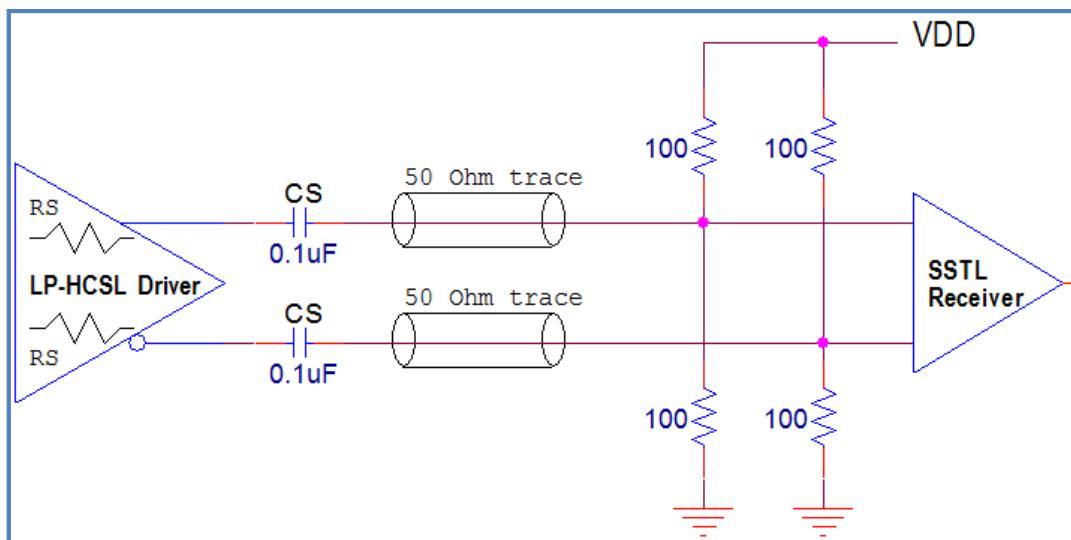
**Figure 8. Recommended Circuit for SSTL-15 and SSTL-135**



VTT is a reference voltage of  $0.5 \times VDD$  that is available with DDR circuits.

In case VTT is not available, the following alternative termination can be used:

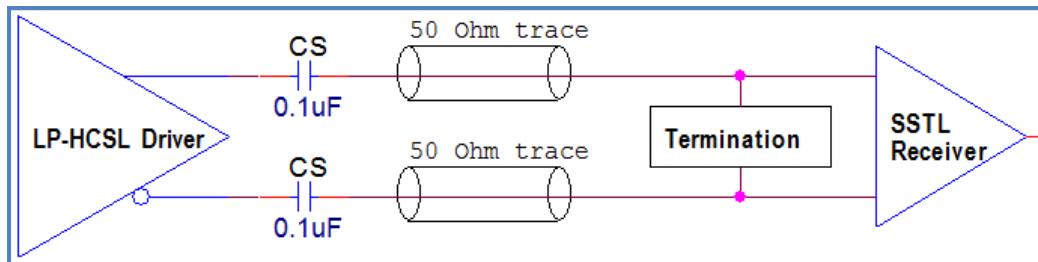
**Figure 9. Recommended Circuit for SSTL-15 and SSTL-135 when VTT is not available**



VDD in both circuits is the VDD of the SSTL receiver. In SSTL or DDR documentation this VDD is often referred to as VDDQ.

For the SSTL-18 (DDR2) case that requires at least 500mVpp of clock signal swing, please use a LP-HCSL driver that does not have internal termination.

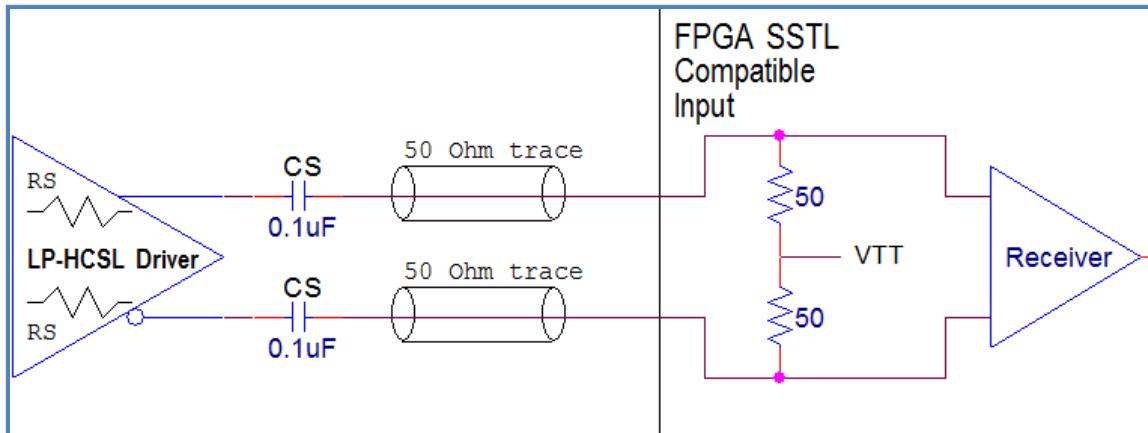
**Figure 10. Recommended Circuit for SSTL-18, using a LP-HCSL Driver without Internal Termination**



The same end terminations as in [Figure 8](#) and [Figure 9](#) can be used with the circuit in [Figure 10](#). The circuits in [Figure 8](#) and [Figure 9](#) are both source and end-terminated, the circuit in [Figure 10](#) is only end-terminated. The LP-HCSL driver without internal termination has an output impedance of  $17\Omega$ . The attenuation with the end termination is now  $50 / (17+50) = 0.75\times$ . Starting with 800mVpp HCSL amplitude, the amplitude at the receiver input is reduced to  $0.75\times 800 = 600\text{mVpp}$ . The situation is similar to LVPECL where you also drive  $50\Omega$  traces with a low impedance driver. The proper  $50\Omega$  termination at the end prevents reflections and preserves signal integrity.

FPGAs may have SSTL compatible inputs with the termination on the chip. In that case the external termination at the SSTL receiver input can be removed and all that's left is the AC coupling capacitors. Also see the section "Driving Generic Differential Inputs".

**Figure 11. Recommended Circuit for SSTL Compatible Inputs on an FPGA**



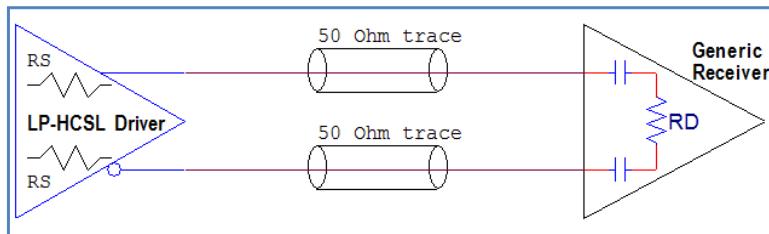
FPGAs often can work with much smaller signal amplitudes at the receiver input than with a standard SSTL input and this circuit can work with many SSTL types.

### Driving Generic Differential Inputs

More ICs are using generic differential receivers, often with an on-chip differential termination resistor. While compatible with LVDS, such devices commonly accept larger signal swings than specified for LVDS. For example, FPGAs commonly have on-chip receiver terminations and require LVDS signal swings at a minimum, while specifying a different common mode voltage. The FPGA datasheet may have a network like that shown in [Figure 1](#) and will recommend values for RP and RN. Below are recommended circuits for driving a variety of generic receiver inputs.

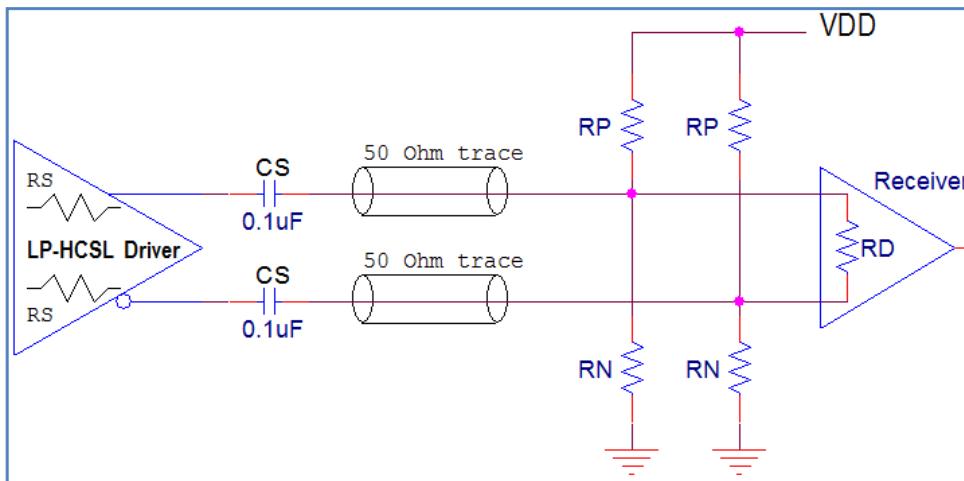
**Figure 12. Terminating LP-HCSL to a Self-biasing Generic Receiver with On-chip Termination and**

## AC-Coupling



Refer to [Figure 12](#). In this case all we need is RS and, when RS is integrated, we can connect the LP-HCSL output directly to transmission line without any additional components. The swing at the receiver input is 400mVpp single-ended or 800mVpp differential. Note, receivers often specify the swing differentially.

**Figure 13. Terminating LP-HCSL to a Generic Receiver with On-chip Termination**

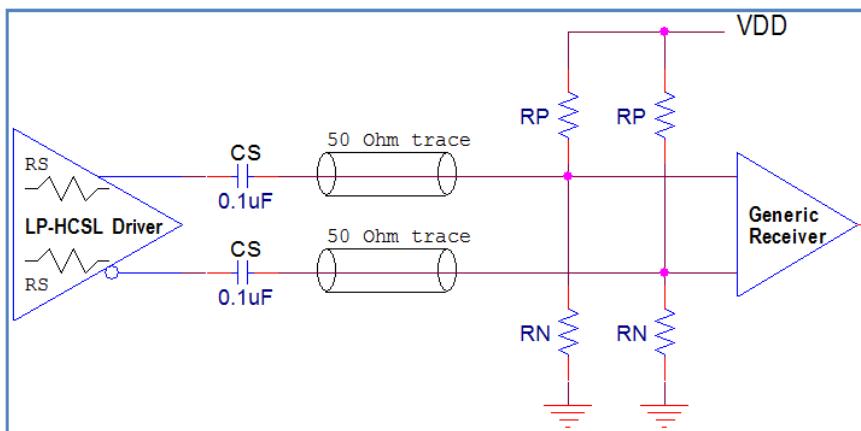


Refer to [Figure 13](#). The receiver datasheet may recommend RP and RN values. If not, use the equation on page 1 to find RP and RN values for the required common mode voltage. Make sure that the resistance value for RN and RP in parallel is at least 1KΩ to minimize DC current in the termination network.

When VDD is the same value as the receiver VDD, and the IC's datasheet does not specify a common mode voltage, a good VCM value is 50%VDD. In this case RP and RN can have the same value, for example 2200Ω each.

The swing at the receiver input is then 391mVpp single-ended for  $RN = RP = 2200\Omega$ ..

**Figure 14. Terminating LP-HCSL to Generic Receiver without Termination or Self-biasing**



Refer to [Figure 14](#). Generic differential receivers can often handle up to 1000mVpp of swing (single-ended) at the input pins. For these receivers attenuation is not needed and it is beneficial to keep the swing as large as possible. For RN and RP values, see the previous circuit for a differential input with on-chip termination.

## 85 Ohm Differential Trace Impedances

Many systems use  $42.5\Omega$  single-ended (or  $85\Omega$  differential) trace impedances and Renesas offers LP-HCSL devices with integrated RS for these systems, as well. The equations in this application note apply to 85 ohm systems with minor changes to resistor and impedance values. The 50 ohm trace becomes a 42.5 ohm trace. This changes the RS value from 33 ohms to  $[33 - (50 - 42.5)]\text{ohms} = (33 - 7.5) \text{ ohms} = 25.5 \text{ ohms}$  for 1% resistors. If 5% resistors are desired, RS becomes 24 ohms.

## Conclusion

Low-power HCSL drivers can be used as a generic differential driver for a wide variety of differential input types. At the same time LP-HCSL can use up to 9x less power than traditional HCSL drivers, and up to 19x less power than LVPECL, LVDS or CML drivers.

## Revision History

Revision Date	Description of Change
December 5, 2023	<ul style="list-style-type: none"><li>▪ Updated descriptive text under <a href="#">Figure 2</a>; replaced “clock signal” with “VDD”.</li><li>▪ Updated <a href="#">Driving CML</a> section.</li></ul>
July 16, 2015	Initial release.

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