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2010年4月1日
瑞萨电子公司

【发行】瑞萨电子公司（<http://www.renesas.com>）

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H8/300L Super Low Power 系列

8 位 BCD 的除法

要点

进行 8 位 BCD（2 进制编码 10 进制数）的除法运算，并将除法结果（8 位 BCD）设定到通用寄存器。

动作确认器件

H8/38024

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1. 参数

	内容	保存位置	数据长度（字节）
输入	被除数	R0、R1	4
	除数	R2、R3	4
输出	除法结果（商）	R0、R1	4
	除法结果（余数）	R4、R5	4
	有无错误	Z 标志（CCR）	1

2. 内部寄存器变化和标志变化

R0	R1
○	○
R2	R3
•	•
R4	R5
○	○
R6	R7
×	×

I	U	H	U
•	•	×	•
N	Z	V	C
×	○	×	×

•：不变，×：不定，○：结果

3. 程序设计

程序存储器（字节）
84
数据存储器（字节）
0
堆栈（字节）
0
时钟周期数
1162
重入
可
再定位
可
中途中断
可

4. 注意事项

规格的时钟周期数是进行了 $99999999 \div 9999$ 运算时的值。

5. 说明

5.1 功能

(1) 参数的详细内容如下：

- R0: 设定 8 位 BCD (32 位长) 被除数的高 4 位
执行软件 DIVD 后, 设定 8 位 BCD 除法结果 (商) 的高 4 位。
- R1: 设定 8 位 BCD (32 位长) 被除数的低 4 位。
执行软件 DIVD 后, 设定 8 位 BCD 除法结果 (商) 的低 4 位。
- R2: 输入参数, 设定 8 位 BCD 除数的高 4 位。
- R3: 输入参数, 设定 8 位 BCD 除数的低 4 位。
- R4: 输出参数, 设定 8 位 BCD 余数的高 4 位。
- R5: 输出参数, 设定 8 位 BCD 余数的低 4 位。
- Z 标志 (CCR): 输出参数, 表示在软件 DIVD 执行中有无错误 (被 0 除)。
Z 标志= 1: 表示除数是 “0”, 为错误。
Z 标志= 0: 表示除数不是 “0”。

(2) 软件 DIVD 的执行例子如图 22-1 所示。

一旦如①设定输入参数, 就如②设定除法结果。

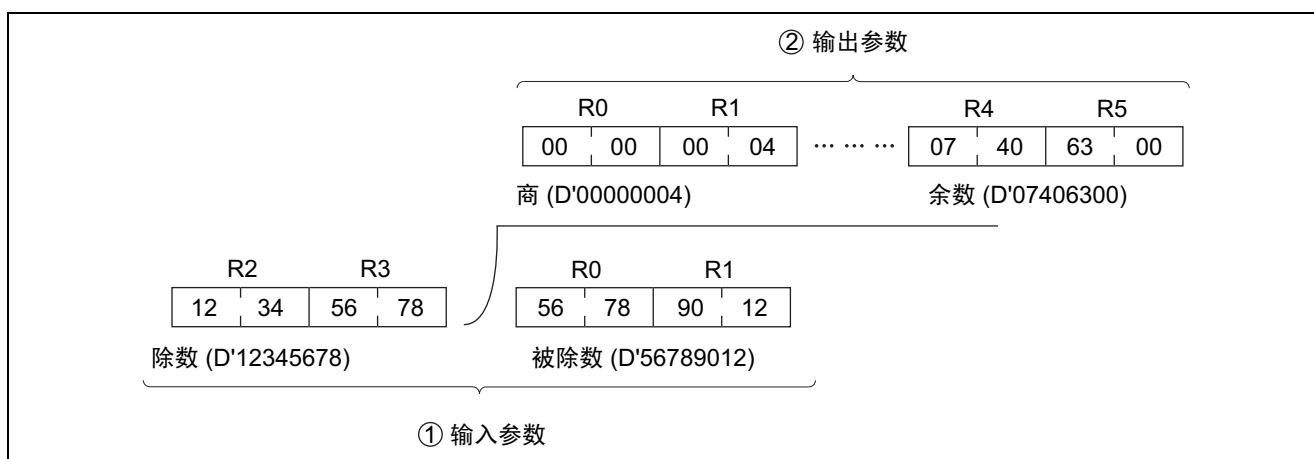


图 22-1 软件 DIVD 的执行例子

(3) 输入参数置 “0” 时的结果如表 22-1 所示。

表 22-1 输入参数置 “0” 时的结果

输入参数		输出参数		
被除数 (R0、R1)	除数 (R2、R3)	商 (R0、R1)	余数 (R4、R5)	错误 (Z)
H'*****	H'00000000	H'*****	H'00000000	1
H'00000000	H'*****	H'00000000	H'00000000	0
H'00000000	H'00000000	H'00000000	H'00000000	1

【注】 H'****表示 16 进制数。

5.2 使用时的注意

- (1) 如图 22-2，如果不使用高位，就必须将它置“0”。如果不置“0”，因为进行含有被设定在高位的不定数据的除法运算，所以就得不到正确的除法结果。

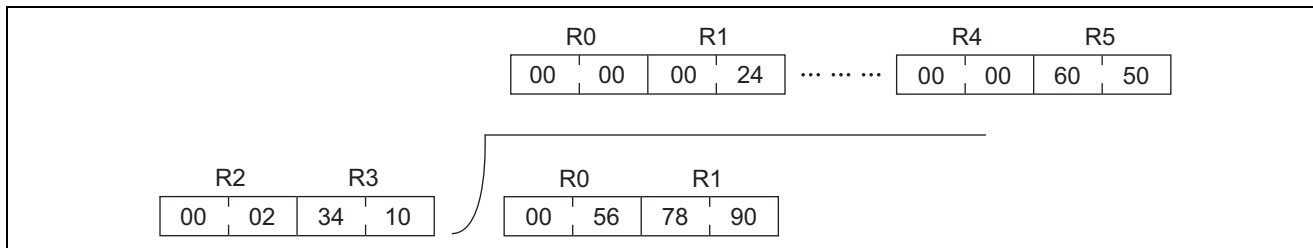


图 22-2 不使用高位的除法例子

- (2) 因为执行软件 DIVD 后商被设定到 R0、R1，所以将破坏被除数。如果执行后还需要被除数，就必须预先保存到存储器。

5.3 数据存储器的说明

软件 DIVD 不使用数据存储器。

5.4 使用例

设定被除数和除数，子程序调用软件 DIVD。

WORK1	.RES. W 2	...	...	确保用户程序设定8位BCD被除数的数据存储器区。
WORK2	.RES. W 2	...	...	确保用户程序设定8位BCD除数的数据存储器区。
WORK3	.RES. W 2	...	...	确保用户程序设定8位BCD商的数据存储器区。
WORK4	.RES. W 2	...	...	确保用户程序设定8位BCD余数的数据存储器区。
	...			
	MOV. W @WORK1, R0	}	...	将用户程序设定的8位BCD被除数设定到输入参数。
	MOV. W @WORK1+2, R1		...	
	...			
	MOV. W @WORK2, R2	}	...	将用户程序设定的8位BCD除数设定到输入参数。
	MOV. W @WORK2+2, R3		...	
	...			
	JSR @DIVD		...	子程序调用软件DIVD。
	...			
	BEQ ERROR		...	除法结果发生错误（被除0）时，向处理程序转移。
	...			
	MOV. W R0, @WORK3	}	...	将设定在输出参数中的除法结果保存到用户程序的数据存储器。
	MOV. W R1, @WORK3+2		...	
	MOV. W R4, @WORK4		...	
	MOV. W R5, @WORK4+2		...	
	...			
ERROR	被除0的处理程序			
	...			

5.5 工作原理

(1) 10 进制的除法能通过重复减法实现。

除法例子 ($64733088 \div 5$) 如图 22-3 所示。

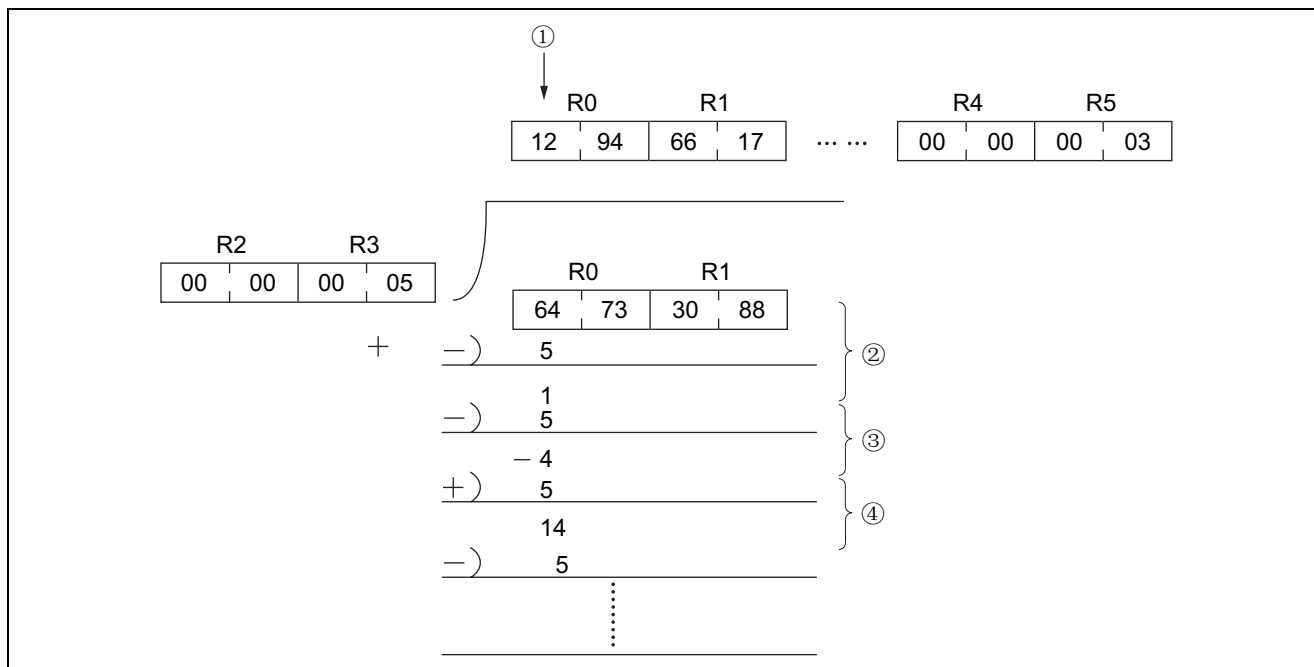
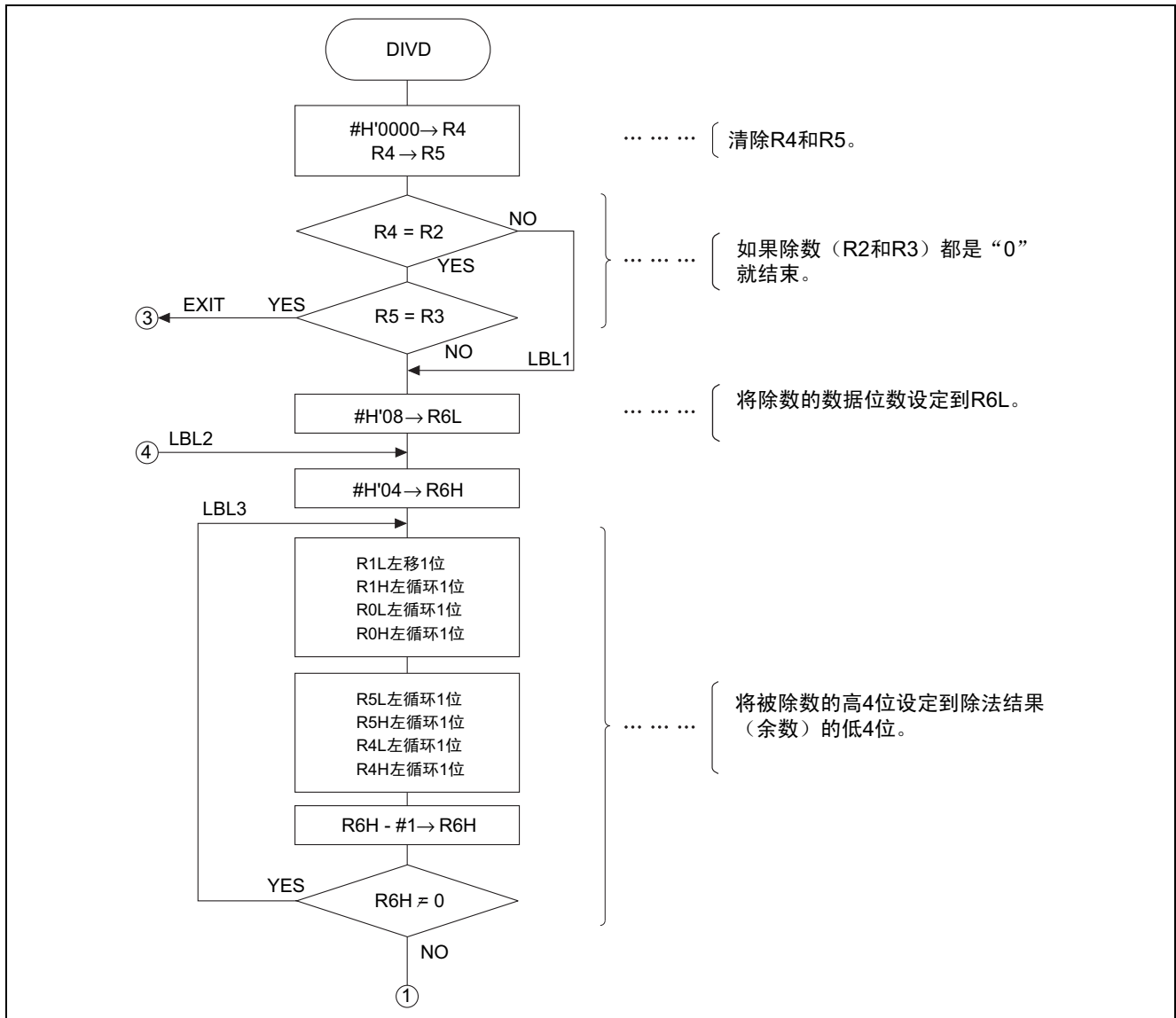


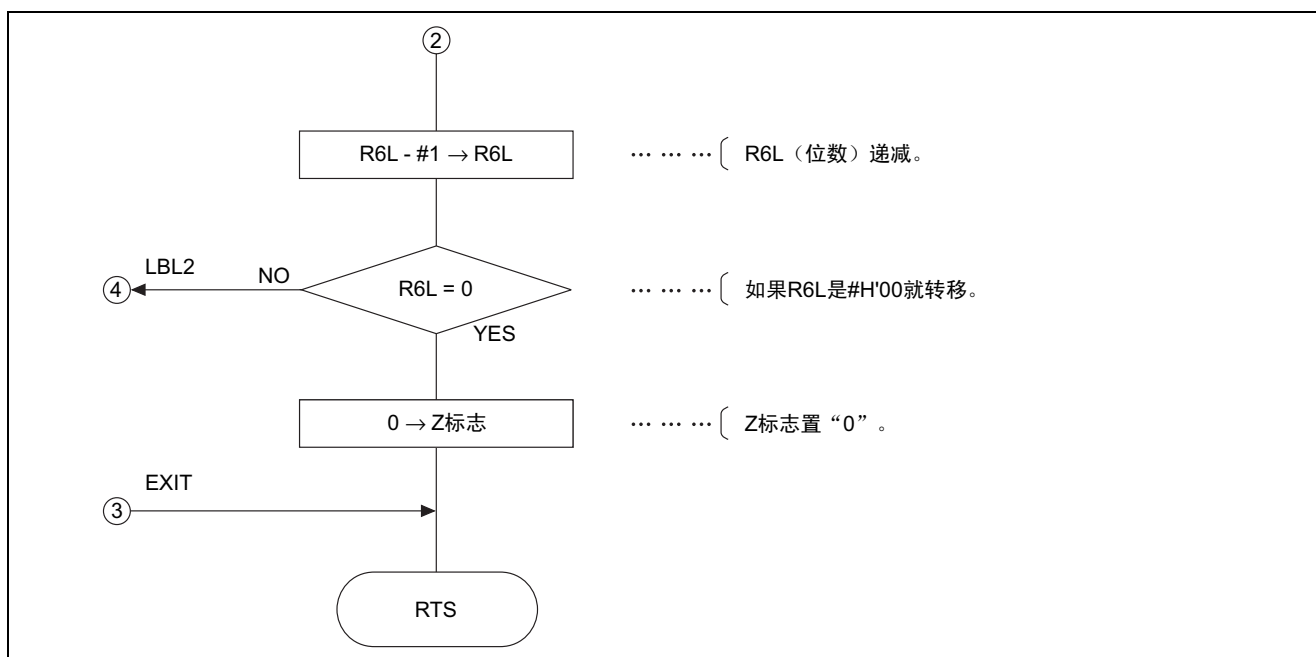
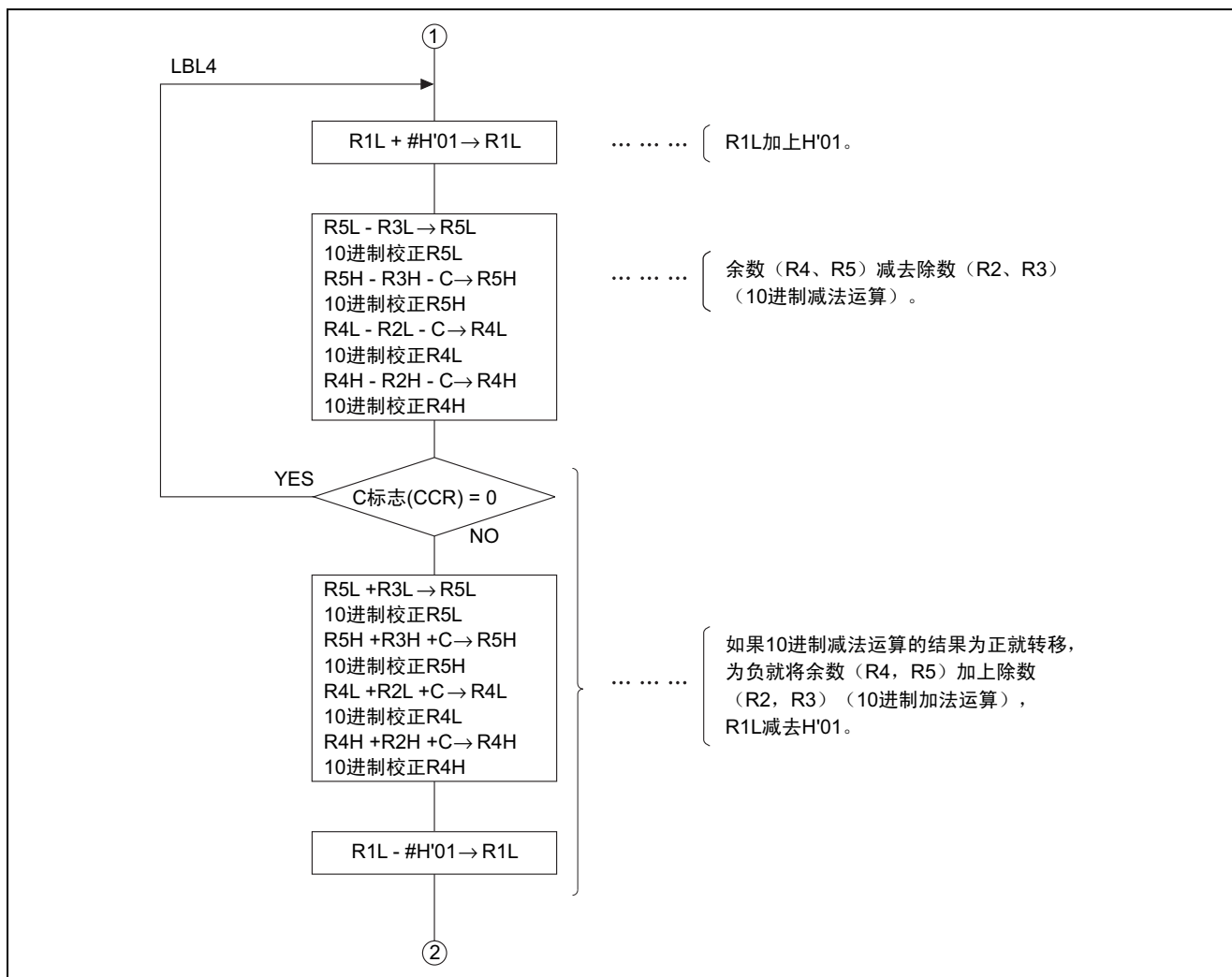
图 22-3 除法例子 ($64733088 \div 5$)

(2) 以下说明程序的详细内容:

- 被除数左移 4 位 (BCD 的 1 位)，将被除数的高 4 位设定到除法结果 (余数) 的低 4 位。
- 被除数减去除数。直到减法结果为负，重复减法运算，并将减法次数设定到低 4 位 (最低位) (图 22-3 ②→③→①)。
- 如果减法结果为负，就将减法结果 (余数) 加上除数，恢复到减法运算前的数值 (图 22-3 ④)。
- 重复 8 位数次 (a)~(b) 的处理。

6. 流程图





7. 程序清单

*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:02:05

PROGRAM NAME =

```

1          ;*****
2          ;*
3          ;*      00 - NAME :MULTIPLE-PRECISION DECIMAL DIVISION (DIVD)
4          ;*
5          ;*****
6          ;*
7          ;*      ENTRY      :R2,R3      (DIVISOR)
8          ;*                  R0,R1      (DIVIDEND)
9          ;*
10         ;*      RETURNS   :R0,R1      (QUOTIENT)
11         ;*                  R4,R5      (RESIDUAL)
12         ;*                  Z flag OF CCR (Z=1;FALSE , Z=0;TRUE)
13         ;*
14         ;*****
15         ;
16 DIVD_cod C 0000          .SECTION      DIVD_code, CODE, ALIGN=2
17                          .EXPORT      DIVD
18                          ;
19 DIVD_cod C      00000000 DIVD .EQU      $          ;Entry point
20 DIVD_cod C 0000 79040000      MOV.W      #H'0000, R4      ;Clear R4
21 DIVD_cod C 0004 0D45          MOV.W      R4, R5          ;Clear R5
22 DIVD_cod C 0006 1D42          CMP.W      R4, R2
23 DIVD_cod C 0008 4604          BNE        LBL1              ;Branch if Z=0
24 DIVD_cod C 000A 1D53          CMP.W      R5, R3
25 DIVD_cod C 000C 4744          BEQ        EXIT              ;Branch if Z=1 then exit
26 DIVD_cod C 000E          LBL1          MOV.B      #H'08, R6L      ;Set bit counter1
27 DIVD_cod C 000E FE08          LBL2          MOV.B      #H'04, R6H      ;Set bit counter2
28 DIVD_cod C 0010          LBL3          SHLL.B      R1L          ;Shift dividend
29 DIVD_cod C 0010 F604          ROTXL.B     R1H
30 DIVD_cod C 0012          ROTXL.B     R0L
31 DIVD_cod C 0012 1009          ROTXL.B     R0H
32 DIVD_cod C 0014 1201          ROTXL.B     R5L
33 DIVD_cod C 0016 1208          ROTXL.B     R5H
34 DIVD_cod C 0018 1200          ROTXL.B     R4L
35 DIVD_cod C 001A 120D          ROTXL.B     R4H
36 DIVD_cod C 001C 1205          DEC.B      R6H              ;Decrement bit counter2
37 DIVD_cod C 001E 120C          BNE        LBL3              ;Branch if Z=0
38 DIVD_cod C 0020 1204          LBL4          INC.B      R1L          ;Increment R1L
39 DIVD_cod C 0022 1A06          SUB.B      R3L, R5L          ;R5L - R3L -> R5L
40 DIVD_cod C 0024 46EC          DAS.B      R5L              ;Decimal adjust R5L
41 DIVD_cod C 0026          SUBX.B      R3H, R5H          ;R5H - R3H - C -> R5H
42 DIVD_cod C 0026 0A09          DAS.B      R5H              ;Decimal adjust R5H
43 DIVD_cod C 0028 18BD          SUBX.B      R2L, R4L          ;R4L - R2L - C -> R4L
44 DIVD_cod C 002A 1F0D          DAS.B      R4L              ;Decimal adjust R4L
45 DIVD_cod C 002C 1E35          SUBX.B      R2H, R4H          ;R4H - R2H - C -> R4H
46 DIVD_cod C 002E 1F05          DAS.B      R4H              ;Decimal adjust R4H
47 DIVD_cod C 0030 1EAC          BCC        LBL4              ;Branch if C=0
48 DIVD_cod C 0032 1F0C          ADD.B      R3L, R5L          ;R3L + R5L -> R5L
49 DIVD_cod C 0034 1E24          ;
50 DIVD_cod C 0036 1F04          ;
51 DIVD_cod C 0038 44EC          ;
52          ;
53 DIVD_cod C 003A 08BD          ;

```

```

54 DIVD_cod C 003C 0F0D          DAA.B      R5L          ;Decimal adjust R5L
55 DIVD_cod C 003E 0E35          ADDX.B     R3H,R5H       ;R3H + R5H + C -> R5H
56 DIVD_cod C 0040 0F05          DAA.B      R5H          ;Decimal adjust R5H
57 DIVD_cod C 0042 0EAC          ADDX.B     R2L,R4L       ;R2L + R4L + C -> R4L
58 DIVD_cod C 0044 0F0C          DAA.B      R4L          ;Decimal adjust R4L
59 DIVD_cod C 0046 0E24          ADDX.B     R2H,R4H       ;R2H + R4H + C -> R4H
60 DIVD_cod C 0048 0F04          DAA.B      R4H          ;Decimal adjust R4H
61 DIVD_cod C 004A 1A09          DEC.B      R1L          ;Decrement R1L
62 DIVD_cod C 004C 1A0E          DEC.B      R6L          ;Decrement bit counter1
63 DIVD_cod C 004E 46C0          BNE        LBL2
64 DIVD_cod C 0050 06FB          ANDC.B     #B'11111011,CCR ;Clear Z flag of CCR
65 DIVD_cod C 0052              EXIT
66 DIVD_cod C 0052 5470          RTS
67                               ;
68                               .END
*****TOTAL ERRORS      0
*****TOTAL WARNINGS    0

```

修订记录

Rev.	发行日	修订内容	
		页	修订要点
1.00	2005.07.29	—	初版发行

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