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H8/300L SLP 系列

通过事件计数器功能测定脉冲频率

要点

使用定时器 C 的 8 位事件计数器功能，测定从定时器 C 事件输入管脚（TMIC）输入的脉冲频率。

动作确认器件

H8/38024

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1. 规格

- (1) 使用定时器 C 的 8 位事件计数器功能，测定定时器 C 事件输入管脚（TMIC）输入的脉冲频率。
- (2) 将从 TMIC 输入管脚输入的脉冲上升沿检测的次数进行 1sec 间的累加计数，将 1sec 间的计数保存到 RAM。
- (3) 使用定时器 A 时钟时基功能测量 1sec 的测定时间。
- (4) 将 UD 管脚连接到 GND，将定时器 C 的计数器（TCC）设定为硬件控制的递增计数器。

2. 使用功能说明

- (1) 在本例子中，使用定时器 C 的 8 位事件计数器功能，测定 TMIC 输入管脚输入的脉冲频率。
 - (a) 定时器 C 的 8 位事件计数器功能的框图如图 1 所示。以下说明有关定时器 C 的 8 位事件计数器功能的框图。
 - 定时器模式寄存器 C（TMC）是 8 位可读写的寄存器，进行间隔功能的选择、定时器计数器 C（TCC）的递增/递减控制以及输入时钟的选择。TCC 的递增/递减控制选择是由 UD 管脚输入进行硬件控制还是由软件控制递增计数器或递减计数器。
 - 定时器计数器 C（TCC）是 8 位可读的计数器，由输入的时钟/外部事件进行累加/递减计数。输入的时钟可从系统时钟的 8192、2048、512、64、16、4 分频、或子时钟的 4 分频以及外部时钟共 8 种的时钟中选择。在本例子中，将 TCC 设定为硬件控制的递增计数器，对 TCC 的输入时钟选择 TMIC 输入管脚的边沿检测。
 - 定时器 C 中断请求标志（IRRTC）通过 TCC 溢出置“1”。在 IRRTC 被置“1”、中断允许寄存器 2（IENR2）的定时器 C 中断允许（IENTC）为“1”并且条件码寄存器（CCR）的 I 位被清“0”时，受理定时器 C 中断，开始定时器 C 中断处理。
 - 定时器 C 事件输入管脚（TMIC）作为进行频率测定的脉冲输入管脚。

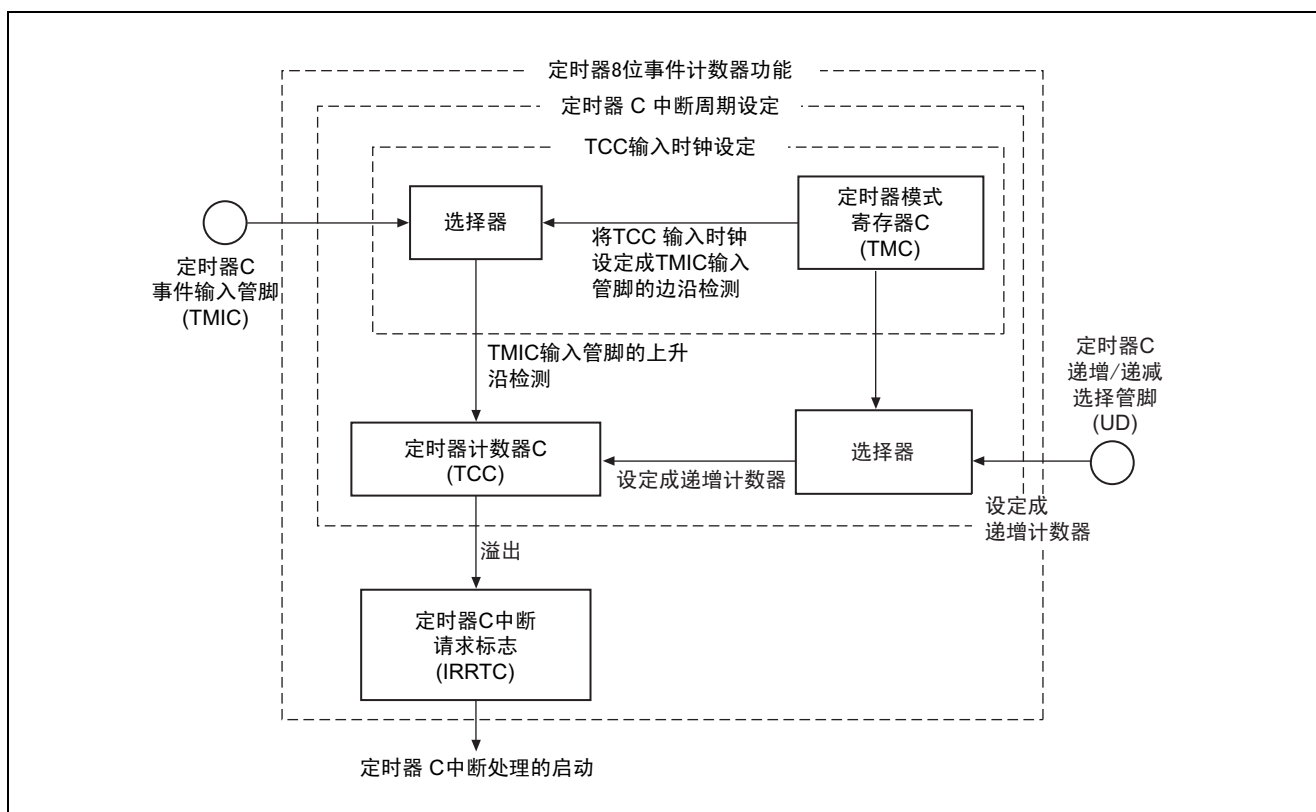


图 1 定时器 C 的 8 位事件计数器功能的框图

(b) 以下说明有关频率的测定方法

- 如果对 TMIC 输入管脚输入 256 次的上升沿，TCC 就溢出，发生定时器 C 中断。
- 在定时器 C 中断处理中，使 8 位计数器 cnt1 递增。
- 在经过 1sec 时，将 TCC 的计数值保存到 cnt2，结束使用 TMIC 输入端子的 TCC 的累加计数。
- 输入到 TMIC 管脚的脉冲频率按以下公式计算。

$$\text{输入脉冲的频率 (Hz)} = (\text{定时器 C 中断发生的次数}) \times 256 + (\text{经过 1sec 时刻的 TCC 的计数器值})$$

$$= (\text{cnt1 的值}) \times 256 + (\text{cnt2 的值})$$
- 因为对定时器 C 中断发生次数进行计数的计数器 (cnt1) 是 8 位计数器，所以可测定的最大输入脉冲频率是 65.535kHz。
- 如果对定时器 C 中断次数进行计数的 8 位计数器 (cnt1) 溢出，就中止此时的频率测定，并且对 cnt1 和保存在经过 1sec 时 TCC 计数器值的寄存器 (cnt2) 写 H'00 后结束。

(2) 本例子的功能分配如表 1 所示。分配如表 1 所示的功能，由定时器 C 的 8 位事件计数器功能进行频率测定。

表 1 功能分配

功能	功能分配
PSW	将 32.768kHz 的 4 分频后的时钟作为输入的 5 位计数器
TMA	选择 PSW，设定 TCA 溢出周期
TCA	将 32.768kHz 的 128 分频后的时钟作为输入的 8 位计数器
TMC	设定间隔功能，将 TCC 设定为硬件控制的递增计数器，并且将 TCC 输入时钟设定为 TMIC 输入管脚的边沿检测
TCC	将 TMIC 输入管脚的边沿检测作为输入的 8 位计数器
TLC	将 TCC 溢出时的再装入值设定为 0x00
IRQ1	将 PB3/AN3/IRQ1 管脚设定为 TMIC 输入管脚
IEG1	将 TMIC 管脚的输入检测设定为上升沿检测
IENTA	允许定时器 A 中断请求
IENTC	允许定时器 C 中断请求
IRRTA	反映定时器 A 中断请求的有无
IRRTC	反映定时器 C 中断请求的有无
TMIC	进行频率测定的脉冲输入管脚
UD 管脚	将 TCC 设定为递增计数器的输入管脚

3. 运行说明

(1) 如图 2 所示。根据如图 2 所示的硬件处理和软件处理，由定时器 C 的 8 位事件计数功能进行脉冲频率的测定。

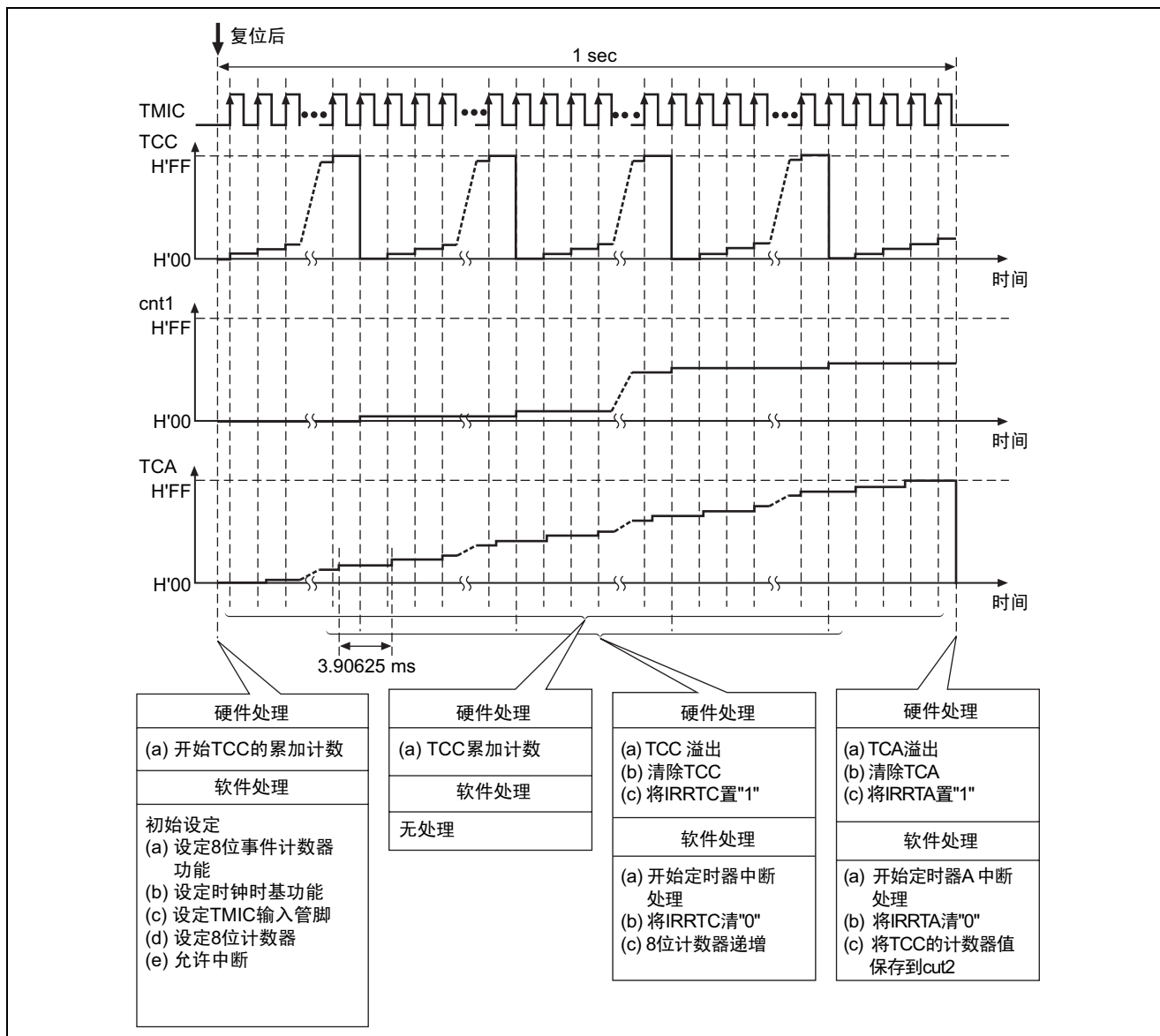


图 2 由定时器 C 的 8 位事件计数器功能进行频率测定的运行说明

4. 软件说明

(1) 模块说明

本例子的模块如表 2 所示。

表 2 模块说明

模块名	标号名	功能
主程序	main	进行定时器 C 的 8 位事件计数器功能的设定、时钟时基功能的设定、8 位计数器的设定、中断的允许、测定结束后定时器 C 的初始化。
经过 1sec	taint	是定时器 A 的中断处理，经过 1sec 禁止中断，将 TCC 的计数器值保存到 cnt2。
8 位计数器	tcint	是定时器 C 的中断处理，进行 8 位计数器的递增和 cnt1 溢出时的处理

(2) 参数说明

本例子使用的参数如表 3 所示。

表 3 参数的说明

参数名	功能	使用模块名	数据长	输入/输出
cnt1	保存经过 1sec 时的 8 位计数器的计数器值	8 位计数器	1 字节	输出
cnt2	保存经过 1sec 时的 TCC 计数器值	1sec	1 字节	输出

(3) 内部寄存器说明

本例子使用的内部寄存器如表 4 所示。

表 4 使用内部寄存器的说明

寄存器名	功能	地址	设定值
TMA	定时器模式寄存器 A ： TMA=H'18 时，将定时器 A 功能设定为时钟时基功能，将 TCA 输入时钟源设定为 PSW，将 TCA 溢出周期设定为 1sec	H'FFB0	H'18
TCA	定时器计数器 A ： 将 32.768kHz 的 128 分频的时钟作为输入的 8 位递增计数器	H'FFB1	H'00
TMC	定时器模式寄存器 C ： TMC=H'7F 时，将定时器 C 功能设定为间隔功能，将 TCC 设定为硬件控制的递增计数器，将 TCC 输入时钟设定为 TMIC 管脚的输入边沿检测	H'FFB4	H'7F
TCC	定时器计数器 C ： 将 MIC 管脚的输入边沿检测作为输入的 8 位递增计数器	H'FFB5	H'00
TLC	定时器装入寄存器 C ： 如果设定为 TLC=H'00, TCC 就从 H'00 开始累加计数, 如果 TCC 溢出就将 H'00 装入 TCC	H'FFB5	H'00
PMR3	UD 端口模式寄存器 3 (P30/UD 端子转换) ： UD="0"时，作为 P30 输入/输出管脚功能 ： UD="1"时，作为 UD 输入管脚功能	H'FFCA 位 0	1

表 4 使用内部寄存器的说明（续）

寄存器名		功能	地址	设定值
PMRB	IRQ1	端口模式寄存器 B (PB3/AN3/IRQ1 管脚转换) : IRQ1="0"时, 作为 PB3/AN3 输入管脚功能 : IRQ1="1"时, 作为 $\overline{\text{IRQ1}}$ /TMIC 输入管脚功能	H'FFEE 位 3	1
IEGR	IEG1	IRQ 边沿选择寄存器 (IRQ1 边沿选择) : IEG1=0 时, 将 TMIC 输入管脚的边沿检测设定为下降沿 : IEG1=1 时, 将 TMIC 输入管脚的边沿检测设定为上升沿	H'FFF2 位 1	1
IENR1	IENTA	中断允许寄存器 1 (定时器 A 中断允许) : IENTA=0 时, 禁止定时器 A 中断请求 : IENTA=1 时, 允许定时器 A 中断请求	H'FFF3 位 7	1
IENR2	IENTC	中断允许寄存器 2 (定时器 C 中断允许) : IENTC=0 时, 禁止定时器 C 中断请求 : IENTC=1 时, 允许定时器 C 中断请求	H'FFF4 位 1	1
IRR1	IRRTA	中断请求寄存器 1 (定时器 A 中断请求标志) : IRRTA=0 时, 没发生定时器 A 中断请求 : IRRTA=1 时, 发生定时器 A 中断请求	H'FFF6 位 7	0
IRR2	IRRTC	中断请求寄存器 2 (定时器 C 中断请求标志) : IRRTC=0 时, 没发生定时器 C 中断请求 : IRRTC=1 时, 发生定时器 C 中断请求	H'FFF7 位 1	0

(4) 使用 RAM 说明

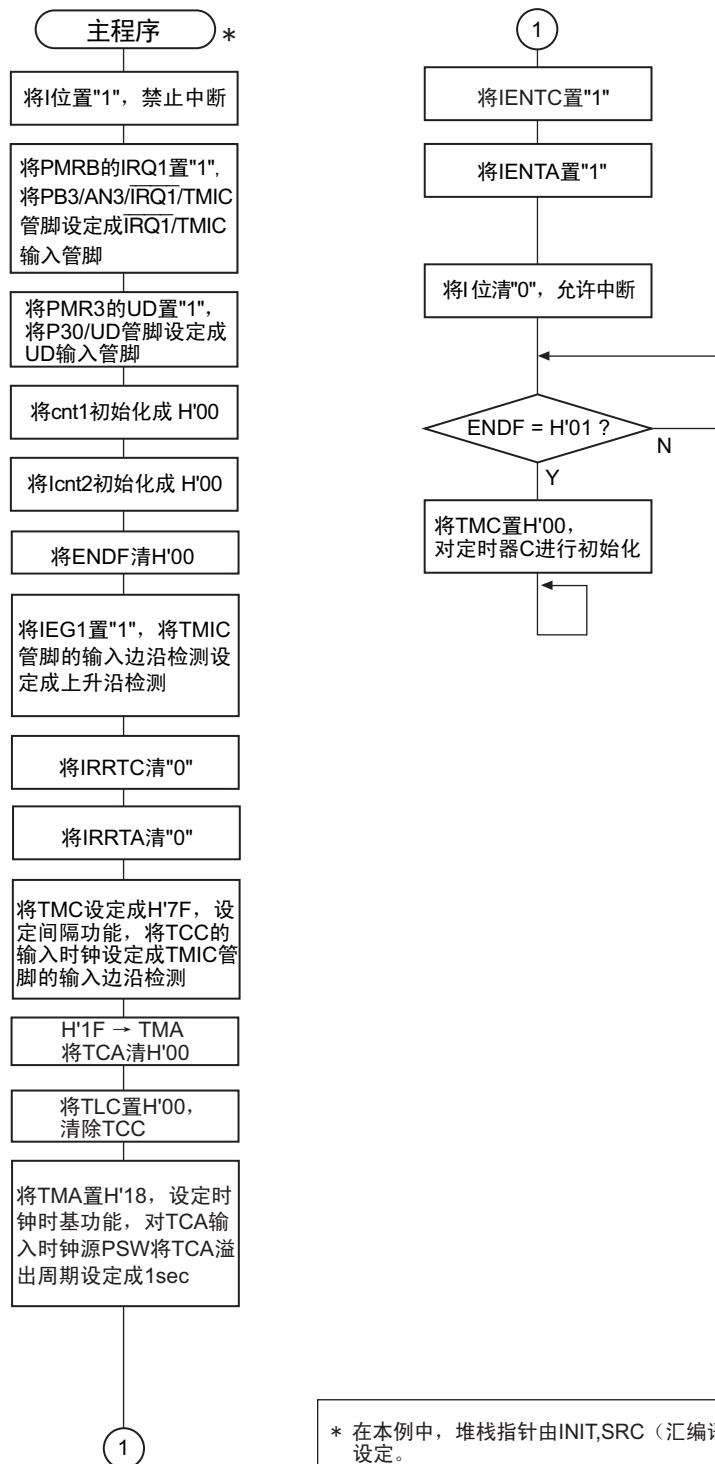
本例子使用的 RAM 如表 5 所示。

表 5 使用 RAM 的说明

标号名	功能	地址	使用模块名
cnt1	保存经过 1sec 时的 8 位计数器的计数器值	H'FB80	8 位计数器
cnt2	保存经过 1sec 时的 TCC 计数器值	H'FB81	经过 1sec
ENDF	判断输入脉冲的频率测定是否结束的数据 测定时间未满 1sec 且 cnt1<H'FF 时, ENDF=H'00 处理时间经过 1sec 或 cnt1=H'FF 时, ENDF=H'01	H'FB82	主程序 8 位计数器 经过 1sec

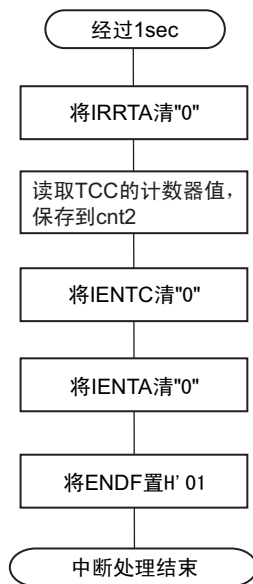
5. 流程图

(1) 主程序

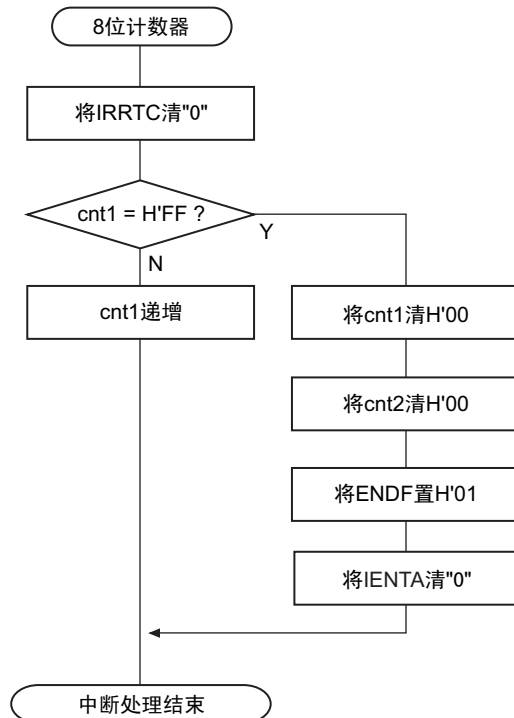


* 在本例中, 堆栈指针由INIT,SRC (汇编语言) 设定。

(2) 定时器A中断处理程序



(3) 定时器C中断处理程序



6. 程序清单

6.1 INIT.SRC (程序清单)

```

.EXPORT  _INIT
.IMPORT  _main
;
.SECTION P, CODE
_INIT:
    MOV.W    #H'FF80, R7
    LDC.B    #B'10000000, CCR
    JMP      @_main
;
.END

/*****
/*
/*                                     */
/* H8/300L Super Low Power Series      */
/* -H8/38024 Series-                  */
/* Application Note                    */
/*                                     */
/* 'Pulse Frequency Measurement by Event Counter Function'
/*                                     */
/* Function                            */
/* :Timer C 8bit Event Counter         */
/*                                     */
/* External Clock : 10MHz               */
/* Internal Clock : 5MHz               */
/* Sub Clock      : 32.768kHz          */
/*                                     */
*****/

#include <machine.h>

/*****
/* Symbol Definition                    */
*****/
struct BIT {
    unsigned char  b7:1;    /* bit7 */
    unsigned char  b6:1;    /* bit6 */
    unsigned char  b5:1;    /* bit5 */
    unsigned char  b4:1;    /* bit4 */
    unsigned char  b3:1;    /* bit3 */
    unsigned char  b2:1;    /* bit2 */
    unsigned char  b1:1;    /* bit1 */
    unsigned char  b0:1;    /* bit0 */
};

#define TMA      *(volatile unsigned char *)0xFFB0 /* Timer Mode Register A */
#define TCA      *(volatile unsigned char *)0xFFB1 /* Timer Counter A */
#define TMC      *(volatile unsigned char *)0xFFB4 /* Timer Mode Register C */
#define TCC      *(volatile unsigned char *)0xFFB5 /* Timer Counter C */
#define TLC      *(volatile unsigned char *)0xFFB5 /* Timer Load Register C */
#define PMR3_BIT (*(struct BIT *)0xFFCA) /* Port Mode Register 3 */
#define UD        PMR3_BIT.b0 /* Port Mode Register 3 bit0 */
#define PMRB_BIT  (*(struct BIT *)0xFFEE) /* Port Mode Register B */
#define IRQ1      PMRB_BIT.b3 /* Port Mode Register B bit3 */

```

```

#define IEGR_BIT    (*(struct BIT *)0xFFF2)        /* Interrupt Edge Select Register 1 */
#define IEG1        IEGR_BIT.b1                    /* IRQ1 Edge Select */
#define IENR1_BIT   (*(struct BIT *)0xFFF3)        /* Interrupt Enable Register 1 */
#define IENTA       IENR1_BIT.b7                    /* Timer A Interrupt Enable */
#define IENR2_BIT   (*(struct BIT *)0xFFF4)        /* Interrupt Enable Register 2 */
#define IENTC       IENR2_BIT.b1                    /* Timer C Interrupt Enable */
#define IRR1_BIT    (*(struct BIT *)0xFFF6)        /* Interrupt Request Register 1 */
#define IRRTA       IRR1_BIT.b7                    /* Timer A Interrupt Request Flag */
#define IRR2_BIT    (*(struct BIT *)0xFFF7)        /* Interrupt Request Register 2 */
#define IRRTC       IRR2_BIT.b1                    /* Timer C Interrupt Request Flag */

#pragma interrupt (taint)
#pragma interrupt (tcint)
/*****/
/* Function define */
/*****/
extern void INIT ( void );                          /* SP Set */
void      main ( void );
void      taint ( void );
void      tcint ( void );

/*****/
/* RAM define */
/*****/
unsigned char cnt1;                                /* 8bit Counter */
unsigned char cnt2;                                /* 8bit Counter */
unsigned char ENDF;                                /* End Data */

/*****/
/* Vector Address */
/*****/
#pragma section V1                                  /* VECTOR SECT0IN SET */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT                                /* 00 Reset */
};
#pragma section V2                                  /* VECTOR SECT0IN SET */
void (*const VEC_TBL2[])(void) = {
    taint                                /* 16 Timer A Interrupt */
};
#pragma section V3                                  /* VECTOR SECT0IN SET */
void (*const VEC_TBL3[])(void) = {
    tcint                                /* 1A Timer C Interrupt */
};

#pragma section                                     /* P */
/*****/
/* Main Program */
/*****/
void main ( void )
{
    set_imask_ccr(1);                        /* Interrupt Disable */

    IRQ1 = 1;                                /* TMIC Input Select */
    UD   = 1;                                /* UD Input Select */

    cnt1 = 0;                                /* Initialize 8bit Counter */

```

```

cnt2 = 0;                                /* Initialize 8bit Counter */
ENDF = 0;                                /* Clear END Flag */

IEG1 = 1;                                /* TMIC Select */
IRRTC = 0;                               /* Clear IRRTC */
IRRTA = 0;                               /* Clear IRRTC */

TMC = 0x7F;                             /* Initialize 8bit Event Counter Function */
TMA = 0x1F;                             /* Initialize Timer Counter A */
TLC = 0x00;                             /* Clear TCC */
TMA = 0x18;                             /* Initialize Clock Time Base Function */

IENTC = 1;                              /* Timer C Interrupt Enable */
IENTA = 1;                              /* Timer A Interrupt Enable */

set_imask_ccr(0);                        /* Interrupt Enable */

while (ENDF==0);

TMC = 0;                                /* Initialize Timer C Function */

while (1) {
    ;
}

/*****/
/* Timer A Interrupt */
/*****/
void taint ( void )
{
    IRRTA = 0;                           /* Clear IRRTA */

    cnt2 = TCC;                          /* Store TCC */

    IENTC = 0;                           /* Timer C Interrupt Disable */
    IENTA = 0;                           /* Timer A Interrupt Disable */

    ENDF = 1;                            /* Set ENDF */
}

/*****/
/* Timer C Interrupt */
/*****/
void tcint ( void )
{
    IRRTC = 0;                           /* Clear IRRTC */

    if ( cnt1 == 0xff ) {                /* 8bit Counter = 0xff? */
        cnt1 = 0;                        /* Clear cnt1 */
        cnt2 = 0;                        /* Clear cnt2 */
        ENDF = 1;                        /* ENDF */
        IENTA = 0;                       /* Timer A Interrupt Disable */
    }
    else {
        cnt1++;                          /* cnt1 Increment */
    }
}

```

```
}  
}
```

连接地址的指定

段名	地址
CV1	H'0000
CV2	H'0016
CV3	H'001A
P	H'0100
B	H'FB80

修订记录

Rev.	发行日	修订内容	
		页	修订要点
1.00	2005.09.14	—	初版发行

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