A/D Range Control Using the ISL5416 3G QPDC

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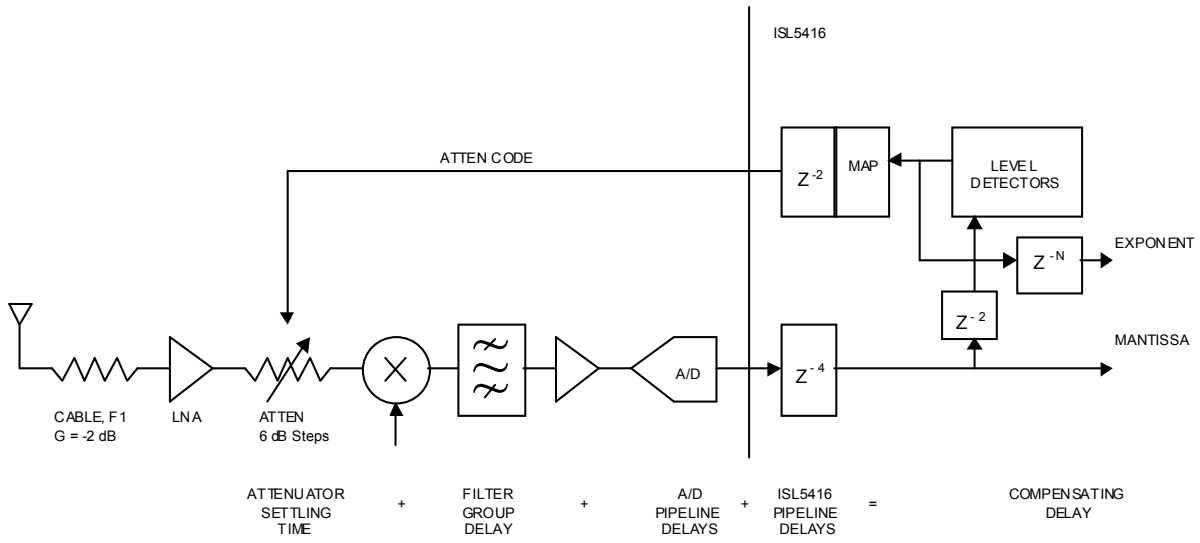
Overview:

The ISL5416 has a range control circuit that monitors the samples from the A/D and adjusts the RF/IF gain to optimize receiver sensitivity. The circuit reduces gain when large signals are present to prevent A/D saturation and increases gain to maximize sensitivity when no large signals are present. This shifts the instantaneous dynamic range of the A/D up and down within the total receiver range set by A/D dynamic range plus the RF/IF attenuation. The RF/IF attenuation controlled by the range control circuit can be thought of as the exponent portion of a floating-point digitizer and the A/D output thought of as the mantissa. The ISL5416 requires that the gain adjustments be in 6 dB increments though in general, floating-point digitizers can use any exponent step size. The DSP processing in the ISL5416 adds 6 dB of gain to the A/D output (mantissa) for each 6 dB of RF/IF attenuation step. This converts the floating-point samples to fixed point for processing. The overall gain is constant through the RF, A/D, and DSP front end. A simplified block diagram is provided in figure 1.

Figure 2 illustrates what happens to the signal at various points from the RF to through the DSP front end. As the RF signal level increases, the signal envelope at the A/D output crosses a threshold and the range control circuit increases the RF attenuation to reduce the signal level at the A/D input. Whenever the RF attenuation is increased, the DSP gain is increased to compensate and maintain a constant overall gain from the RF through the DSP front end. The attenuation and gain controls signals are in offset in time to compensate for the delays from the RF through the A/D and DSP.

Figure 3 illustrates how the instantaneous dynamic range of the A/D maps to the RF signal range. As attenuation is added, the full scale at the A/D corresponds to a larger RF signal power. The added attenuation, however, also raises the A/D noise floor relative to the RF input and reduces sensitivity.



NOTE: The compensating delay, Z^{-N}, is chosen as close as possible to the sum of the settling time, group delay, and pipeline delays. This minimizes the transient due to an attenuation change. The delay is programmable from 1 to 256 clock periods (12 ns to 3.2 us at 80 MSPS).

FIGURE 1. TYPICAL SYSTEM CONFIGURATION, INCLUDING SIGNAL DELAYS

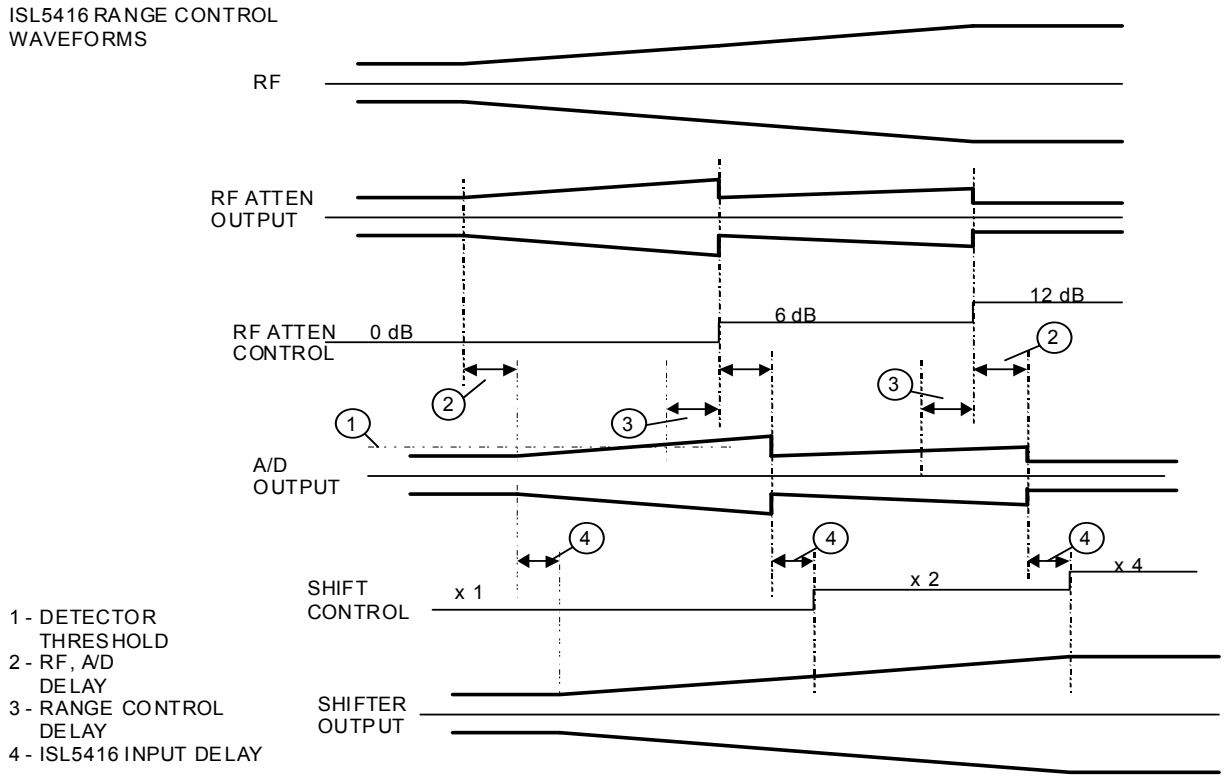


FIGURE 2. ISL5416 RANGE CONTROL WAVE FORMS

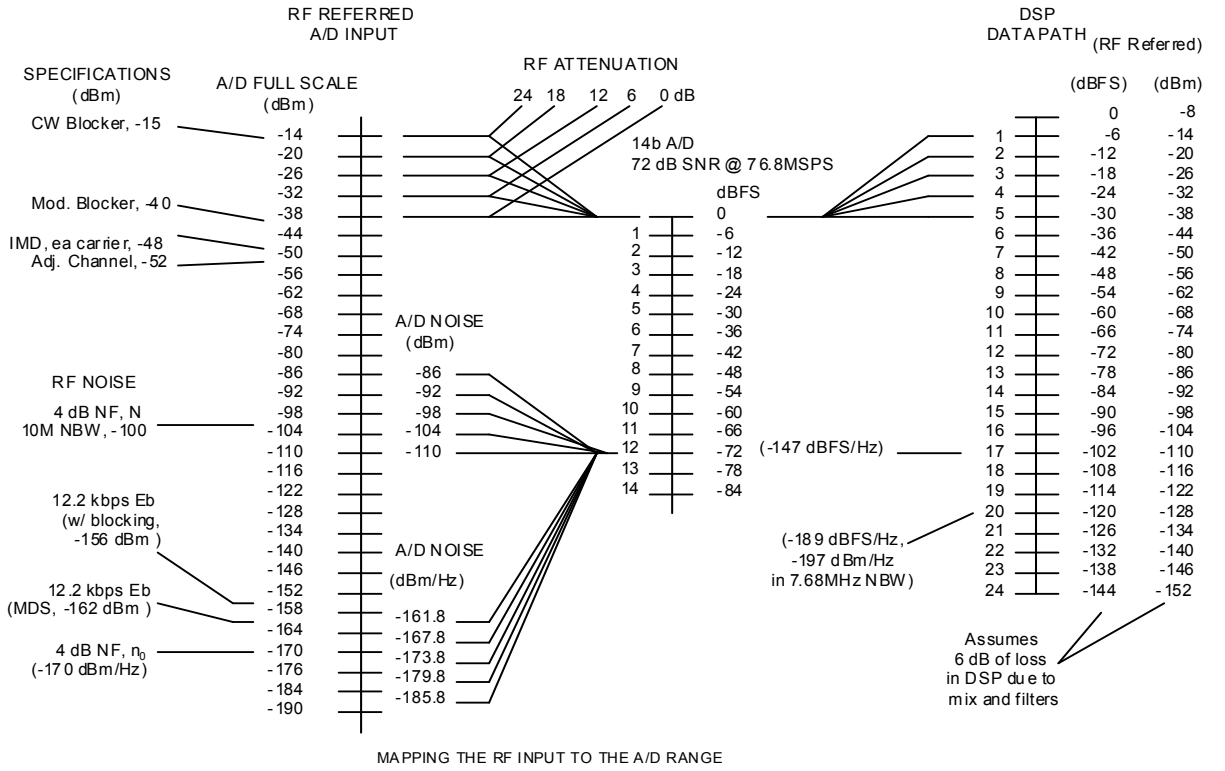


FIGURE 3. MAPPING THE RF INPUT TO THE A/D RANGE

The ISL5416 Range Control Operation Description

Figure 4 is a simplified system block diagram of the ISL5416 range control circuitry. The input samples from the A/D are monitored with a set of filters and level detectors. The level detector decisions control whether to increase or decrease the contents of an accumulator that holds an RF/IF attenuation word. Only the MSBs of the accumulator are mapped to the attenuation control bits, so by programming the accumulator changes to be below these MSBs, the accumulator can act as a filter on the detector outputs. Programmable upper and lower limits restrict the accumulator to only the attenuation range that is needed.

There are two signal paths for the samples from the A/D converter. In one path, the absolute value of each sample is compared to a programmable threshold. In the other path, the samples are averaged before making a decision. In the sample-by-sample path, if any sample exceeds the threshold, the RF/IF attenuation is immediately increased. The purpose of this detector is to prevent saturation of the A/D converter due a rapid increase in input power, and this detector is given the highest priority. The threshold for this detector is usually set within a few dB of the A/D full scale and the gain adjustment from an immediate threshold crossing usually set to 6.02 dB. After an immediate threshold crossing, the immediate detector is disabled for a programmable number of samples to allow the loop to settle before making another adjustment.

The other signal path filters the A/D samples before making decisions. The samples are first high-pass filtered to block DC offsets from the A/D converter. The absolute values of the samples are then averaged in an integrate-and-dump circuit. The integration period is programmable from 2 to 65536 samples. Averaging reduces the standard deviation of the samples for a better decision and is a necessity for a lower limit comparison since the A/D samples pass through zero. The integrator output is divided by 2^N in a barrel shifter to compensate for growth in the integrator and reduce the range of the data to the detectors. The average magnitude is next compared against upper and lower thresholds. In the averaged signal path, threshold decisions are only made at the end of the integration period. If the upper threshold is exceeded, the attenuation control accumulator is increased by a programmable amount. If the average falls below the lower threshold, the accumulator is decreased by a separate programmable amount. These average signal thresholds set the desired operating limits for the signal to the A/D. The upper limit is typically set based on the peak-to-average ratio of the expected input signals with sufficient back off to prevent tripping the immediate threshold. The lower limit is set to guarantee a minimum SNR from the RF and/or a minimum number of effective bits from of the A/D converter. When the signal falls below this threshold, attenuation is removed to lower the RF noise figure and to increase the signal to the A/D so that more bits toggle.

If the average magnitude is between the upper and lower averaged limits, at the end of the integration period a programmable bias value is added to the attenuation control accumulator. This bias slowly adds or removes attenuation to bias the signal toward one end of the operating range. This bias overcomes the large hysteresis that results when there is a large separation between the upper and lower thresholds. For small separations between the upper and lower thresholds, the bias can be disabled.

The three MSBs of the attenuation control accumulator represent the attenuation value from 0 to 42 dB in 6 dB steps. These three bits are routed to the tuner channels that receive the input samples and control the amount of additional gain that is added by a barrel shifter that precedes the CIC filter. The gain is added at the CIC to maximize the dynamic range through the NCO/mixer stage. The three gain control bits are delayed by a programmable delay stage to compensate for the delays in the RF/IF/DSP due to attenuator settling time, filter group delays, and A/D and DSP pipeline delays and align the CIC shifter gain changes with the RF changes. The delay is programmable from 1 to 256 clock periods, providing up to 2.56 usec at 100 MSPS.

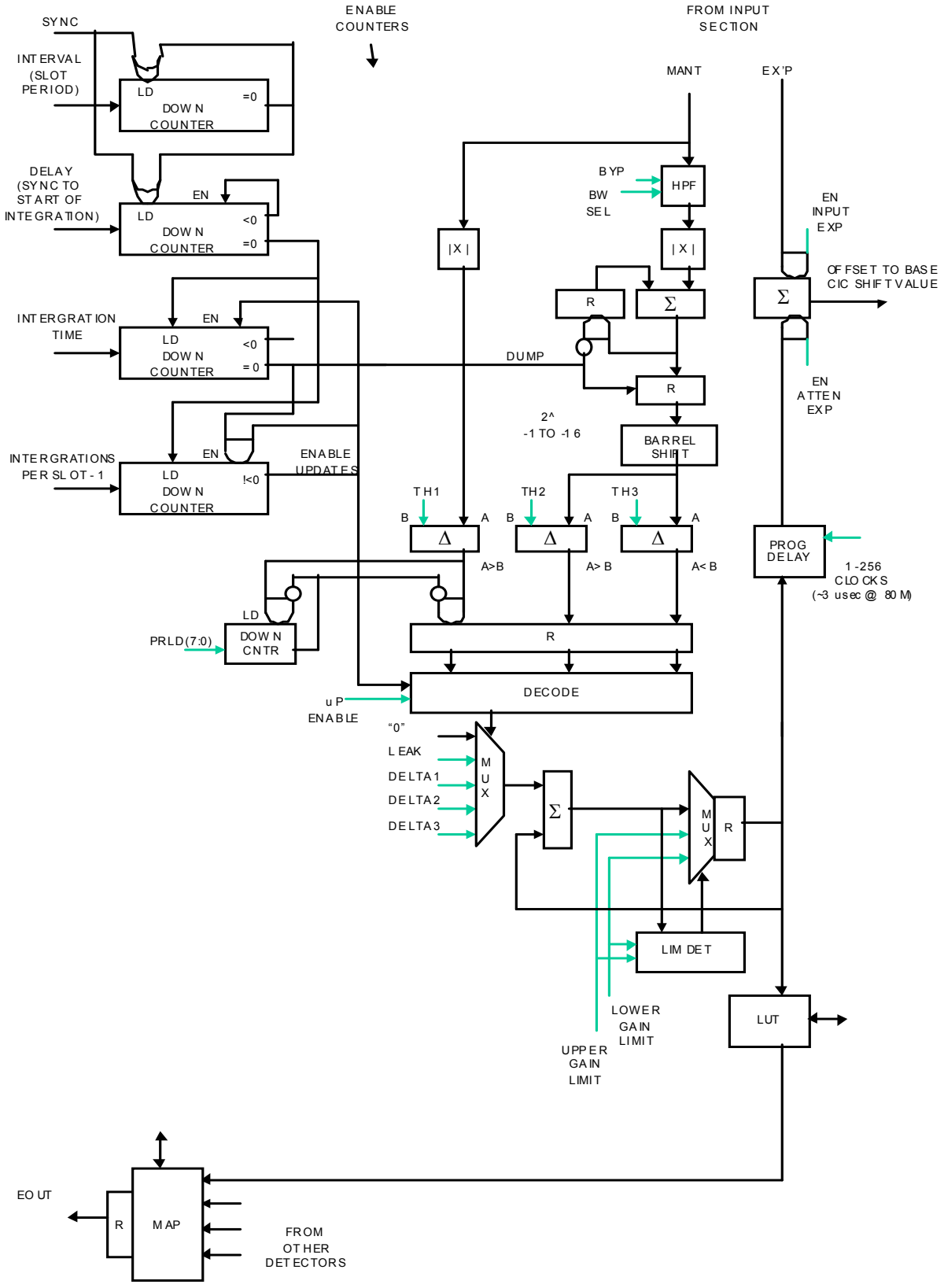


FIGURE 4. RANGE CONTROL BLOCK DIAGRAM

To simplify the interface to attenuators from different manufacturers, the three-bit attenuation control addresses an 8-location look-up table with 8 bits per location. Each location corresponds to one of the attenuation steps and up to 8 bits can be used to control the attenuation at each step. If the attenuator has finer resolution than 6 dB, the extra bits and attenuation steps can be used for calibrating the RF/IF gains with different codes loaded in the look-up tables for each input bus to equalize the gains to each A/D.

The 16-bit EOUT bus is the attenuation control bus. It updates at the CLKC rate. The mapping of range control channel to EOUT bits is programmable in four bit groups so that either four range control channels with four bits per channel or two channels with eight bits per channel can be used.

There is a set of four counters that control the range control updates in the averaged data path. The sample-by-sample data path operation is independent of the counters. Figure 5 illustrates the counter operation. The timing is based on a slot period and which can be aligned to system timing events such as TDM slots or can free run asynchronous to the system timing. Within the slot there can be one or more integration periods for the averaged data path described above. The integration periods shifted around within the slots and across slot boundaries using a delay counter. The delay compensates for TX/RX offsets and/or RF/IF group delay. An integration time counter sets the length of each integration period. An integration period counter counts the number of integration periods per slot. The slot counter sets the overall time interval from 1 to 65536 input clock or sample periods. The slot counter restarts when it finishes its count but can also be restarted by a SyncIn signal to align it to the system timing. The delay counter is loaded at the same time as the slot counter. The first integration period begins when the delay counter reaches the end of its count.

The control microprocessor can load the attenuation control accumulator to initialize it or to manually control the attenuators. So that it can monitor the operation of the range control circuit, the processor can read the range control accumulator, read the DC offset value blocked by the high pass filter, and read the normalized averaged magnitude.

Test Data

Test data from two lab configurations is presented below. The first case used all digital components. The second case added a D/A, an A/D, and analog filters and replaced a digital barrel shifter with an analog attenuator with digital controls.

Case 1: All-Digital Test Configuration

Figure 6 shows the configuration for this test. A multi-channel digital up converter evaluation board, the ISL5217EVAL was used to filter, interpolate, and modulate a digital pattern to a sampled IF. The digital output of the evaluation board was then routed through an FPGA prototyping board with the FPGA programmed as a barrel shifter. The barrel shifter included saturation logic to prevent wraparound in the event of overflow. The output of the barrel shifter was connected to the input bus of an ISL5416 evaluation board. Pins from the EOUT bus were connected to the barrel shifter controls to close the range control loop. D/A converters on each board allowed monitoring of the important signals.

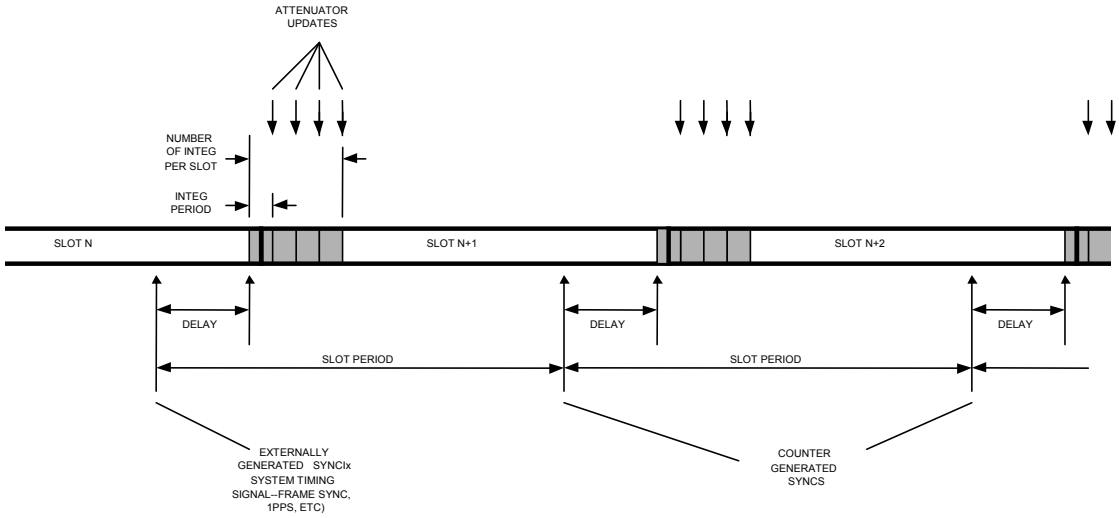
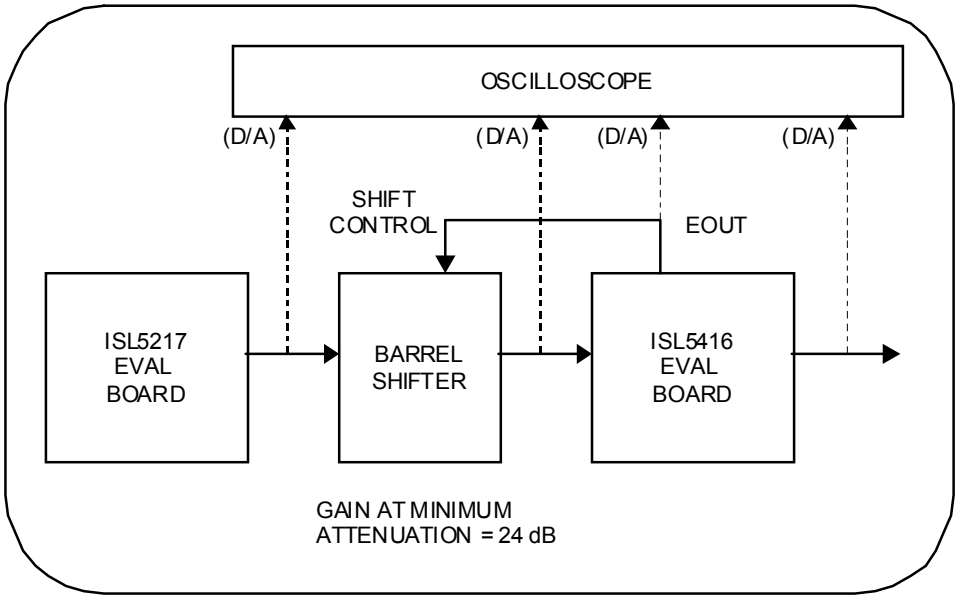


FIGURE 5. RANGE CONTROL TIMER OPERATION



NOTE: Connections between the evaluation boards are 16-bit digital. D/A converters on the boards and a 4-channel digital oscilloscope are used for monitoring and data collection.

FIGURE 6. TEST CONFIGURATION 1

Two channels of the digital up converter were used. One channel generated a CW signal at 8.5 MHz. The other channel filtered and modulated a square wave baseband pattern onto an 11 MHz carrier. A Gaussian filter was used to produce rapid envelope changes while limiting the width of the spectrum. The AM modulation depth was 77 dB from 48 dB above to 29 dB below the CW carrier. Hard-wired gain in the barrel shifter put the modulated signal range from +18 dBFS to -59 dBFS at the input to the ISL5416 at the minimum attenuation setting. Figure 7A shows the signal levels and gain distribution. Appendix 1 provides more details on the configuration and gain distribution.

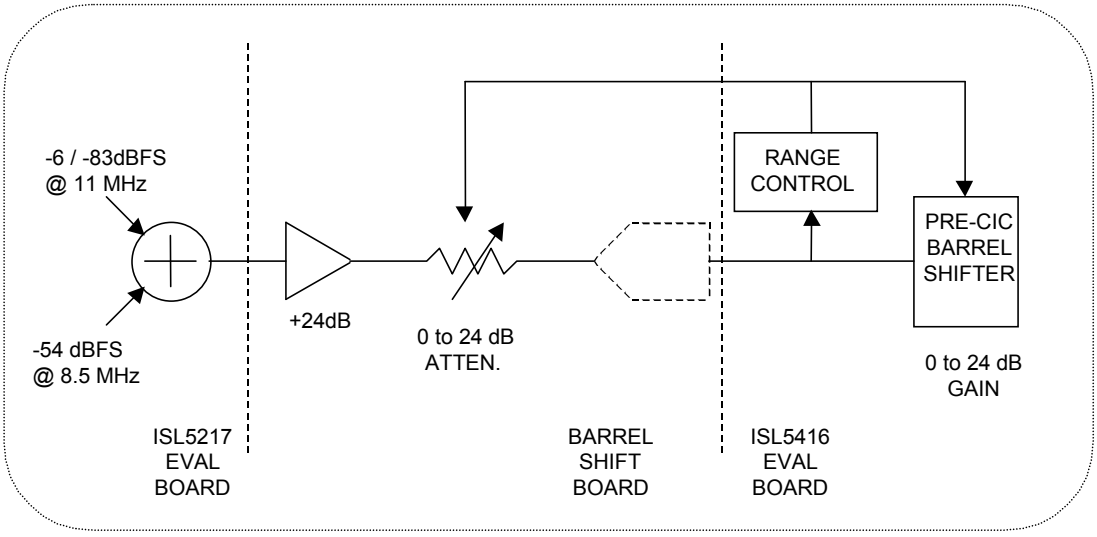
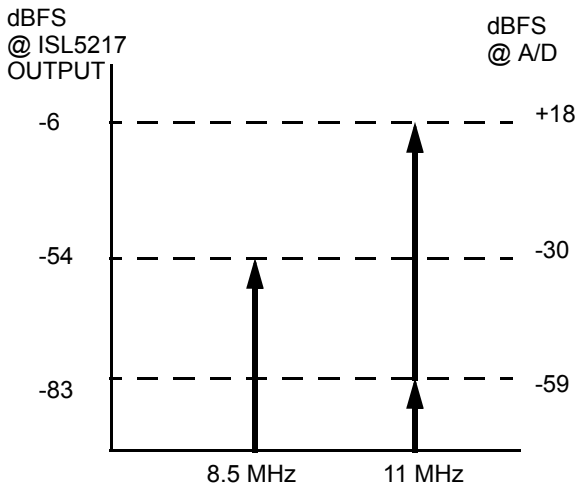


FIGURE 7A. TEST CONFIGURATION 1 GAIN DISTRIBUTION



NOTE: The desired signal is at 8.5M and the AM Modulated Interferer is at 11.5M

FIGURE 7B. TEST CONFIGURATION 1 SIGNAL LEVELS

Figures 8A and 8B show the waveforms at the rising and falling edges of the square wave, respectively. In both cases, the digital oscilloscope samples at approximately 6 times the input clock rate and the ISL5416 output sample rate was 1/8 the clock rate. In figure 7A, as the signal ramps up, it crosses the immediate threshold and triggers a 6 dB increase in attenuation. The hold-off counter prevents additional immediate threshold triggers while the gain change propagates through the pipeline delays in the 5416 and barrel shifter (a total of 12 clocks). During this delay, the signal ramps fast enough that the shifter output saturates briefly. When the hold off counter times out, the immediate threshold triggers again, increasing the attenuation to 12 dB. The signal slew rate decreases, but still triggers another attenuation increase to 18 dB. The signal settles to its final value below the immediate threshold, but above the upper threshold of -15 dBFS. After 6 integration periods at 1 dB attenuation increase per period, the attenuation control accumulator reaches its next 6 dB step and the shifter output is reduced below the upper threshold and holds at 24 dB of attenuation. Note that the brief period of input saturation caused a short period of signal suppression at the output of the 5416.

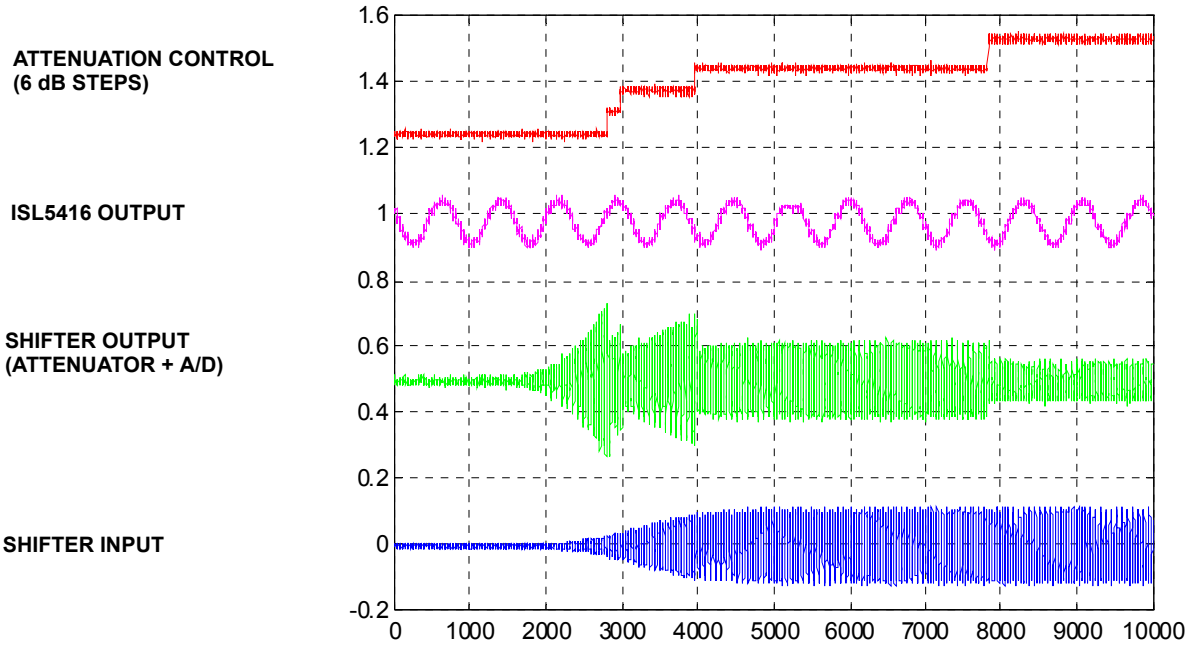


FIGURE 8A. ARRIVAL OF INTERFERING SIGNAL

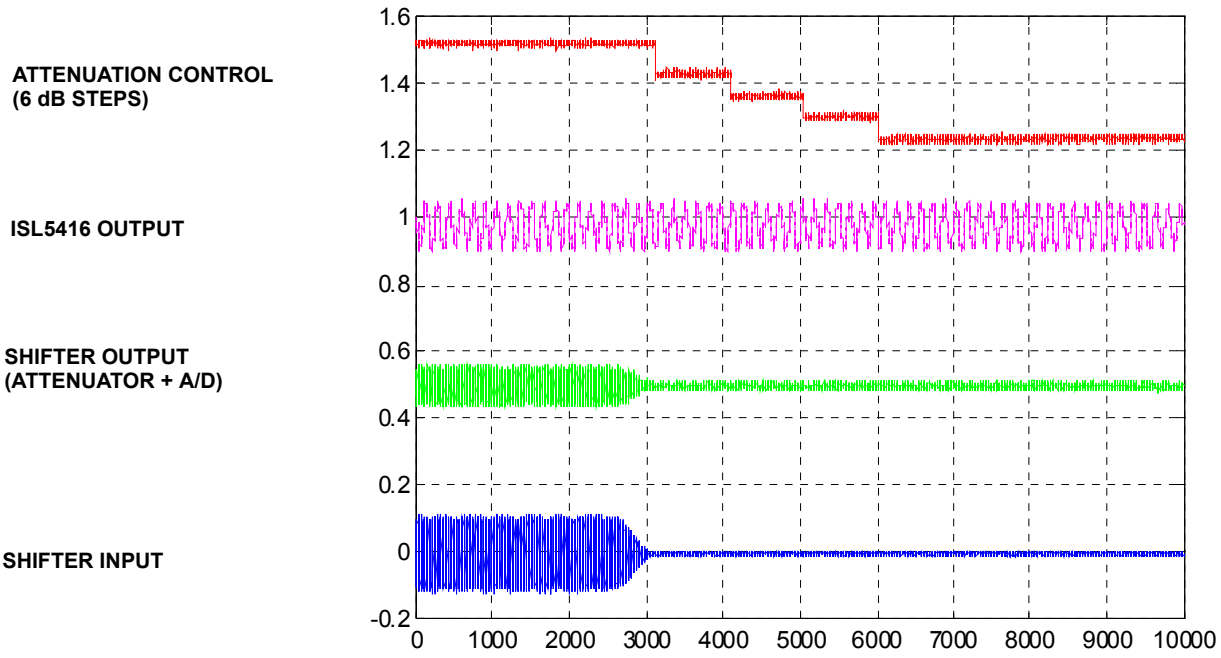


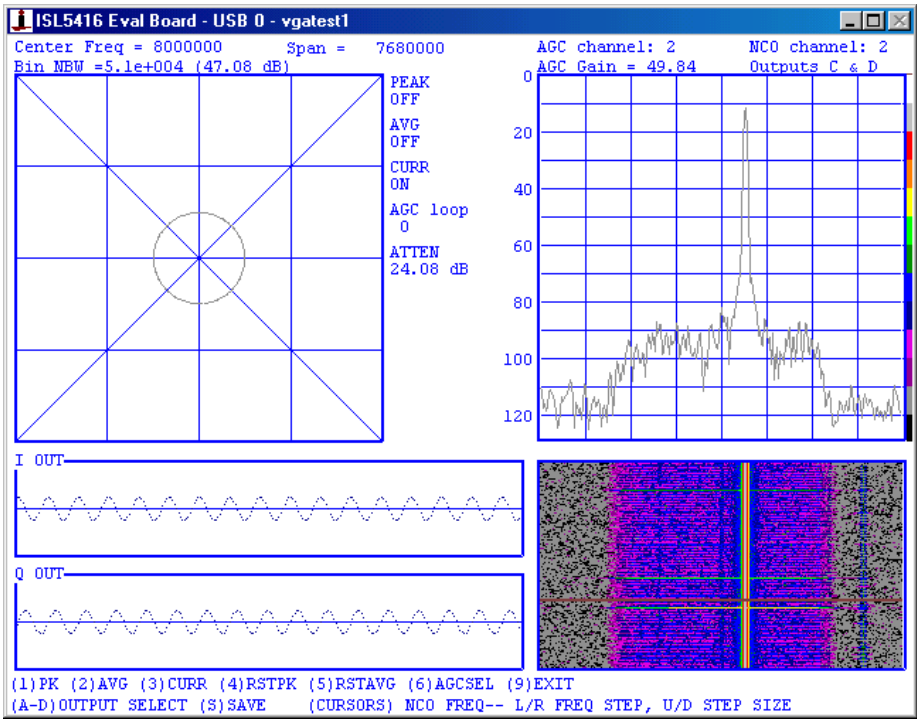
FIGURE 8B. DEPARTURE OF INTERFERING SIGNAL

When the signal falls below the lower threshold, the attenuation control accumulator starts to ramp down. Eventually it reaches minimum attenuation. The number of significant bits at the shifter output (A/Din a real system) increases as the attenuation decreases.

Figure 8B shows the falling edge of the modulated signal. In this case, only the lower threshold has an effect and the attenuation is removed in 6 dB steps until the attenuation is once again 0 dB. When the signal falls below the lower threshold, the attenuation control accumulator starts to ramp down. Eventually it reaches minimum attenuation. The number of significant bits at the shifter output (A/D in a real system) increases as the attenuation decreases.

Figures 9A and 9B show the ISL5416 evaluation board software display screen for the minimum and maximum attenuation cases, respectively. Note that the attenuation shown on the screen is not accurate because the output samples and range control attenuation are retrieved from the board in two accesses and the gain is changing faster than the access rate over the USB bus. Note the increase in the noise floor when the attenuation is added. This is because the signal of interest has been attenuated 24 dB toward the quantization noise floor at the input to the ISL5416. The CIC barrel shifter compensated for the loss, so the AGC gain did not changed. The output SNR, however, has dropped as the full-scale input range ISL5416 has increased 24 dB.

Note that the decrease in SNR is not quite 24 dB. This is because at minimum attenuation, the signal is backed off 24 dB at the CIC barrel shifter and the input noise floor is attenuated below the 20-bit quantization noise floor in the data path. At maximum attenuation, there is no back off at the barrel shifter and the input quantization noise of approximately -172 dBFS/Hz dominates. The combination of a 16-bit input width at 61.44 MSPS and a 24 dB attenuation range constitutes a 20-bit floating point A/D system with a -197 dBFS/Hz theoretical noise floor. This is lower than the internal 20-bit noise floor in the data path when the sample rate has been lowered to 7.68MSPS by decimation.



NOTE: in both figures, the reported attenuation level does not align with the FFT display due to the delay over the USB

FIGURE 9A. INTERFERING SIGNAL AT MINIMUM LEVEL (MINIMUM ATTENUATION)

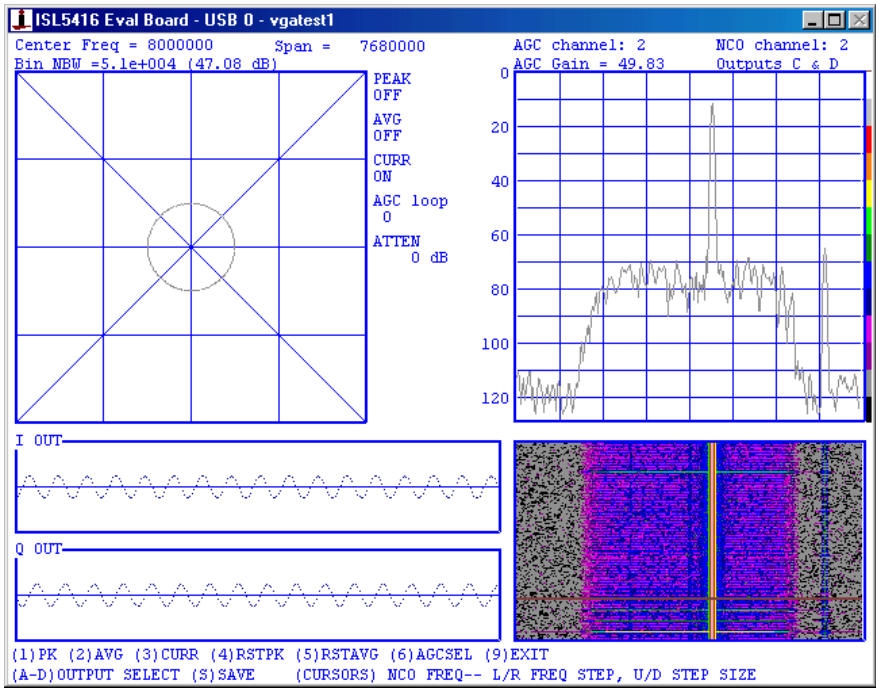


FIGURE 9B. INTERFERING SIGNAL AT MAXIMUM LEVEL (MAXIMUM ATTENUATION)

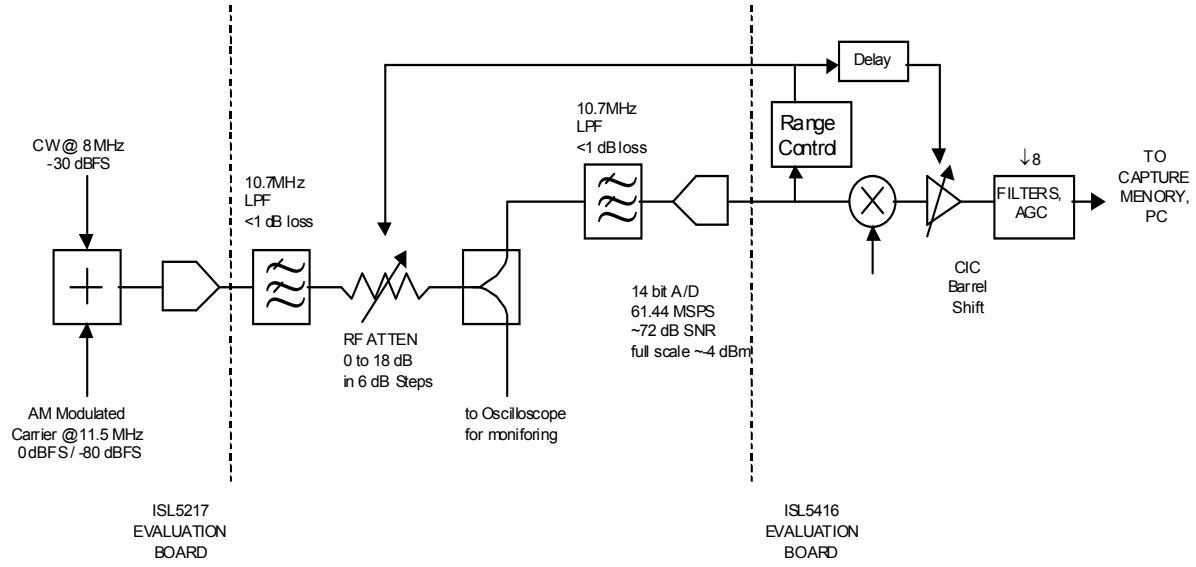


FIGURE 10. TEST CONFIGURATION 2

Case 2: Real World Components

This example replaces the digital attenuator (barrel shifter) with a D/A, A/D, digitally controlled attenuator, and low-pass filters. A block diagram for this test configuration is shown in figure 10. Because the D/A converter output does not reach the full-scale input voltage of the A/D, for these tests, the range control thresholds were reduced by 15 dB from case 1 to -19, -30, and -45 dBFS for the immediate, upper, and lower thresholds, respectively. The ISL5217 signal levels were increased to -30 dBFS and to -0.2/-80 dBFS for the signal of interest and the interferer, respectively. Appendix 2 provides more details on the settings and gain distribution for the configuration.

Figures 10A and 10B shows the I output of the ISL5416 at the arrival and departure of the interfering signal. Figures 11A and 11B shows the log of the magnitude of the ISL5416 I/Q output. The discontinuities in the display result occur at the switching points between attenuation settings. These can be caused by the attenuator not switching cleanly between steps and/or the gain discontinuity from the attenuation switching exciting the low-pass filters and spreading the attenuation change over the impulse response length of the filters. The range control RF delay is programmed to the approximate center of the filter group delay and converter delay, but the gain change at the filter output is not instantaneous and starts before and settles after the CIC barrel shift change. In a direct sequence spread spectrum system, the de-spreading process will reduce the effects of the discontinuities. In non-spread systems, aligning the range control timing to time slot boundaries may minimize the effects of discontinuities. This illustrates why it is important to minimize the number of gain changes by proper selection of the thresholds and gain steps. An attenuator at IF rather than RF can also minimize the discontinuities by reducing filter effects but this requires RF and IF components with higher compression points. The change in SNR with the change in attenuation can also be seen in the figures.

Figure 11B shows the AGC settling after the attenuator changes to compensate for the attenuator inaccuracy. The attenuator steps are not exactly 6 dB. In this example the error is about 0.25 - 0.5 dB. This is the overall non-linearity of the floating-point A/D system. The A/D converter sets the instantaneous non-linearity of the system, but the attenuator dominates the non-linearity of the system. If the attenuator adjusted every sample, the performance would be roughly equal to a 5 bit A/D.

Figures 12A and 12B are FFTs of the ISL5416 output at minimum and maximum attenuation. The sample rate is 7.68 MHz and the bin NBW is approximately 12.75 kHz (41 dB). From the displays, the C/No can be estimated to be

104 dB/Hz and 89 dB/Hz for 0 dB and 18 dB of attenuation, respectively. The spurs that appear when there is 18 dB of attenuation are approximately -93 dBFS at the A/D input and may be caused by signal leakage in the test fixture at the higher attenuation setting.

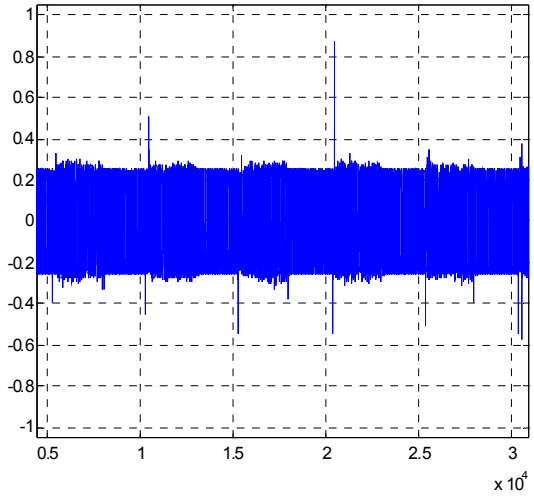


FIGURE 10A.

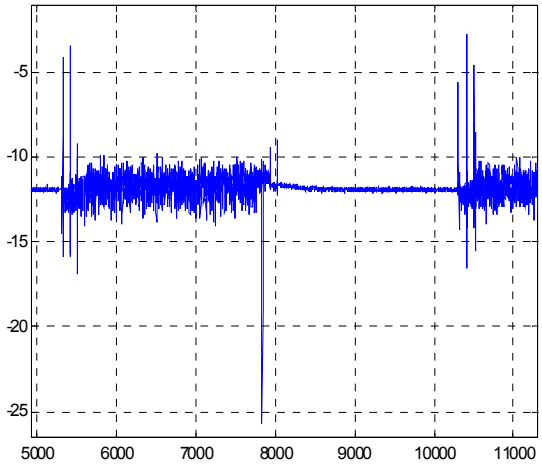


FIGURE 11A.

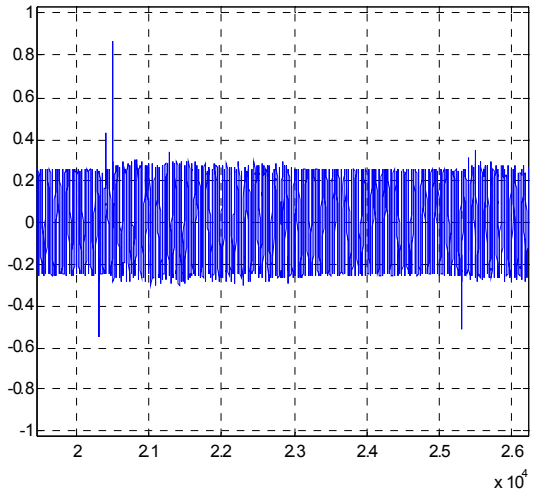


FIGURE 10B.

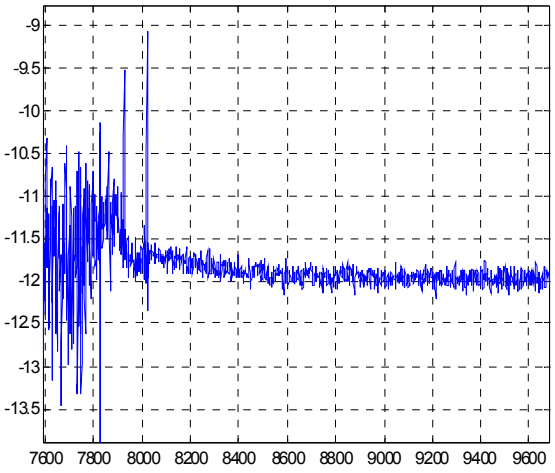


FIGURE 11B.

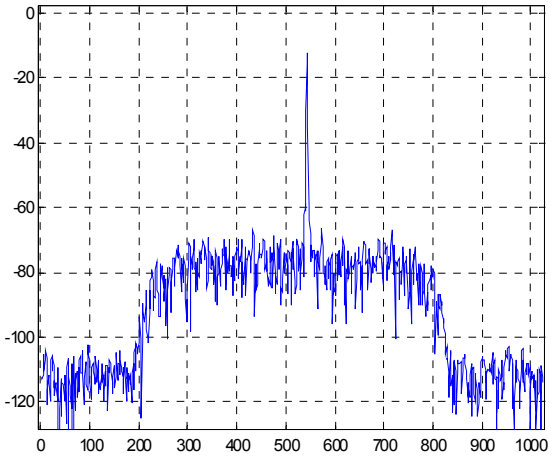


FIGURE 12A. ISL5416 OUTPUT, 1K POINT FFT, BLACKMAN WINDOW, ~1.7 BIN NBW/BIN SPACING FACTOR (0 dB ATTENUATION)

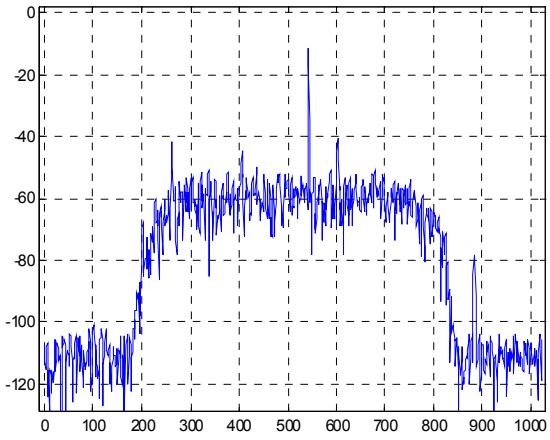


FIGURE 12B. ISL5416 OUTPUT, 1K POINT FFT, BLACKMAN WINDOW, ~1.7 BIN NBW/BIN SPACING FACTOR (18 dB ATTENUATION)

Figures 13A and 13B show the evaluation software screens at minimum and maximum attenuation. The FFT display is 256 points and the noise bandwidth of an FFT bin is shown at the upper left corner of the display. The signal of interest is -47 dBFS into the A/D converter with minimum attenuation and -65 dBFS at maximum attenuation. The converter noise floor is approximately 72 dB at 61.44MSPS or -122 dBFS per FFT bin at the A/D input. At minimum attenuation the output SNR is approximately 31 dB. At maximum attenuation it is reduced to about 16 dB. The AGC gain drops by 0.8 dB due to the attenuator inaccuracy and the extra noise in the output bandwidth.

The waterfall display shows the spectral noise floor occasionally jumps. This occurs when the samples used by the FFT include discontinuities from the attenuation change.

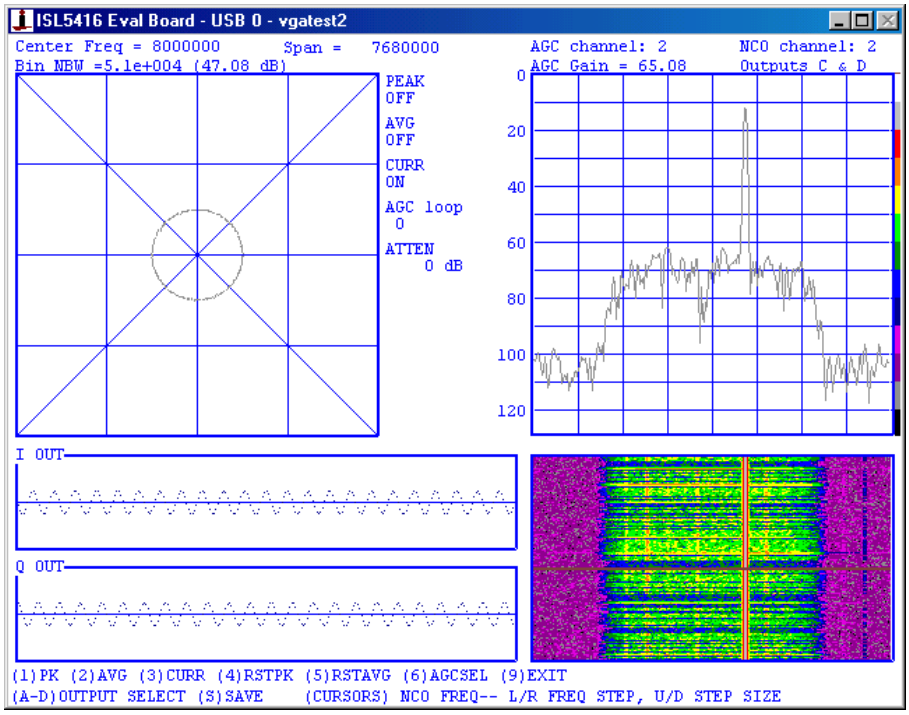
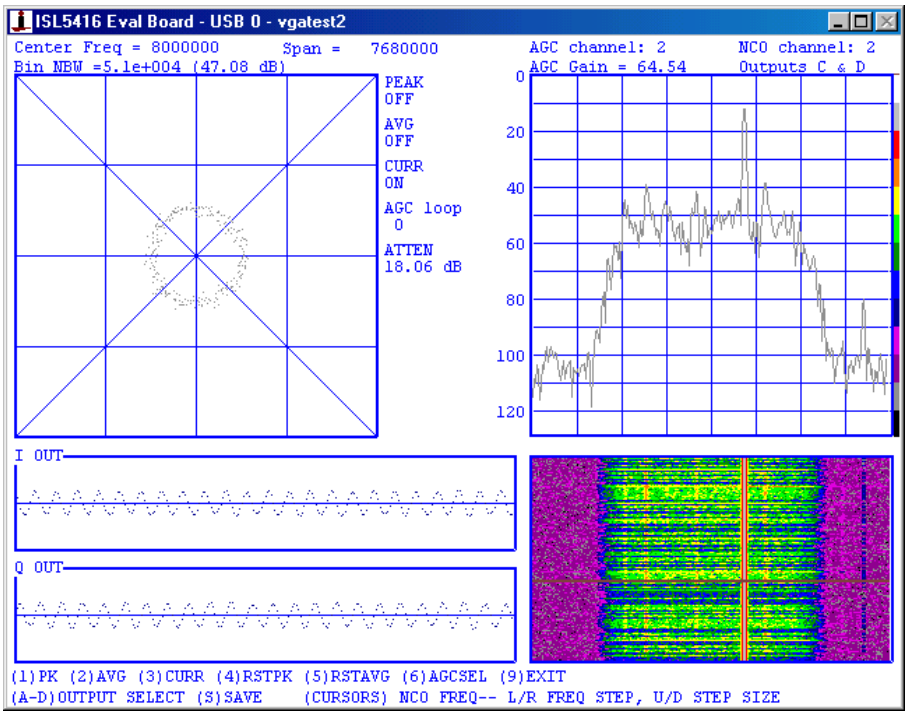


FIGURE 13A. EVALUATION BOARD SOFTWARE SCREEN (0 dB ATTENUATION)



NOTE: It is not shown by the screens that the A/D has a DC offset of -30 dBFS. The high-pass filter blocks the DC component in the averaged path. Without the high pass filter, the lower limit would never be reached and the attenuation would stay at 18 dB after the first time the interfering signal arrived (the leak term is disable in this example).

FIGURE 13B. EVALUATION BOARD SOFTWARE SCREEN (18 dB ATTENUATION)

Miscellaneous Notes on Usage and Applicatoins

Detector Use Strategies

A number of different range-control strategies are possible depending on which detectors are enabled.

1. All thresholds and the bias enabled. This mode gives the most control over the operating range and can most quickly settle to that range.
2. Only the immediate threshold and the bias are enabled. This mode takes the A/D out of saturation quickly and slowly removes attenuation using the bias until it is all removed or the immediate threshold triggers again. This mode can have the fewest attenuator adjustments, minimizing the number of discontinuities in the A/D output. This mode can also have long periods of low sensitivity while attenuation is slowly removed by the bias after the large signal that triggered the immediate threshold goes away.
3. Use only the immediate threshold and lower threshold. This mode takes the A/D out of saturation quickly and can remove attenuation when it is no longer needed more rapidly than case 2.

Threshold Setting and Disabling Detectors

The thresholds and bias can be disabled as follows:

1. Immediate threshold: set the threshold to full scale, (0 dBFS)
2. Upper threshold: set the threshold to full scale (0 dBFS)
3. Lower threshold: set the threshold to its minimum value
4. Bias: set the bias increment to zero.

The immediate threshold is usually set a few dB from full scale. If the input is expected to increase rapidly and there is a large delay from the attenuator to the A/D output, the threshold may need to be lower to reduce the time in saturation due to the delay.

The upper threshold is set based on the peak-to-average ratio of the interfering signal. For example, with noise-like signals the threshold might be set to so that A/D saturation occurs at the four standard deviations from the RMS signal. Note that the detectors operate on the average and the average magnitude of a Gaussian random variable is about 2 dB below the standard deviation. If the interfering signal is a sinusoid, the threshold might be set so that the peaks are below the immediate threshold. The RMS-to-average ratio for a sinusoid is usually around 1.11 (0.91 dB), but there are special cases at

Fs/4 and close to DC or Fs/2. At DC or Fs/2, the period of the sinusoid can be longer than the integration period for the detector. At Fs/4 the average can vary from 0.5 to 0.7071 depending on the phase.

The lower threshold is always set above the noise floor of the A/D. When the signal level drops, the lower threshold detector is used to quickly remove attenuation. This lowers the A/D noise floor relative to the RF noise floor and increases the receiver sensitivity. To quickly restore maximum sensitivity, the lower threshold should be set high, close to the upper threshold. The lower threshold can be set farther below the upper threshold to provide hysteresis in the loop.

The bias value sets the maximum time that the receiver sensitivity is reduced due to unneeded attenuation. A large bias step value will remove attenuation move quickly.

Figures 14 illustrate how the thresholds move relative to the RF power as attenuation changes. Figure 15 illustrates choosing thresholds values.

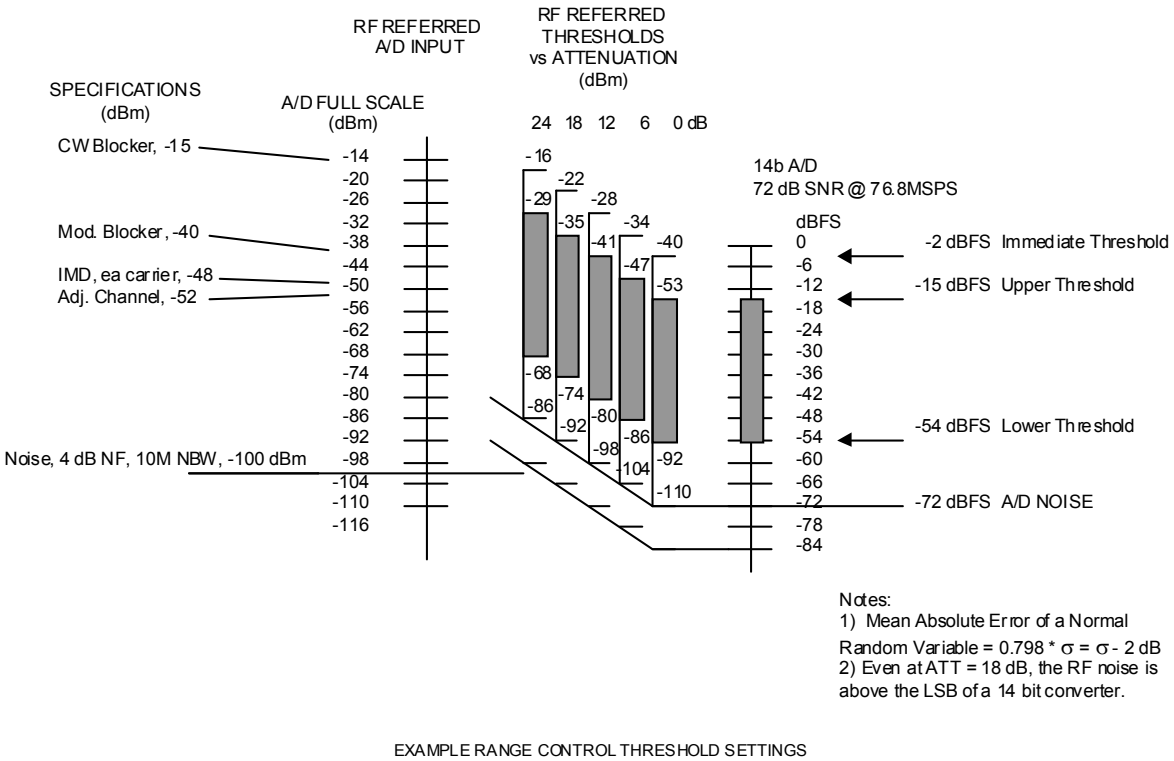
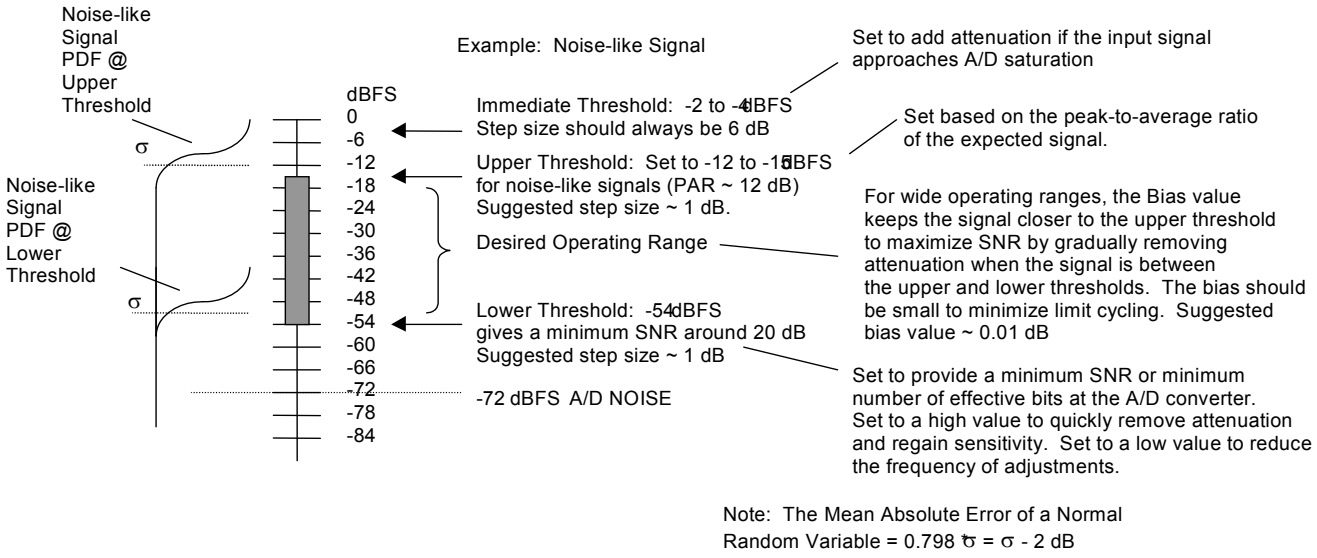


FIGURE 14. THRESHOLD MAPPING



•Integration Time: chosen to be long enough to reduce the standard deviation of the threshold comparison:

$\sigma' = \sigma / \mathrm{SQRT}(N)$, and to be short enough to react to the departure of a large signal.

•

The slot period must be longer than the integration time.

•

•Integrations/slot: integration time x integrations / slot must be less than the slot period

FIGURE 15. CHOOSING THRESHOLD VALUES

Attenuator Location

Positioning an RF attenuator before the LNA will impact the receiver noise figure nearly dB for dB as attenuation is added. Putting it after the LNA has less effect on the noise figure but allows the LNA to be overloaded. Using two attenuators-one prior to and one following the LNA can be a good compromise. Equal attenuation can be added at both points or attenuation can be first added after the LNA and only added ahead of the LNA at maximum attenuation when there is the LNA approaches compression.

System Calibration

An attenuator with gain steps smaller than 6 dB together with the extra bits in the range control look-up table can be used during system calibration to equalize the gain between receive channels. The AGC in the ISL5416 can also assist by accurately measure the difference in signal power between channels. After the gain difference between channels is measured, each look-up table can be programmed with a different set of codes to compensate.

Attenuator Options and Vendors

The choice of attenuator will on the specific application, but two sources for digital RF attenuators are M/A-COM (AT90 series GaAs FET attenuators) and Honeywell Solid State Electronic Center (HRF-AT4000 series SOI CMOS). A multiplying D/A converter may suffice at IF. A D/A converter controlling a variable-gain amplifier is another possible solution. The D/A converter would be clocked with the same clock as CLKC.

Transient Effects

In choosing components, the following will have an effect on the range control loop and should be considered.

1. **Filters**: The group delay of the filters between the attenuator and the A/D will increase the response time of the loop. The step response of the filter will show up at every attenuator change and will lengthen the gain transient seen by the A/D converter. Typically, the lower the shape factor of the filter, the longer the delay.
2. **Attenuators**: The attenuator accuracy will dominate the overall linearity of the receiver. The AGC can compensate for the error between steps, but if the AGC is used for signal power measurements, the attenuation value at each step may need to be measured at system calibration so that errors can be removed in the post processing. The attenuator settling time should be short to minimize delay in the loop, but remember that the high frequency components of fast edges can cause other problems in the receiver.
3. **A/D converters**: The pipeline delay of the A/D and the recovery time from an input step or over-range condition should be considered.

Appendices

Appendix 1 provides details on the all-digital test configuration.

Appendix 2 provides details on the test configuration using analog components.

Appendix 3 shows an example receive chain with example spreadsheet calculations for noise floor, minimum detectable signal (MDS), and output SNR for some 3GPP signal specifications.

Appendix 4 reviews the 3GPP FDD basestation receiver specifications and derives the dynamic range requirements for the A/D and DSP.

Appendix 5 is an example calculation of the digital noise contribution to the system noise.

Appendix 6 shows the relative bit weights in the range control data path.

Appendix 1

Test Configuration 1: (all digital)

Tx Configuration - ISL5217

- 61.44MHz clock
- Two transmit channels
- Main channel, CW, 8.5MHz center frequency, output level -54 dBFS
- Interferer, AM modulation, 11MHz carrier, input alternates between (0.7071, 0.7071) and (0.0001, 0.0001), 80 samples of each at a 240ksps rate
- Gaussian transmit shaping filter BT = 0.3
- Output attenuation of 6 dB
- Signal alternates between ~-6 dBFS and -83 dBFS (+48 to -29 dBc)

Gain/Attenuation Stage -- Barrel Shifter

- 24 dB gain at minimum attenuation
- Attenuation added in 6 dB steps

RX Configuration - ISL5416 (file name: vgatest1.416)

- CIC decimation of 4, 31thbf.imp filter decimating by 2, rrc64a22.imp filter decimating by 1.
- AGC enabled
- VGA RF delay = 4 clocks (pipeline delay of shifter board)
- Imm. Thresh = -2 dBFS, 6 dB change
- Upp. Thresh = -15 , 1
- Low Thresh = -30 , 1
- Bias 0.01
- Slot = 129, delay = 1, integ = 128, # integ = 1
- Upper limit = 24, Lower limit = 0

- The CIC input is backed off an extra 24 dB at the CIC barrel shifter to allow for up to 24 dB of gain.

- The AGC adds ~50 dB of gain to bring the target signal to -12 dBFS.

MINIMUM ATTENUATION

		TARGET	INTERFERER	
TX		-54	-6	-83 dBFS
GAIN	+24	-30	+18	-59 dBFS
MIXER	-6	-36	SAT	-65 dBFS
CIC SHIFT	-24	-60		-89 dBFS
AGC	+48	-12		-41 dBFS (-141*)

MAXIMUM ATTENUATION

		TARGET	INTERFERER	
TX		-54	-6	-83 dBFS
GAIN	+0	-54	-6	-83 dBFS
MIXER	-6	-60	-12	-89 dBFS
CIC SHIFT	-0	-60	-12	-89 dBFS
AGC	+48	-12	+36 (-64*)	-41 dBFS (-141*)

NOTE: *RECEIVER OUT-OF-BAND ATTENUATION ~ 100 dB

Appendix 2

Test Configuration 2 (analog components)

Signal Flow:

ISL5217 Digital Up-converter

-> HI5828 DAC, ~-5 to -6 dBm full scale

-> 10.7M LPF

-> Digital Attenuator, 6 dB steps, 2 dB min attenuation

-> Power divider (-4.5 dB gain)

-> 10.7M LPF

-> 14bit A/D, ~72 dB SNR, +4 dBm full scale

-> ISL5416 Digital Down-converter Evaluation Board

At minimum attenuation, there is approximately 17 dB of loss from the ISL5217 (digital) output to ADC/ISL5416 input.

Transmitter:

- ISL5217 Evaluation Board 61.44 MHz clock
- Channel 1: desired signal @ 8 MHz CW @ -30 dBFS at ISL5217, output -47 dBFS at A/D input (-12 dB multiplier, -18 dB (1/8) shift)
- Channel 2: interfering signal @ 11 MHz; Tx pattern - square wave AM with 77 dB modulation repeating sequence of 80 samples each of (0.7071, 0.7071) and (0.0001, 0.0001) at 240 ksps, Interpolated to 61.44 MSPS with a Gaussian interpolation FIR filter, IHBF, and high-order interpolation filter. Alternates between -0.2 and -77 dBFS at the ISL5217 output (-0.2 dB multiplier, shifter scale by 1) and -17 to -94 dBFS at the A/D input.

Receiver:

- ISL5416 Evaluation Board
- Range Control: 11 clock RF delay, -19 dBFS immediate threshold, 6 dB immedediate step, -30 dBFS upper threshold, 1 dB upper threshold step, -45 dBFS lower threshold, 1 dB lower threshold step, 0 dB leak, 128 clock integegration time, attenuation limits: 0, 24 dB
- Filtering: 5th order CIC, decimate by 4, 31 tap HBF, decimate by 2, 64 tap RRC, a=0.22 filter
- AGC: 0 to 96 dB gain range, -12 dBFS set point, 0.1 dB maximum attack, decay slew rates

Desired signal level is -47 dBFS to A/D converter w/ 0 dB attenuation and is -65 dBFS with 18 dB of attenuation.

There is 24 dB of loss in the CIC shifter due to back off to accommodate up to 24 dB of added gain (range control upper limit).

The mixing loss -6 dB because the input signal is composed of upper and lower sidebands, each at -6 dBFS and the tuner selects only one.

The desired signal is -47 - 24 - 6 = -77 dBFS at the CIC input with 0 dB attenuation, and -95 dBFS with 18 dB of attenuation.

To reach the programmed -12 dBFS set point, the AGC adds 64.4 and 65.2 of gain for 0 and 18 dB of attenuation, respectively.

SNR calculations:

The C/N for the desired signal at the output (7.68 MHz BW) with 0 dB attenuation is:

C/N= -47 dBFS - (-72 dB SNR) + (9 dB processing gain) = ~ 34 dB

(C/n_0 = -103 dBc/Hz).

The desired signal C/N at the output (7.68 MHz BW) with 18 dB attenuation is:

C/N = -65 dBFS -(-72 dB SNR) + (9 dB processing gain) = ~ 16 dB.

(C/n_0 = -87 dBc/Hz).

Appendix 3:

Example Calculations for SNR, MDS

The block diagram below shows a possible wide-band, single (analog) conversion receive chain design. There are, of course, many possible receive chain designs. The specifications listed were taken from the data sheets for the parts. The SAW filter loss is typical of low loss SAW filters and is not for any particular part number. If the LC filter is sufficiently sharp, F3 and A6 would not be needed. This architecture has not been built. The attenuators are available with a 31 range in 1 dB steps or a 15.5 dB range with 0.5 dB steps. The range control circuit would control the attenuators to step a single attenuator by 6 dB or each of two attenuators by 3 dB. The extra resolution can be used to compensate for gain variations in the other components. At system test or calibration the system gain could be measured and the attenuator codes in the ISL5416 adjusted to keep the RF/IF gain variation between systems within the resolution of the attenuator control.

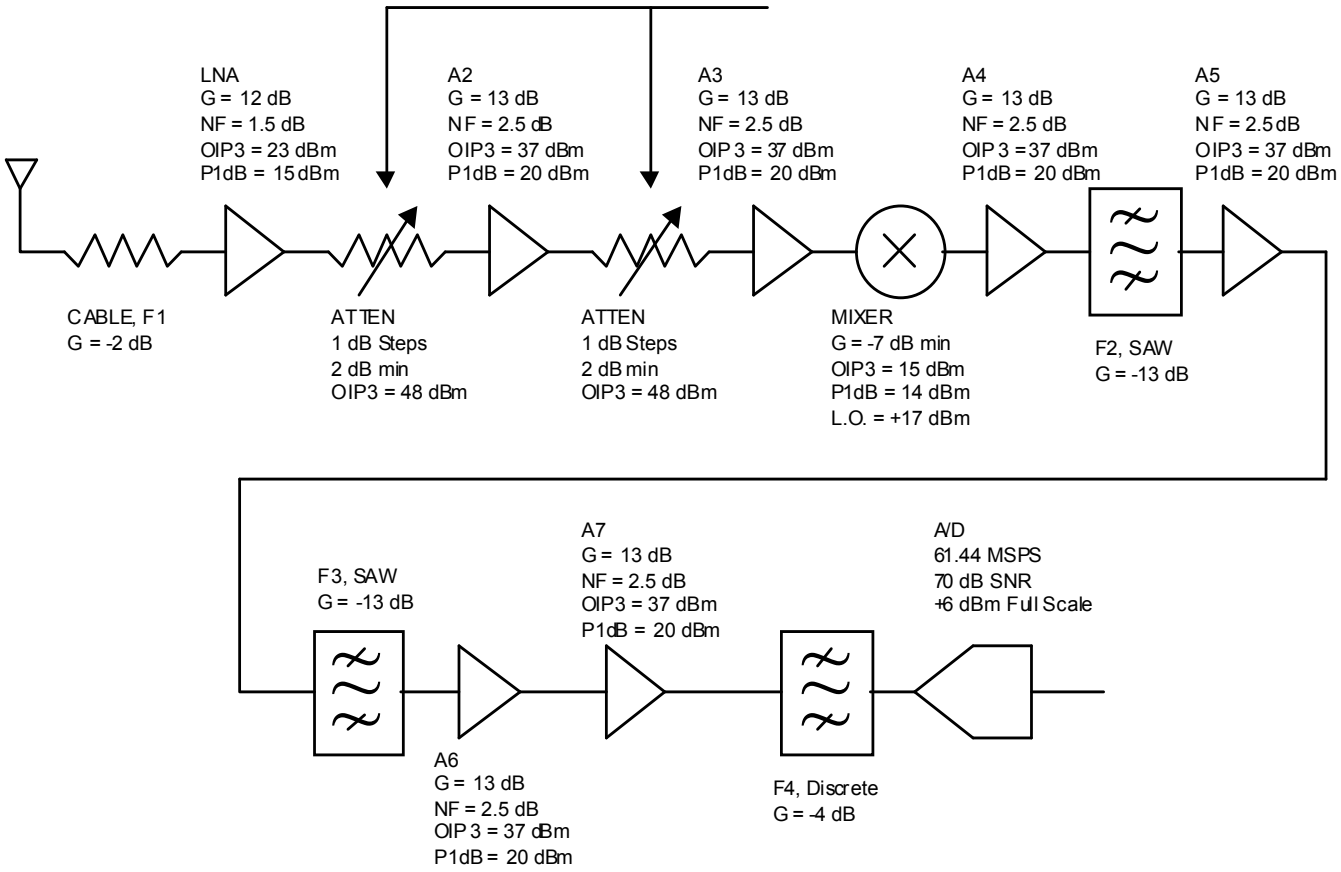


FIGURE 16. WIDE-BAND, SINGLE (ANALOG) CONVERSION RECEIVE CHAIN DESIGN

The table below shows the effects of the added attenuation on the minimum and maximum RF signal levels for the Rx chain shown. The two sets of entries show the difference in noise figure and minimum detectable signal (MDS) when using two 3 dB step attenuators, one before and one after an amplifier versus using a fixed attenuator and a single 6 dB step attenuator before an amplifier.

EFFECTS OF ADDED ATTENUATION ON THE MINIMUM AND MAXIMUM RF SIGNAL LEVELS

ADDED ATTENUATION (dB)	ATTENUATOR 1 (dB)	ATTENUATOR 2 (dB)	A/D FULL SCALE REFERRED TO THE RF (dBm)	MDS AT 5 dB Eb/No (dBm)	CASCADE NOISE FIGURE (dB)
0	2	5	-38	-123.9	4.2
6	5	8	-32	-122.6	5.5
12	8	11	-26	-119.9	8.3
18	11	14	-20	-115.5	12.6
24	14	17	-14	-110.2	17.9
0	2	5	-38	-123.9	4.2
6	8	5	-32	-122.0	6.1
12	14	5	-26	-118.2	10.0
18	20	5	-20	-112.9	15.2
24	26	5	-14	-107.12	21.0

The table below is provided for reference and lists the noise power increase from adding a second noise source versus the relative power of the second noise source.

NOISE POWER INCREASE

RELATIVE POWER (dB)	NOISE POWER INCREASE (dB)	RELATIVE POWER (dB)	NOISE POWER INCREASE (dB)
0	3.01	-10	0.41
-1	2.54	-11	0.33
-2	2.12	-12	0.27
-3	1.76	-13	0.21
-4	1.46	-14	0.17
-5	1.19	-15	0.14
-6	0.97	-16	0.11
-7	0.79	-17	0.09
-8	0.64	-18	0.07
-9	0.51	-19	0.05

Appendix 4

Calculations for 3GPP FDD Basestation RX Specifications

Review of specifications and requirements:

- Chip rate = 3.84 MCPS
- Minimum Detectable Signal (MDS) Requirement (from spec) reference sensitivity level = -121 dBm @ 12.2kbps and <0.001 BER
- In-band interference: Desired Signal: 12.2kbps, -91 dBm, spread to 3.84M; AWGN interference: -73 dBm/3.84M; SNR prior to despread = -91 - -73 = -18 dB in 3.84M NBW; Chip rate = 3.84M, Processing gain = 10*log10(2*3.84e6/12.2e3) = 28 dB (assuming filtering to 3.84M NBW before despread operation)
- SNR after despread = -91 - -73 + 28 = +10 dB in 12.2k NBW

Adjacent Channel/Blocking/IMD Specs

- Adjacent channel BER < 0.001 for a desired signal level of -115 dBm with an adjacent channel level -52 dBm (from spec.)
- Blocking level 1 -- WCDMA w/ one code -40 dBm @ 10M offset peaking of a RRC filter with a=0.22 is approximately 1.7 (4.6 dB). Desired signal is -115 dBm for interference test BER < 0.001
- Blocking level 2 -- CW -15 dBm @ 20M offset from the freq band edge (20+2.5 from the signal center freq). Desired signal is -115 dBm for interference test BER < 0.001
- IMD -- Signal 1 @ -48 dBm, +/-10MHz, CW Signal 2 @ -48 dBm, +/-20MHz, WCDMA w/ one code unless the I.F. filter bandwidth is >20M, signal 2 will be attenuated by the filter and the spec reduces to a CW signal at 10M at -48 dBm (versus -40 dBm for the 10M blocker spec.)

A/D requirements with blocking

CW blocker:

If we set the level at the A/D to handle the -15 dBm CW signal with a 1 dB backoff and we need 7 dB Eb/No for the -115 signal at a sample rate of 61.44M, if the receiver noise is A/D dominated, the A/D would need an SNR of:

Eb = -115 dBm - 10log(12.2k) = -156 dBm

No = -156 dBm - 7 dB = -163 dBm

A/D NBW = 10log(61.44e6/2) = 74.9 dB

N = -163 + 74.9 = -88.1 dBm

A/D FS = -15 dBm + 1 dB = -14 dBm

SNR = -14 - -88.1 = 74.1 dB

If more backoff is desired, the required SNR will increase accordingly.

Note that at a 20 MHz offset, the blocker should be attenuated some by the anti-aliasing filter. The amount depends on the sample rate. For example, at 61.44 MSPS, the band of interest may be 15M spanning from 7.68 to 23.04 MHz. To prevent aliasing of out of band signals, the antialias filter must provide full attenuation at 15.36 MHz from the band edge (7.68M from the DC or the folding frequency). The blocker is >20 MHz from the band edge, so it should be rejected by the anti-alias filter for bandwidths of 15.36M at 61.44 MSPS. The anti-alias filter specs will be easier at a higher sample rate such as 76.8M.

What is fully attenuated? For this test, the processing gain against a CW blocker is 25 dB. If we need 7 dB S/I after despreading, we can have the blocker at +18 dBc after filtering. This means that the anti-aliasing filter must provide 100-18=82 dB of out-of-band attenuation. If the CW blocker was seen by the A/D, this would be the SFDR requirement on the A/D.

Modulated blocker test

The modulated blocker is -40 dBm at +/-10MHz away from the signal, but it can be anywhere in the receive band. For a wide band receiver, we would assume that the desired signal could be at one end of the receive filter and the blocker at the other, i.e. we get no help from the analog filtering.

With a single code transmitted through a RRC filter with a=0.22, the peaks would be approximately 1.7 times the nominal symbol level. This is ~4.6 dB above the nominal. Repeating the calculation for A/D SNR, but allowing for the PAR:

Eb = -115 dBm - 10log(12.2k) = -156 dBm

No = -156 dBm - 7 dB = -163 dBm

A/D NBW = 10log(61.44e6/2) = 74.9 dB

N = -163 + 74.9 = -88.1 dBm

A/D FS = -40 dBm + 4.6 + 1 dB = -34.4 dBm

SNR = -34.4 - -88.1 = 53.7 dB

Any help from the I.F. filter will reduce the SNR requirement. Any additional back off from full scale will increase it.

Assuming the same 18 dB of rejection of the blocker by the despreading (it is actually closer to 21 due to the filtering to 3.84 MHz before despreading), the A/D SFDR needs to be:

-40 (blocker)

- -115 (signal)

+ 7 (desired SNR)

- 18 (processing gain)

+ 5.6 (A/D backoff

69.6 dB

Since the reference sensitivity level is only 6 dB below the signal level for the blocker tests at -121 dBm, increasing the requirements on the A/D by 6 dB could allow us to meet the specifications without an I.F. AGC if the noise is A/D dominated. However, for the reference sensitivity test, the RF noise will come into play, so the A/D specs would have to be improved by more than 6 dB to meet both the blocker and reference sensitivity tests without a variable gain element between the RF and A/D.

Adjacent Channel Interference

This is smaller than the modulated blocker, so the blocker specs are more stringent on the A/D. The adjacent channel spec can be more than one code, so the crest factor may be higher. However, the 12 dB difference in power between the modulated blocker and the adjacent channel should allow for the difference in crest factor. This specification is more of a consideration for the DSP receive processing.

IMD

The total power is less then the modulated carrier, so this should be less stringent. Also, the large frequency to signal 2 should allow the I.F. filtering to attenuate it so that the spec would typically only apply RF/IF components in the system.

If the I.F. filter allowed both signals to pass:

The two signals are each at -48 dBm. This is 8 dB lower than the modulated blocker. If these were both CW, they would have peaks 6 dB higher at -42 dBm. Since one signals is modulated, it could theoretically peak 4.7 dB higher due to filtering to -37.3 dBm. This is slightly lower than the modulated blocker test (-40 + 4.6 = -35.4 dBm).

DSP Processing requirements

Assume full scale at the A/D is -34 dBm (from the modulated blocker test w/o filter attenuation). The MDS is -121 dBm or -97 dBFS. We must filter and output this signal without adding any significant degradation. Any noise in the DSP should ideally be >10 dB below the input noise or interference to cause <0.4 dB of additional degradation or even better >20 dB below for <0.05 dB increase. Since DSP noise is the easiest noise to control, it should be insignificant in the system. If we assume no front end AGC and set the gain so that the input referred noise from the A/D is -169 dBm/Hz for the no AGC case, this is equivalent to an RF noise figure of 5 dB. With an RF noise figure of 5 dB, the total RF and A/D noise would be -166 dBm/Hz for an MDS Eb/No of 4.1 dB.

Given these assumptions, the A/D and RF noise is

-166 - (-34) = -132 dBFS/Hz.

To keep the DSP noise 20 dB below this, it must be -152 dBFS/Hz or less. If the minimum sample rate in the DSP is 2x the chip rate, then the quantization noise is spread across 3.84 MHz of bandwidth. (While complex processing paths have 2x the bandwidth of real processing to spread the noise another 3 dB, the noise in each complex arm is independent, to they add to make the net result the same as real processing.)

RF and A/D noise = -132 dBFS/Hz

DSP noise = -132 dBFS - 20 = -152 dBFS/Hz

BW = 10log10(3.84e6) = 65.8 dB

Ndsp = -152 + 65.8 = 86.2 dBFS @ 7.68 MSPS

This is the total noise from all DSP sources. The dominant noise source will usually be at the narrowest bandwidth. The others will contribute according to their bandwidths. The calculation says the minimum bit width could be as low as 15 bits at the FIR output, but to allow for any signal attenuation in the DSP processing and for any back off to allow for peaking in the filters, the bit width should probably 2-4 bits more than this or 17-19. Any additional headroom required at the A/D will increase this requirement as well. The ISL5416 provides a minimum 20 bits through the filtering to the AGC.

AGC range requirement calculations

Full scale signal into the DSP -34 dBm

RF + A/D noise -166 dBm/Hz

A/D NBW 10*log10(61.44/2) 74.9 dB

(not considering the I.F. filter

effect on RF noise)

Output NBW 10*log10(3.84e6) 65.8 dB

N into A/D -91.1 dBm

N in channel -100.2 dBm

MDS -121 dBm

DSP gain/loss and backoff 12 dB

Output backoff 12 dB

The minimum signal power in the channel will be the noise at -100.2 dBm (this will put the MDS at 21 dB below the noise and 33 dB below full scale at the output to the DSP.)

Maximum signal in the channel

Not specified, but assume that it is equal to the adjacent channel interference level at -52 dBm.

Gain needed through the DSP for a noise dominated output

max gain: minimum signal = input noise

-34 dBm full scale

- -100.2 dBm minimum signal (noise)

+ 12 dB DSP loss, backoff

- 12 dB desired output level

66.2 dB max gain needed

min gain: max signal

-34 dBm full scale

- -52 dBm max signal in channel

+ 12 dB DSP loss, backoff

- 12 dB desired output level

---

18 dB min gain needed

Minimum AGC adjustment range needed = 66.2 - 18 = 48.2 dB

Appendix 5

Digital Noise Floor Calculations with A/D Range Control

Each processing block in the data path adds quantization noise to the signal as it passes through the ISL5416. The data path was sized to minimize the degradation of the input signal to noise by these noise sources. An example calculation of the noise contributions is given below and shown pictorially in figure 17.

Assumptions:

1. A/D range control adjustment range: 18 dB
2. RF input for A/D full scale (no RF attenuation): -30 dBm (chosen to put the A/D noise 6 dB below the RF noise for an RF noise figure of 3 dB)
3. A/D sample rate: 61.44 MSPS
4. A/D SNR: 72 dB

Because the CIC shifter adds gain to compensate for RF attenuation, there is a net 18 dB of attenuation from full scale when there is no RF attenuation.

The combination of the mixer, CIC barrel shifter, and the CIC can have from 6 to 12 dB of attenuation. This is due in part to the non-power-of-two gain in the CIC that cannot be fully compensated by the shifter. There is also a 6 dB loss in the mixer because the tuner selects only the upper or lower sideband of the real input signal. After the unwanted sideband is filtered out, 6 dB of gain can be added.

Worst case A/D full scale level vs data path full scale: -24 dB (18 dB for the RF shift and max of 6 dB for uncompensated CIC gain).

Data path full scale referred to the RF input: -6 dBm

AN EXAMPLE OF THE NOISE CONTRIBUTIONS

	BITS	SAMPLE RATE (MHz)	QUANTIZATION NOISE (dBFS/Hz)**	dBm/Hz @ RF
INPUT	16 + 4*	61.44	-194	-200
L.O.	19 + 4*	61.44	-212	-218
MIXER OUTPUT	≥ 24 + 4*	61.44	-242	-248
SHIFTER OUTPUT	≥ 24	61.44	-218	-224
CIC OUTPUT	24	15.36	-212	-218
GAIN STAGE 1	20	15.36	-188	-194
FIR1 OUTPUT	24	7.68	-209	-215
GAIN STAGE 2	20	7.68	-185	-191
FIR2 OUTPUT	24	7.68	-209	-215
TOTAL				-188

NOTE: * These noise sources are prior to the shifter, so the bits of shifter backoff are added.

NOTE: ** Nq = full scale - 20*log10(#bits) 1.76 dB - 10*log10(Fs/2) + 3.01

1

The A/D noise referred to RF is:

n_o = RF_for_A/D_full_scale - $10*\log_{10}$(Fsamp/2) - A/D_SNR = -30 dBm - $10*\log_{10}$(61.44e6/2) - 72 dB = -177 dBm/Hz referred to RF.

The total ISL5416 quantization noise from above = -188 dBm/Hz referred to RF.

The input noise from the front end noise figure = -171 dBm/Hz.

The A/D noise adds about 0.97 dB to the RF front-end noise: -170.03 dBm/Hz.

The ISL5416 adds an additional 0.07 dB to bring it to: -169.96 dBm/Hz

Increasing the attenuator range to 24 dB would bring it to: -169.76 dBm/Hz due to the 6 dB increase in the ISL5416 noise floor.

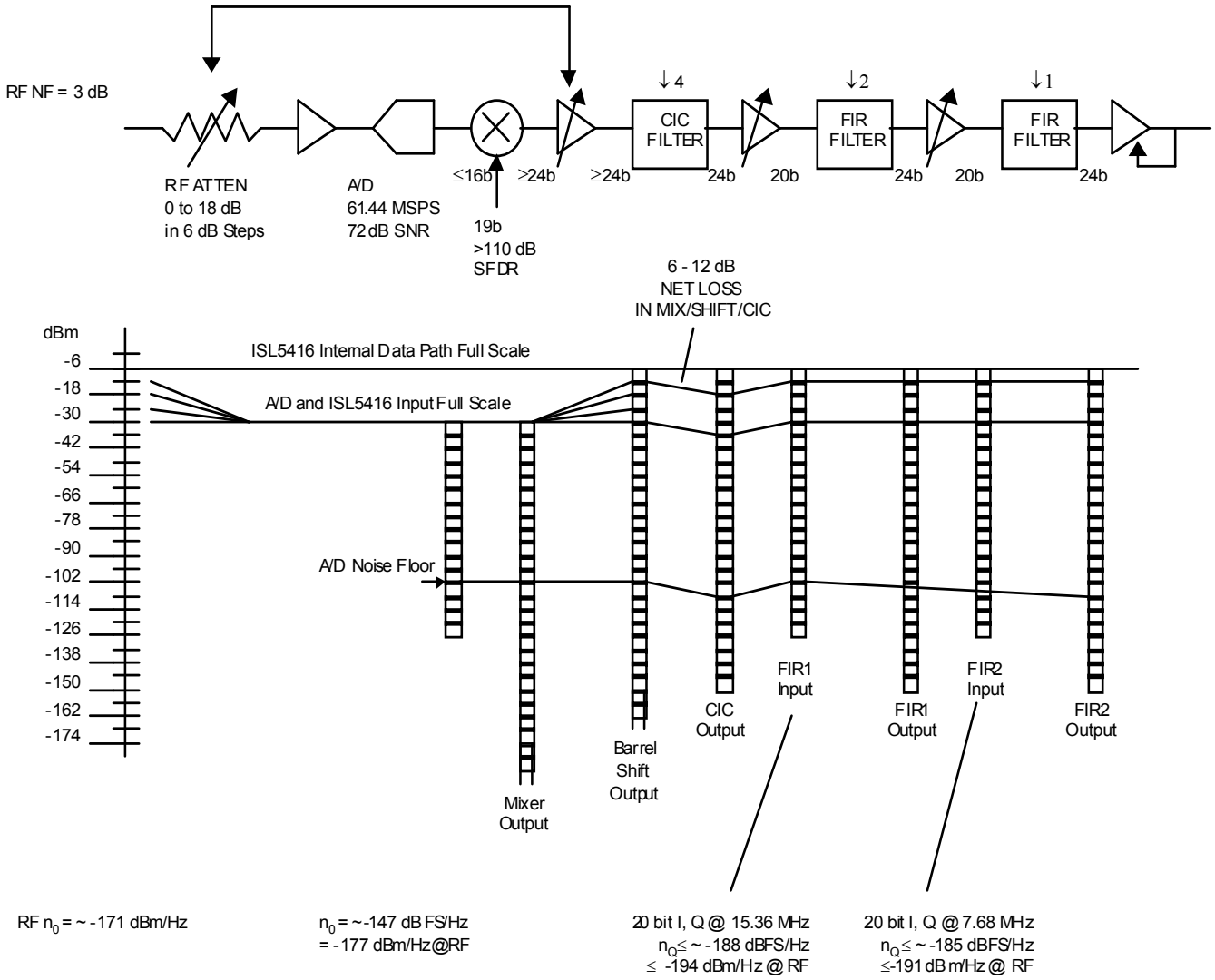
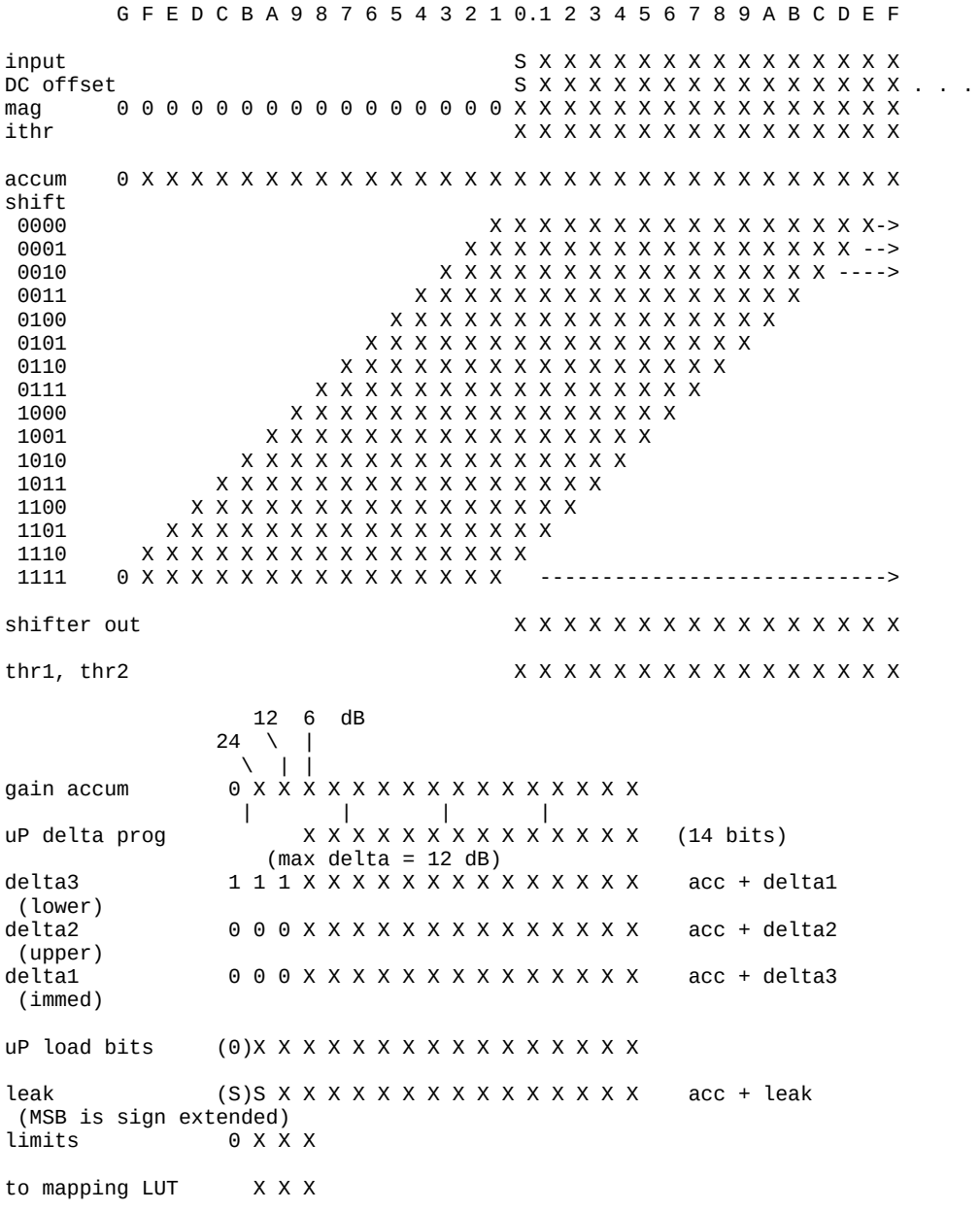


FIGURE 17. NOISE FLOOR CONTRIBUTIONS

Appendix 6 - Range Control Data Path Bit Weighting



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Colophon 7.0

A/D Range Control Using the ISL5416 3G QPDC

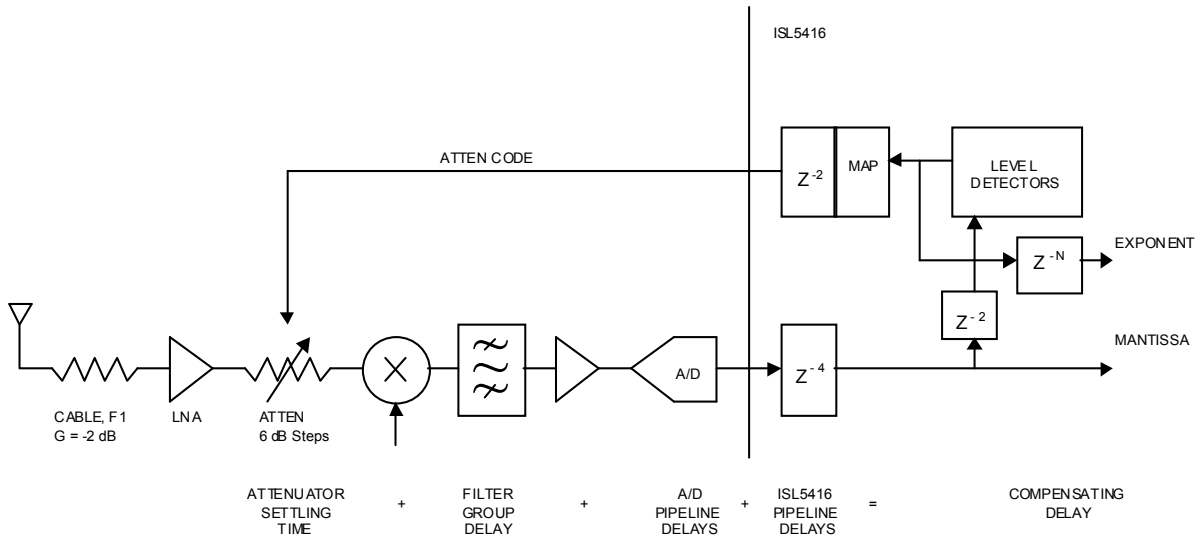
AN1017
Rev 0.00
May 2002

Overview:

The ISL5416 has a range control circuit that monitors the samples from the A/D and adjusts the RF/IF gain to optimize receiver sensitivity. The circuit reduces gain when large signals are present to prevent A/D saturation and increases gain to maximize sensitivity when no large signals are present. This shifts the instantaneous dynamic range of the A/D up and down within the total receiver range set by A/D dynamic range plus the RF/IF attenuation. The RF/IF attenuation controlled by the range control circuit can be thought of as the exponent portion of a floating-point digitizer and the A/D output thought of as the mantissa. The ISL5416 requires that the gain adjustments be in 6 dB increments though in general, floating-point digitizers can use any exponent step size. The DSP processing in the ISL5416 adds 6 dB of gain to the A/D output (mantissa) for each 6 dB of RF/IF attenuation step. This converts the floating-point samples to fixed point for processing. The overall gain is constant through the RF, A/D, and DSP front end. A simplified block diagram is provided in figure 1.

Figure 2 illustrates what happens to the signal at various points from the RF to through the DSP front end. As the RF signal level increases, the signal envelope at the A/D output crosses a threshold and the range control circuit increases the RF attenuation to reduce the signal level at the A/D input. Whenever the RF attenuation is increased, the DSP gain is increased to compensate and maintain a constant overall gain from the RF through the DSP front end. The attenuation and gain controls signals are in offset in time to compensate for the delays from the RF through the A/D and DSP.

Figure 3 illustrates how the instantaneous dynamic range of the A/D maps to the RF signal range. As attenuation is added, the full scale at the A/D corresponds to a larger RF signal power. The added attenuation, however, also raises the A/D noise floor relative to the RF input and reduces sensitivity.



NOTE: The compensating delay, Z^{-N}, is chosen as close as possible to the sum of the settling time, group delay, and pipeline delays. This minimizes the transient due to an attenuation change. The delay is programmable from 1 to 256 clock periods (12 ns to 3.2 us at 80 MSPS).

FIGURE 1. TYPICAL SYSTEM CONFIGURATION, INCLUDING SIGNAL DELAYS

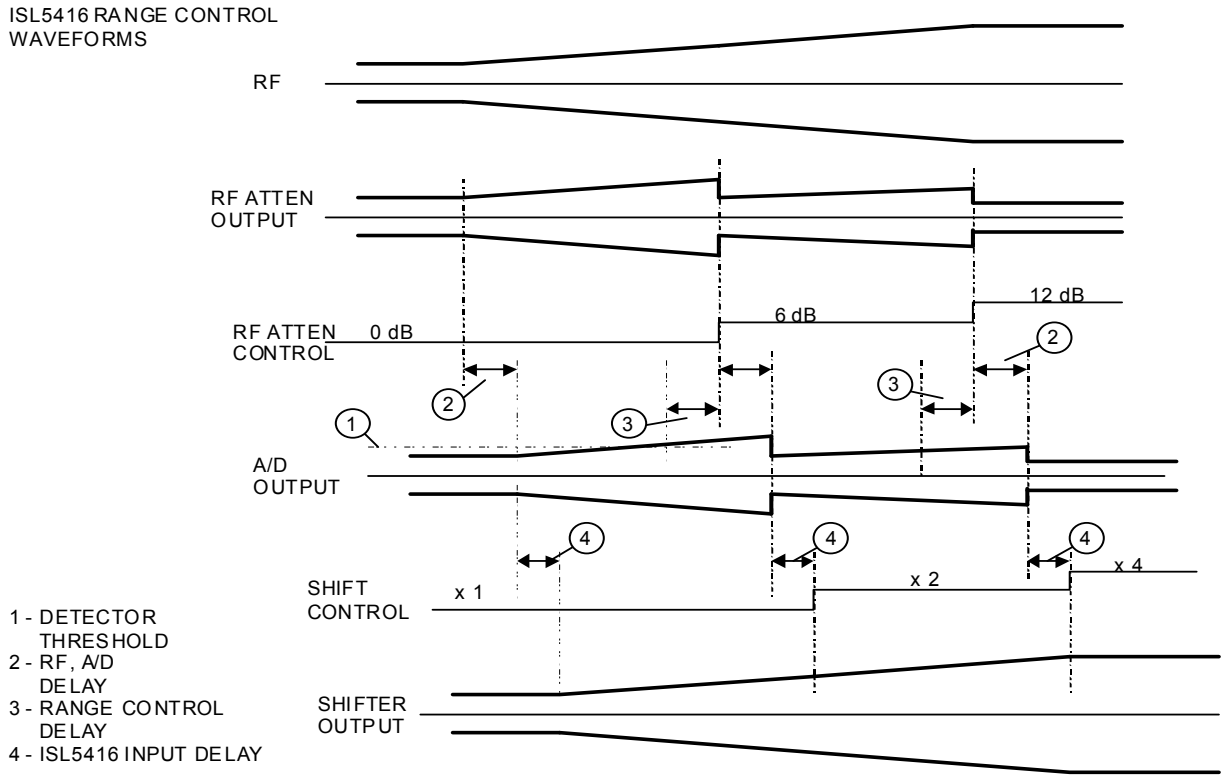


FIGURE 2. ISL5416 RANGE CONTROL WAVE FORMS

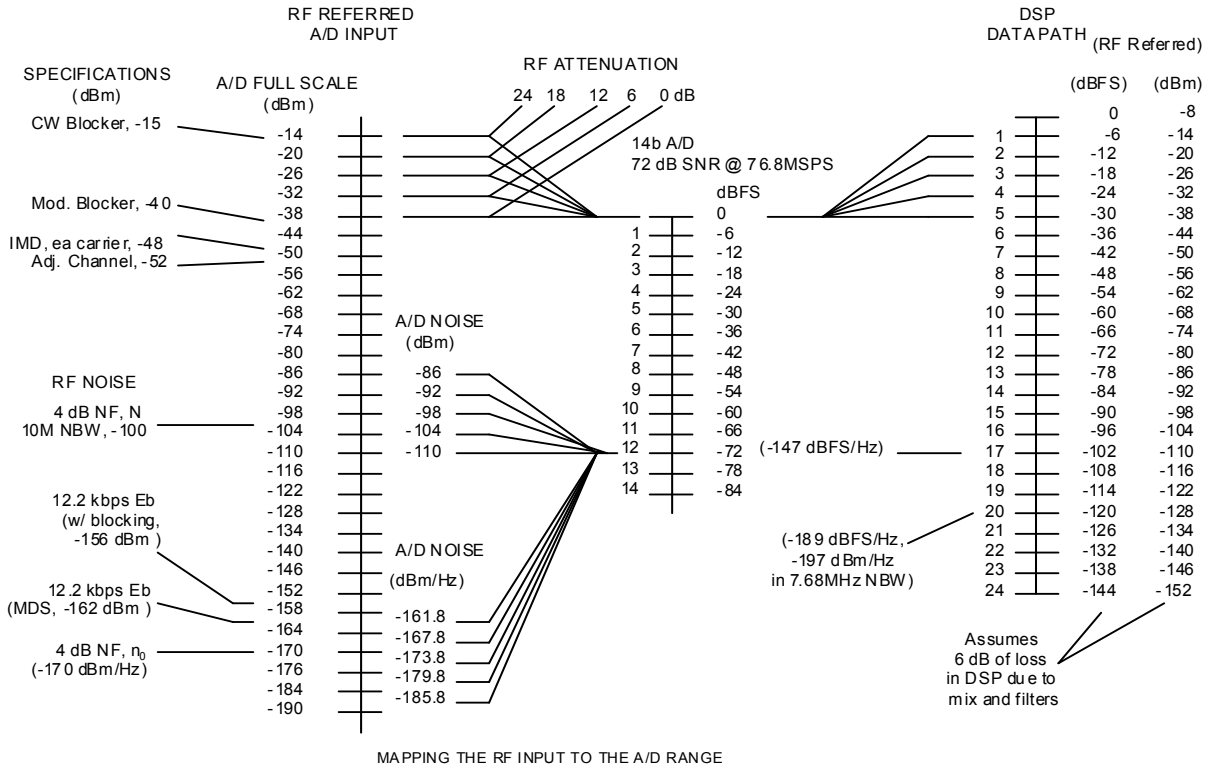


FIGURE 3. MAPPING THE RF INPUT TO THE A/D RANGE

The ISL5416 Range Control Operation Description

Figure 4 is a simplified system block diagram of the ISL5416 range control circuitry. The input samples from the A/D are monitored with a set of filters and level detectors. The level detector decisions control whether to increase or decrease the contents of an accumulator that holds an RF/IF attenuation word. Only the MSBs of the accumulator are mapped to the attenuation control bits, so by programming the accumulator changes to be below these MSBs, the accumulator can act as a filter on the detector outputs. Programmable upper and lower limits restrict the accumulator to only the attenuation range that is needed.

There are two signal paths for the samples from the A/D converter. In one path, the absolute value of each sample is compared to a programmable threshold. In the other path, the samples are averaged before making a decision. In the sample-by-sample path, if any sample exceeds the threshold, the RF/IF attenuation is immediately increased. The purpose of this detector is to prevent saturation of the A/D converter due a rapid increase in input power, and this detector is given the highest priority. The threshold for this detector is usually set within a few dB of the A/D full scale and the gain adjustment from an immediate threshold crossing usually set to 6.02 dB. After an immediate threshold crossing, the immediate detector is disabled for a programmable number of samples to allow the loop to settle before making another adjustment.

The other signal path filters the A/D samples before making decisions. The samples are first high-pass filtered to block DC offsets from the A/D converter. The absolute values of the samples are then averaged in an integrate-and-dump circuit. The integration period is programmable from 2 to 65536 samples. Averaging reduces the standard deviation of the samples for a better decision and is a necessity for a lower limit comparison since the A/D samples pass through zero. The integrator output is divided by 2^N in a barrel shifter to compensate for growth in the integrator and reduce the range of the data to the detectors. The average magnitude is next compared against upper and lower thresholds. In the averaged signal path, threshold decisions are only made at the end of the integration period. If the upper threshold is exceeded, the attenuation control accumulator is increased by a programmable amount. If the average falls below the lower threshold, the accumulator is decreased by a separate programmable amount. These average signal thresholds set the desired operating limits for the signal to the A/D. The upper limit is typically set based on the peak-to-average ratio of the expected input signals with sufficient back off to prevent tripping the immediate threshold. The lower limit is set to guarantee a minimum SNR from the RF and/or a minimum number of effective bits from of the A/D converter. When the signal falls below this threshold, attenuation is removed to lower the RF noise figure and to increase the signal to the A/D so that more bits toggle.

If the average magnitude is between the upper and lower averaged limits, at the end of the integration period a programmable bias value is added to the attenuation control accumulator. This bias slowly adds or removes attenuation to bias the signal toward one end of the operating range. This bias overcomes the large hysteresis that results when there is a large separation between the upper and lower thresholds. For small separations between the upper and lower thresholds, the bias can be disabled.

The three MSBs of the attenuation control accumulator represent the attenuation value from 0 to 42 dB in 6 dB steps. These three bits are routed to the tuner channels that receive the input samples and control the amount of additional gain that is added by a barrel shifter that precedes the CIC filter. The gain is added at the CIC to maximize the dynamic range through the NCO/mixer stage. The three gain control bits are delayed by a programmable delay stage to compensate for the delays in the RF/IF/DSP due to attenuator settling time, filter group delays, and A/D and DSP pipeline delays and align the CIC shifter gain changes with the RF changes. The delay is programmable from 1 to 256 clock periods, providing up to 2.56 usec at 100 MSPS.

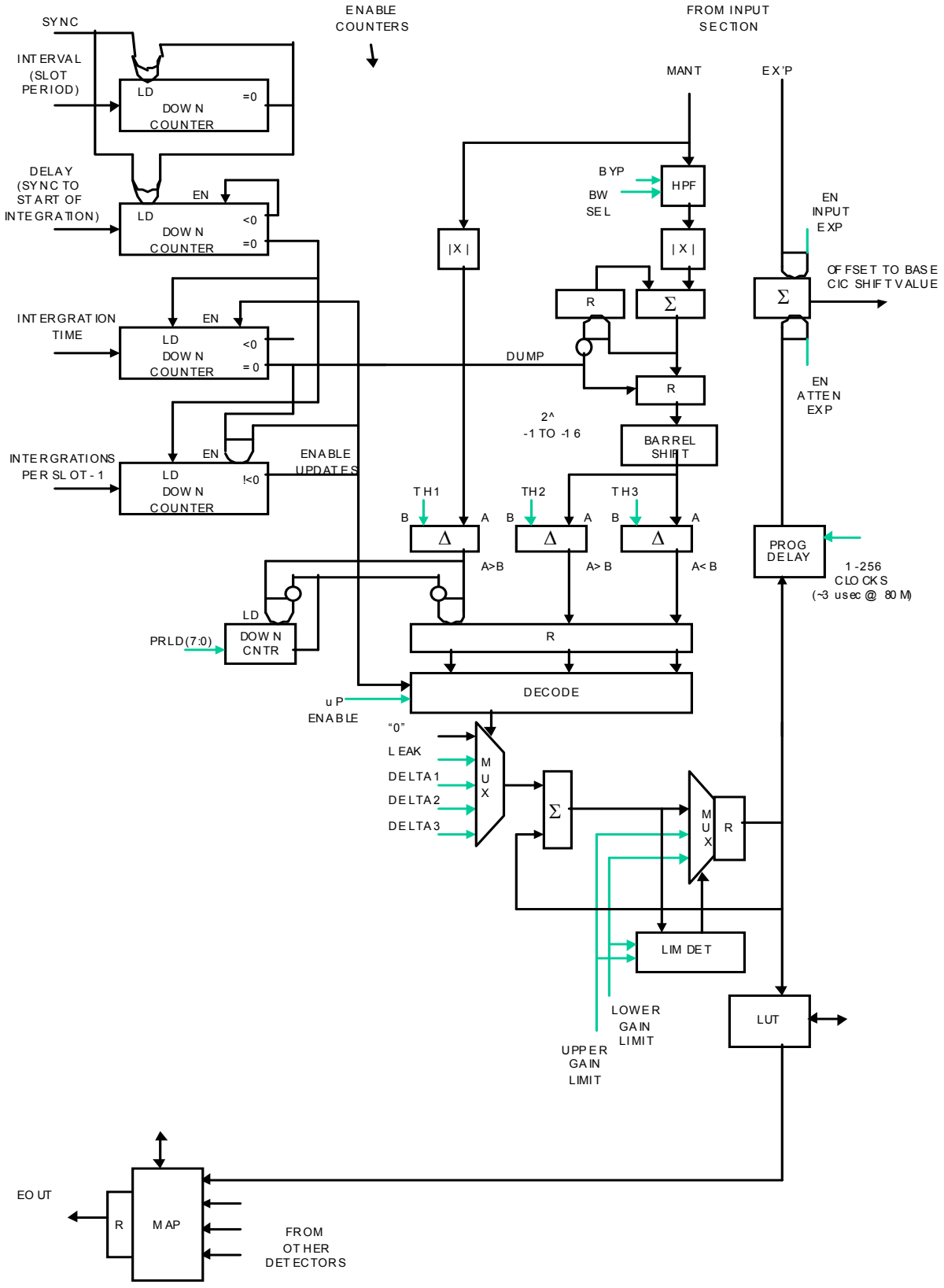


FIGURE 4. RANGE CONTROL BLOCK DIAGRAM

To simplify the interface to attenuators from different manufacturers, the three-bit attenuation control addresses an 8-location look-up table with 8 bits per location. Each location corresponds to one of the attenuation steps and up to 8 bits can be used to control the attenuation at each step. If the attenuator has finer resolution than 6 dB, the extra bits and attenuation steps can be used for calibrating the RF/IF gains with different codes loaded in the look-up tables for each input bus to equalize the gains to each A/D.

The 16-bit EOUT bus is the attenuation control bus. It updates at the CLKC rate. The mapping of range control channel to EOUT bits is programmable in four bit groups so that either four range control channels with four bits per channel or two channels with eight bits per channel can be used.

There is a set of four counters that control the range control updates in the averaged data path. The sample-by-sample data path operation is independent of the counters. Figure 5 illustrates the counter operation. The timing is based on a slot period and which can be aligned to system timing events such as TDM slots or can free run asynchronous to the system timing. Within the slot there can be one or more integration periods for the averaged data path described above. The integration periods shifted around within the slots and across slot boundaries using a delay counter. The delay compensates for TX/RX offsets and/or RF/IF group delay. An integration time counter sets the length of each integration period. An integration period counter counts the number of integration periods per slot. The slot counter sets the overall time interval from 1 to 65536 input clock or sample periods. The slot counter restarts when it finishes its count but can also be restarted by a SyncIn signal to align it to the system timing. The delay counter is loaded at the same time as the slot counter. The first integration period begins when the delay counter reaches the end of its count.

The control microprocessor can load the attenuation control accumulator to initialize it or to manually control the attenuators. So that it can monitor the operation of the range control circuit, the processor can read the range control accumulator, read the DC offset value blocked by the high pass filter, and read the normalized averaged magnitude.

Test Data

Test data from two lab configurations is presented below. The first case used all digital components. The second case added a D/A, an A/D, and analog filters and replaced a digital barrel shifter with an analog attenuator with digital controls.

Case 1: All-Digital Test Configuration

Figure 6 shows the configuration for this test. A multi-channel digital up converter evaluation board, the ISL5217EVAL was used to filter, interpolate, and modulate a digital pattern to a sampled IF. The digital output of the evaluation board was then routed through an FPGA prototyping board with the FPGA programmed as a barrel shifter. The barrel shifter included saturation logic to prevent wraparound in the event of overflow. The output of the barrel shifter was connected to the input bus of an ISL5416 evaluation board. Pins from the EOUT bus were connected to the barrel shifter controls to close the range control loop. D/A converters on each board allowed monitoring of the important signals.

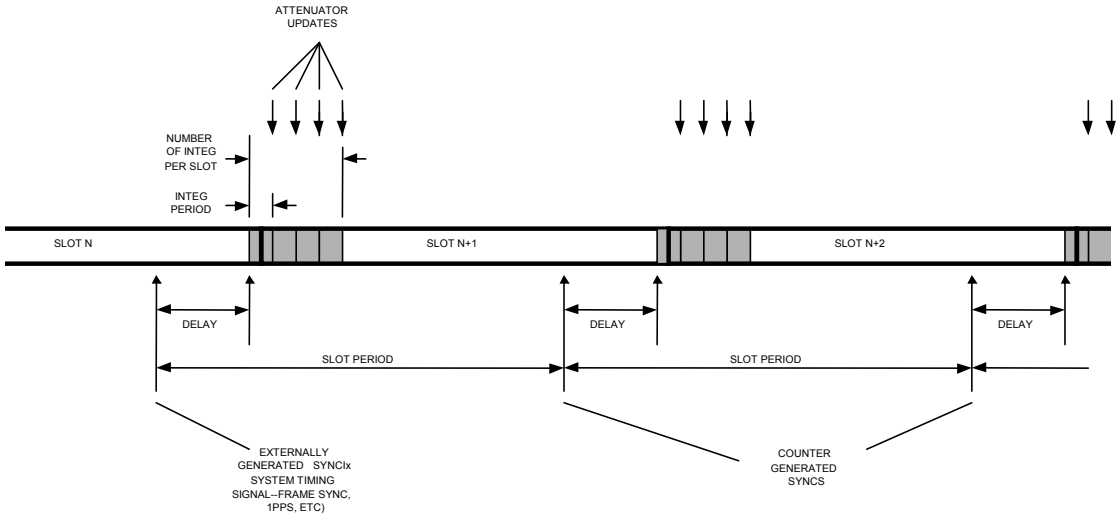
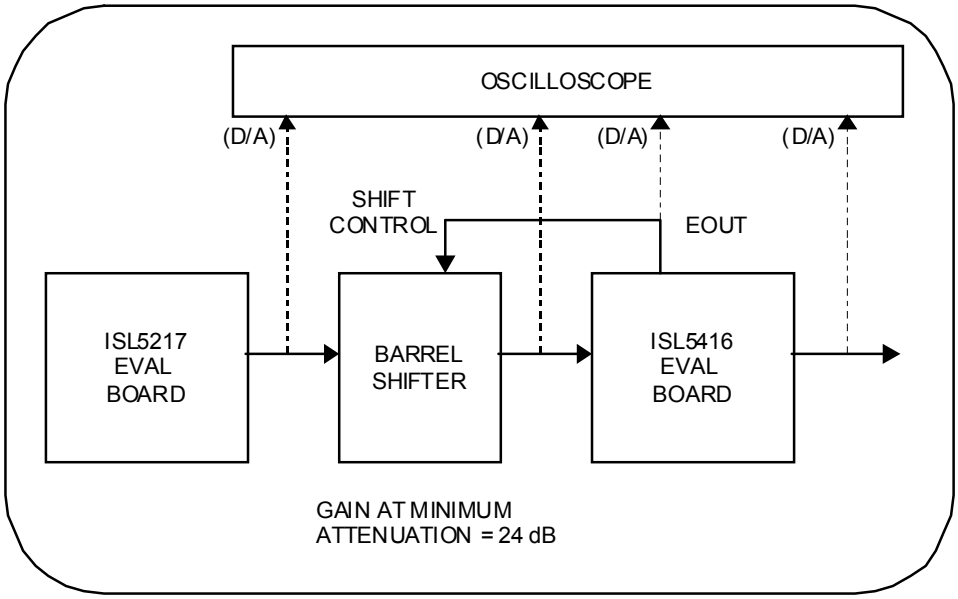


FIGURE 5. RANGE CONTROL TIMER OPERATION



NOTE: Connections between the evaluation boards are 16-bit digital. D/A converters on the boards and a 4-channel digital oscilloscope are used for monitoring and data collection.

FIGURE 6. TEST CONFIGURATION 1

Two channels of the digital up converter were used. One channel generated a CW signal at 8.5 MHz. The other channel filtered and modulated a square wave baseband pattern onto an 11 MHz carrier. A Gaussian filter was used to produce rapid envelope changes while limiting the width of the spectrum. The AM modulation depth was 77 dB from 48 dB above to 29 dB below the CW carrier. Hard-wired gain in the barrel shifter put the modulated signal range from +18 dBFS to -59 dBFS at the input to the ISL5416 at the minimum attenuation setting. Figure 7A shows the signal levels and gain distribution. Appendix 1 provides more details on the configuration and gain distribution.

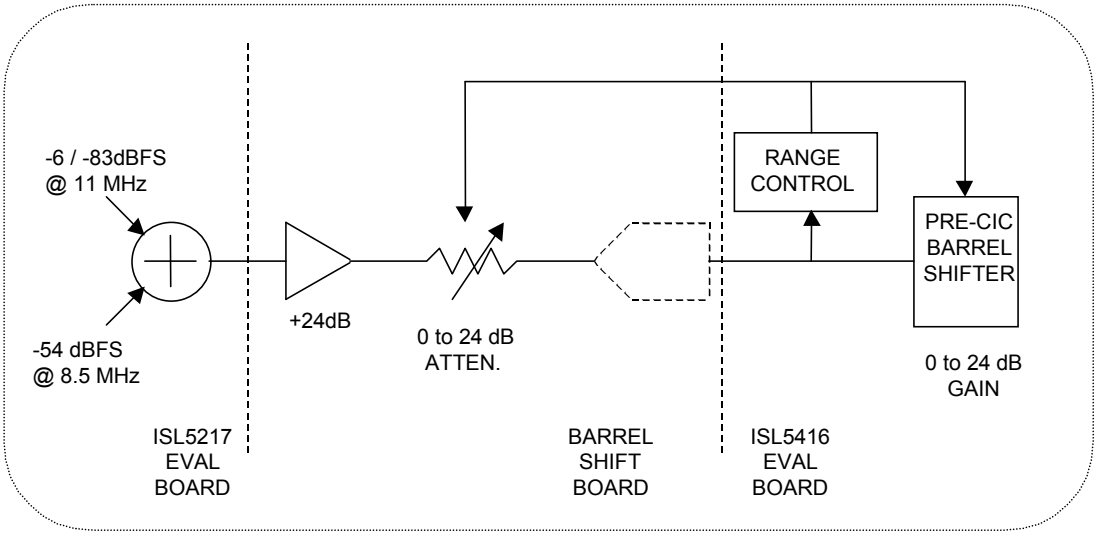
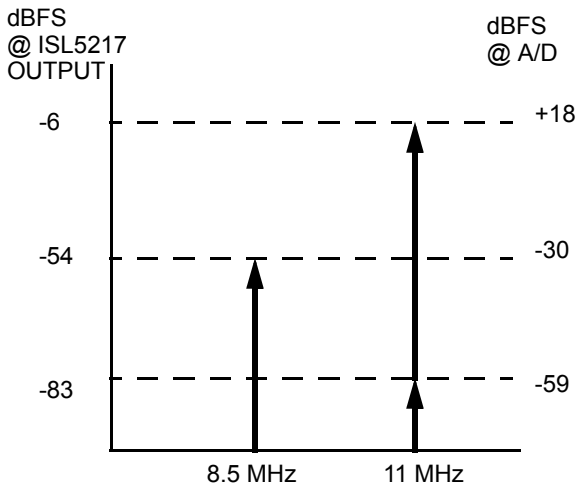


FIGURE 7A. TEST CONFIGURATION 1 GAIN DISTRIBUTION



NOTE: The desired signal is at 8.5M and the AM Modulated Interferer is at 11.5M

FIGURE 7B. TEST CONFIGURATION 1 SIGNAL LEVELS

Figures 8A and 8B show the waveforms at the rising and falling edges of the square wave, respectively. In both cases, the digital oscilloscope samples at approximately 6 times the input clock rate and the ISL5416 output sample rate was 1/8 the clock rate. In figure 7A, as the signal ramps up, it crosses the immediate threshold and triggers a 6 dB increase in attenuation. The hold-off counter prevents additional immediate threshold triggers while the gain change propagates through the pipeline delays in the 5416 and barrel shifter (a total of 12 clocks). During this delay, the signal ramps fast enough that the shifter output saturates briefly. When the hold off counter times out, the immediate threshold triggers again, increasing the attenuation to 12 dB. The signal slew rate decreases, but still triggers another attenuation increase to 18 dB. The signal settles to its final value below the immediate threshold, but above the upper threshold of -15 dBFS. After 6 integration periods at 1 dB attenuation increase per period, the attenuation control accumulator reaches its next 6 dB step and the shifter output is reduced below the upper threshold and holds at 24 dB of attenuation. Note that the brief period of input saturation caused a short period of signal suppression at the output of the 5416.

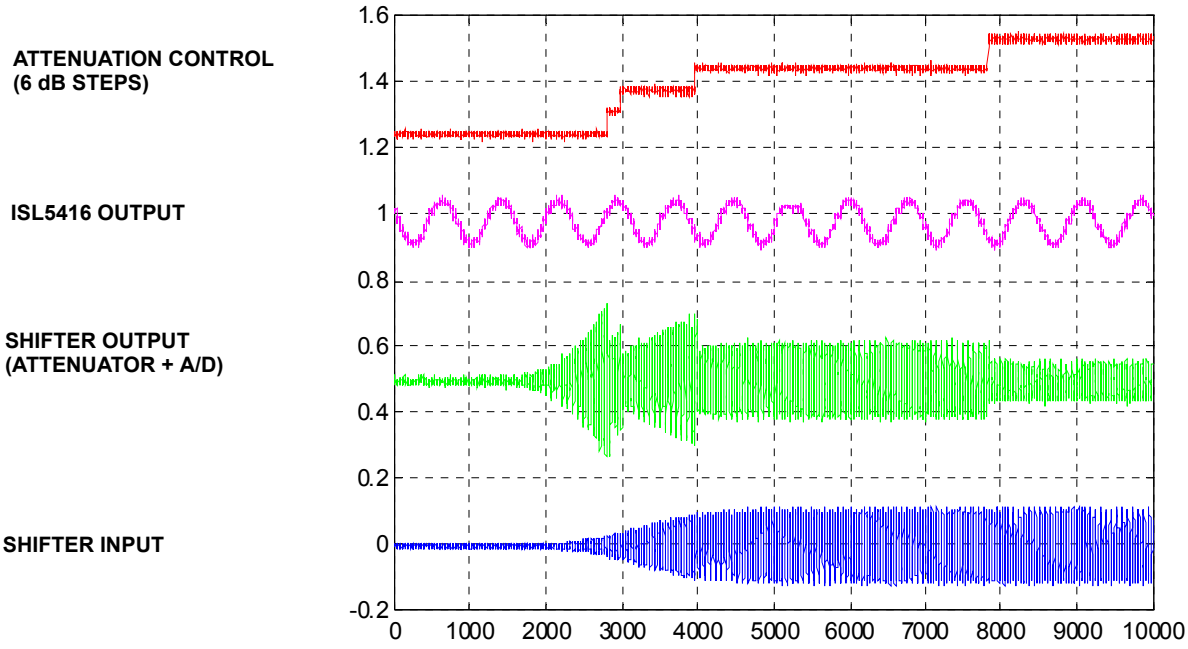


FIGURE 8A. ARRIVAL OF INTERFERING SIGNAL

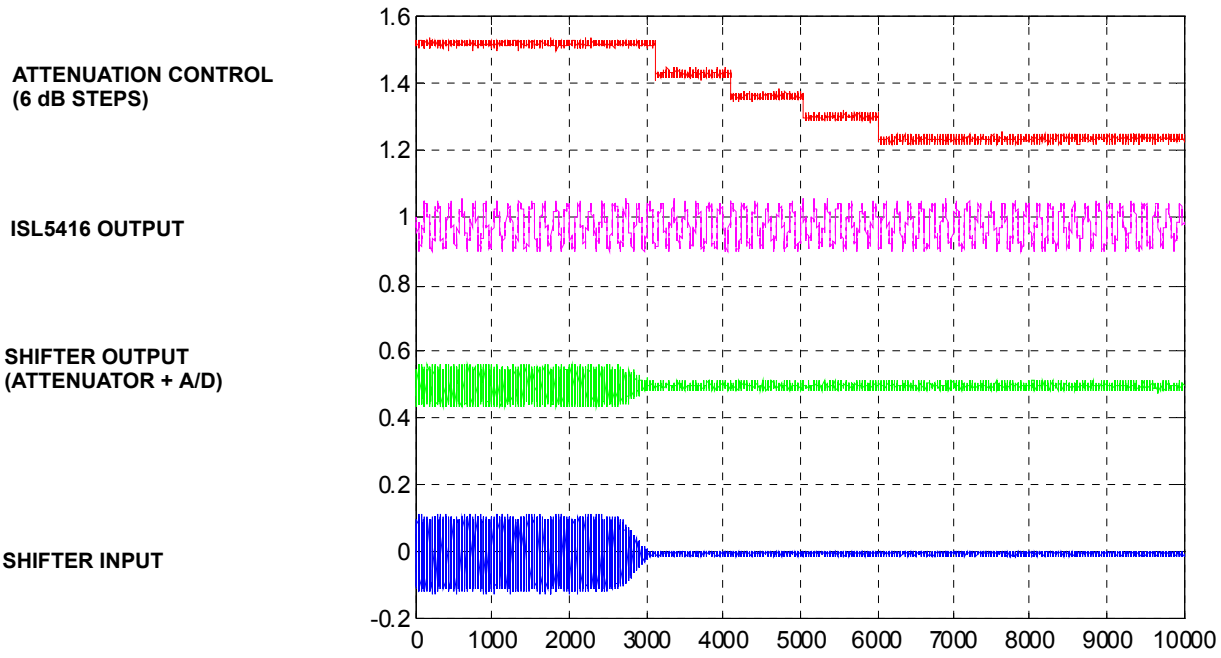


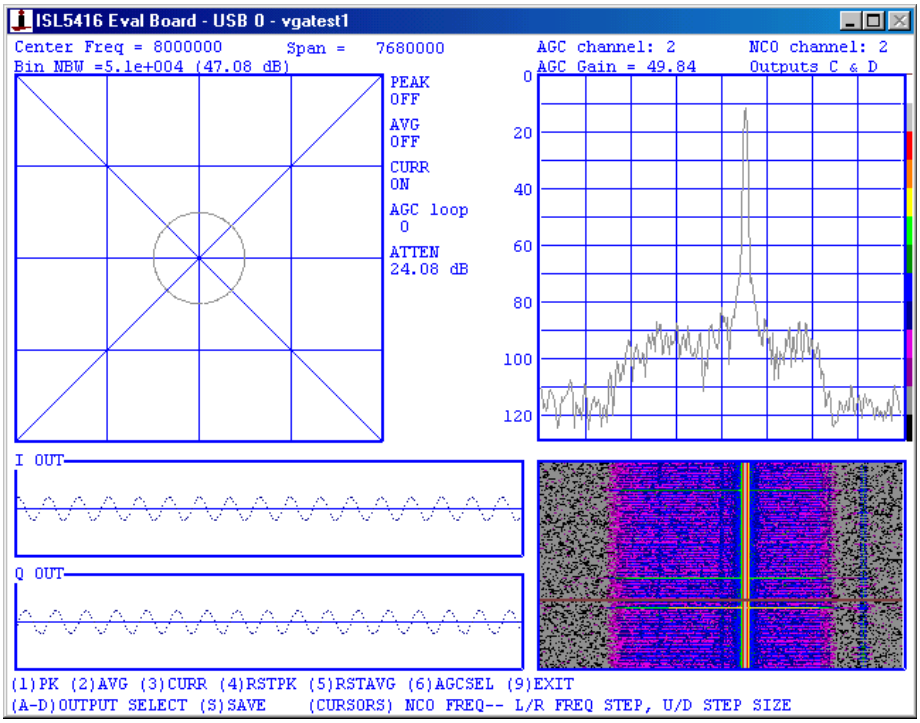
FIGURE 8B. DEPARTURE OF INTERFERING SIGNAL

When the signal falls below the lower threshold, the attenuation control accumulator starts to ramp down. Eventually it reaches minimum attenuation. The number of significant bits at the shifter output (A/Din a real system) increases as the attenuation decreases.

Figure 8B shows the falling edge of the modulated signal. In this case, only the lower threshold has an effect and the attenuation is removed in 6 dB steps until the attenuation is once again 0 dB. When the signal falls below the lower threshold, the attenuation control accumulator starts to ramp down. Eventually it reaches minimum attenuation. The number of significant bits at the shifter output (A/D in a real system) increases as the attenuation decreases.

Figures 9A and 9B show the ISL5416 evaluation board software display screen for the minimum and maximum attenuation cases, respectively. Note that the attenuation shown on the screen is not accurate because the output samples and range control attenuation are retrieved from the board in two accesses and the gain is changing faster than the access rate over the USB bus. Note the increase in the noise floor when the attenuation is added. This is because the signal of interest has been attenuated 24 dB toward the quantization noise floor at the input to the ISL5416. The CIC barrel shifter compensated for the loss, so the AGC gain did not changed. The output SNR, however, has dropped as the full-scale input range ISL5416 has increased 24 dB.

Note that the decrease in SNR is not quite 24 dB. This is because at minimum attenuation, the signal is backed off 24 dB at the CIC barrel shifter and the input noise floor is attenuated below the 20-bit quantization noise floor in the data path. At maximum attenuation, there is no back off at the barrel shifter and the input quantization noise of approximately -172 dBFS/Hz dominates. The combination of a 16-bit input width at 61.44 MSPS and a 24 dB attenuation range constitutes a 20-bit floating point A/D system with a -197 dBFS/Hz theoretical noise floor. This is lower than the internal 20-bit noise floor in the data path when the sample rate has been lowered to 7.68MSPS by decimation.



NOTE: in both figures, the reported attenuation level does not align with the FFT display due to the delay over the USB

FIGURE 9A. INTERFERING SIGNAL AT MINIMUM LEVEL (MINIMUM ATTENUATION)

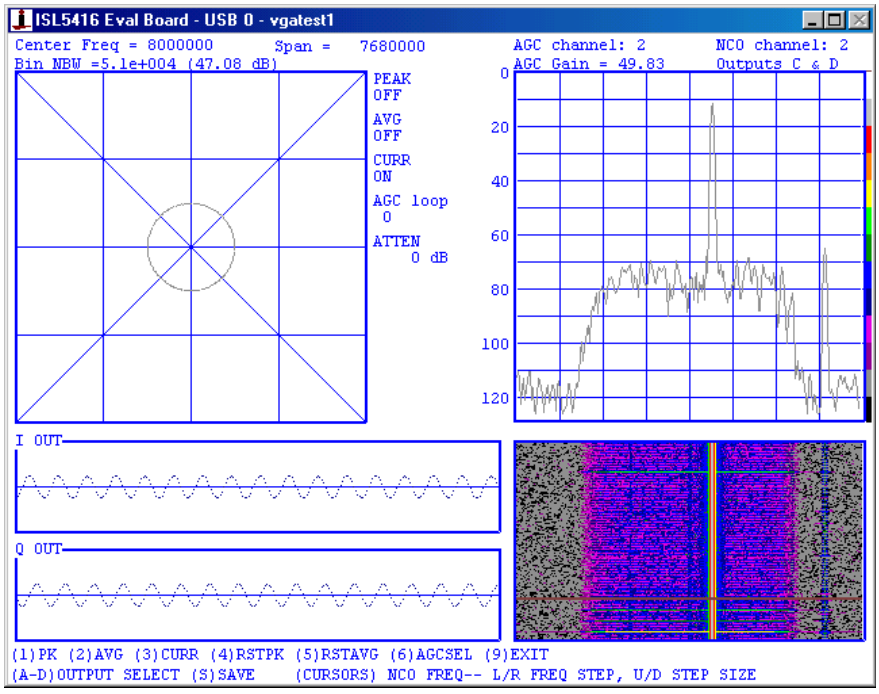


FIGURE 9B. INTERFERING SIGNAL AT MAXIMUM LEVEL (MAXIMUM ATTENUATION)

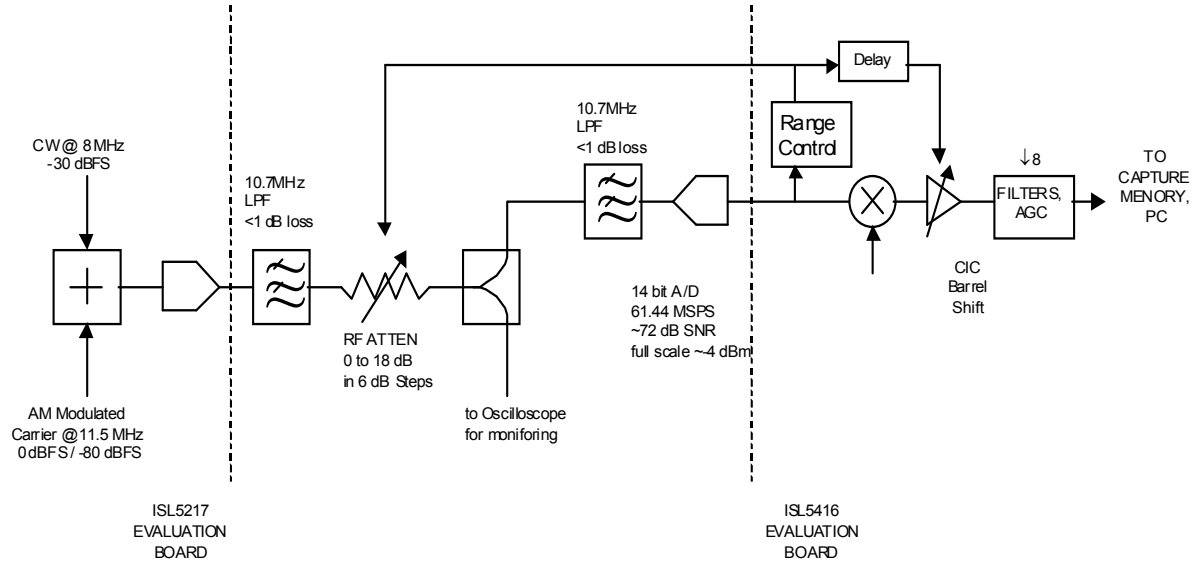


FIGURE 10. TEST CONFIGURATION 2

Case 2: Real World Components

This example replaces the digital attenuator (barrel shifter) with a D/A, A/D, digitally controlled attenuator, and low-pass filters. A block diagram for this test configuration is shown in figure 10. Because the D/A converter output does not reach the full-scale input voltage of the A/D, for these tests, the range control thresholds were reduced by 15 dB from case 1 to -19, -30, and -45 dBFS for the immediate, upper, and lower thresholds, respectively. The ISL5217 signal levels were increased to -30 dBFS and to -0.2/-80 dBFS for the signal of interest and the interferer, respectively. Appendix 2 provides more details on the settings and gain distribution for the configuration.

Figures 10A and 10B shows the I output of the ISL5416 at the arrival and departure of the interfering signal. Figures 11A and 11B shows the log of the magnitude of the ISL5416 I/Q output. The discontinuities in the display result occur at the switching points between attenuation settings. These can be caused by the attenuator not switching cleanly between steps and/or the gain discontinuity from the attenuation switching exciting the low-pass filters and spreading the attenuation change over the impulse response length of the filters. The range control RF delay is programmed to the approximate center of the filter group delay and converter delay, but the gain change at the filter output is not instantaneous and starts before and settles after the CIC barrel shift change. In a direct sequence spread spectrum system, the de-spreading process will reduce the effects of the discontinuities. In non-spread systems, aligning the range control timing to time slot boundaries may minimize the effects of discontinuities. This illustrates why it is important to minimize the number of gain changes by proper selection of the thresholds and gain steps. An attenuator at IF rather than RF can also minimize the discontinuities by reducing filter effects but this requires RF and IF components with higher compression points. The change in SNR with the change in attenuation can also be seen in the figures.

Figure 11B shows the AGC settling after the attenuator changes to compensate for the attenuator inaccuracy. The attenuator steps are not exactly 6 dB. In this example the error is about 0.25 - 0.5 dB. This is the overall non-linearity of the floating-point A/D system. The A/D converter sets the instantaneous non-linearity of the system, but the attenuator dominates the non-linearity of the system. If the attenuator adjusted every sample, the performance would be roughly equal to a 5 bit A/D.

Figures 12A and 12B are FFTs of the ISL5416 output at minimum and maximum attenuation. The sample rate is 7.68 MHz and the bin NBW is approximately 12.75 kHz (41 dB). From the displays, the C/No can be estimated to be

104 dB/Hz and 89 dB/Hz for 0 dB and 18 dB of attenuation, respectively. The spurs that appear when there is 18 dB of attenuation are approximately -93 dBFS at the A/D input and may be caused by signal leakage in the test fixture at the higher attenuation setting.

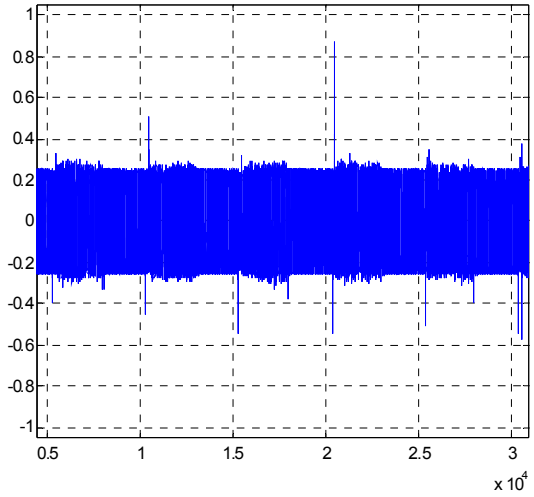


FIGURE 10A.

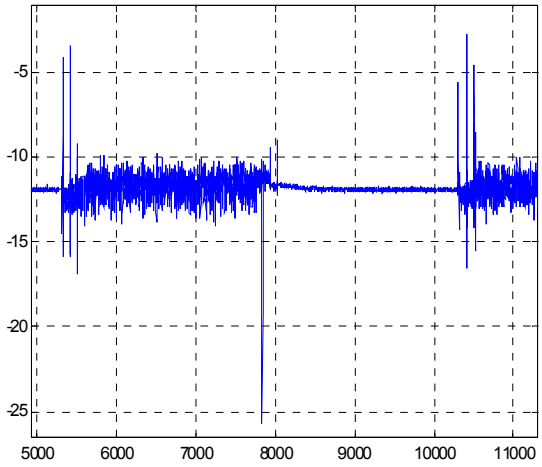


FIGURE 11A.

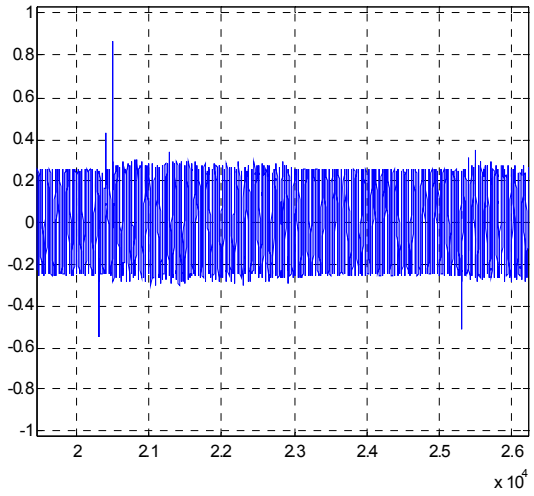


FIGURE 10B.

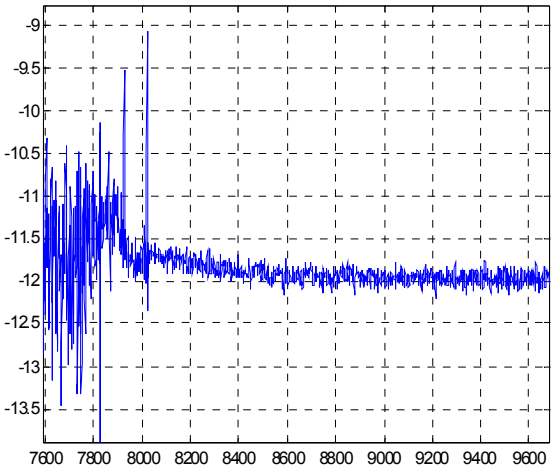


FIGURE 11B.

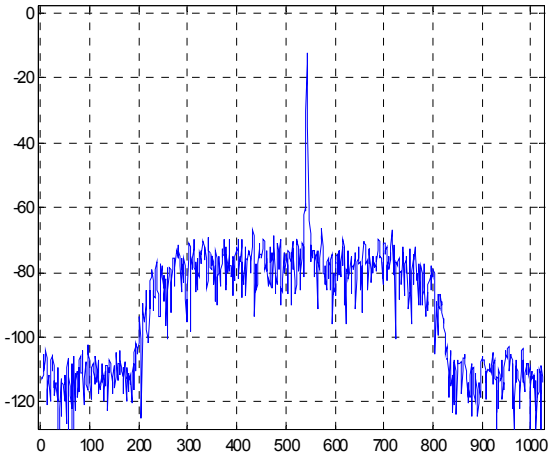


FIGURE 12A. ISL5416 OUTPUT, 1K POINT FFT, BLACKMAN WINDOW, ~1.7 BIN NBW/BIN SPACING FACTOR (0 dB ATTENUATION)

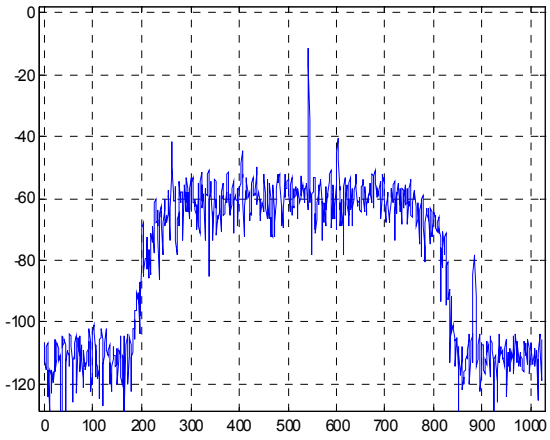


FIGURE 12B. ISL5416 OUTPUT, 1K POINT FFT, BLACKMAN WINDOW, ~1.7 BIN NBW/BIN SPACING FACTOR (18 dB ATTENUATION)

Figures 13A and 13B show the evaluation software screens at minimum and maximum attenuation. The FFT display is 256 points and the noise bandwidth of an FFT bin is shown at the upper left corner of the display. The signal of interest is -47 dBFS into the A/D converter with minimum attenuation and -65 dBFS at maximum attenuation. The converter noise floor is approximately 72 dB at 61.44MSPS or -122 dBFS per FFT bin at the A/D input. At minimum attenuation the output SNR is approximately 31 dB. At maximum attenuation it is reduced to about 16 dB. The AGC gain drops by 0.8 dB due to the attenuator inaccuracy and the extra noise in the output bandwidth.

The waterfall display shows the spectral noise floor occasionally jumps. This occurs when the samples used by the FFT include discontinuities from the attenuation change.

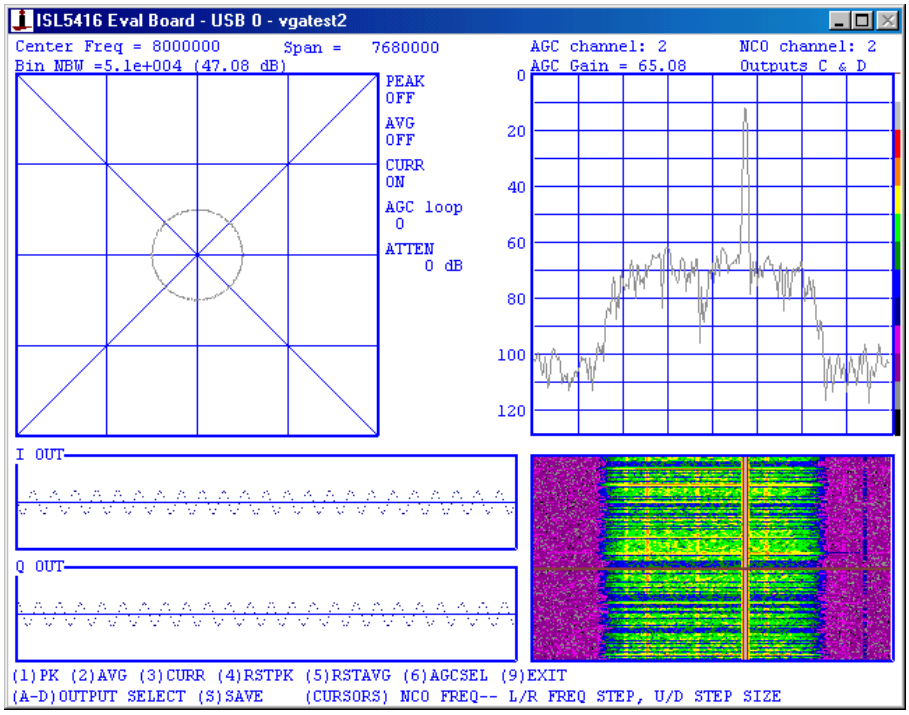
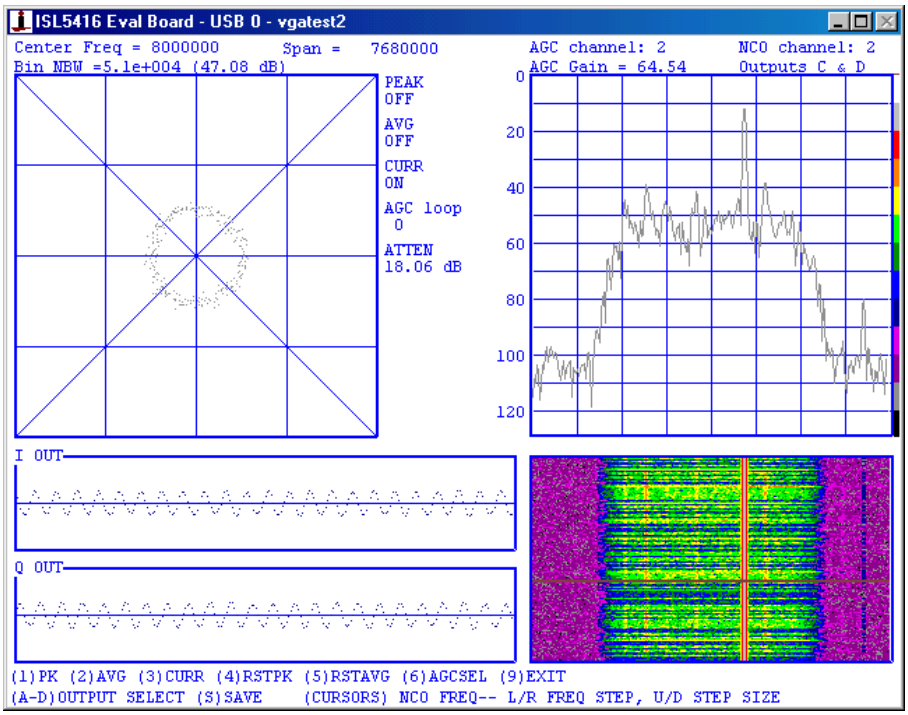


FIGURE 13A. EVALUATION BOARD SOFTWARE SCREEN (0 dB ATTENUATION)



NOTE: It is not shown by the screens that the A/D has a DC offset of -30 dBFS. The high-pass filter blocks the DC component in the averaged path. Without the high pass filter, the lower limit would never be reached and the attenuation would stay at 18 dB after the first time the interfering signal arrived (the leak term is disable in this example).

FIGURE 13B. EVALUATION BOARD SOFTWARE SCREEN (18 dB ATTENUATION)

Miscellaneous Notes on Usage and Applicatoins

Detector Use Strategies

A number of different range-control strategies are possible depending on which detectors are enabled.

1. All thresholds and the bias enabled. This mode gives the most control over the operating range and can most quickly settle to that range.
2. Only the immediate threshold and the bias are enabled. This mode takes the A/D out of saturation quickly and slowly removes attenuation using the bias until it is all removed or the immediate threshold triggers again. This mode can have the fewest attenuator adjustments, minimizing the number of discontinuities in the A/D output. This mode can also have long periods of low sensitivity while attenuation is slowly removed by the bias after the large signal that triggered the immediate threshold goes away.
3. Use only the immediate threshold and lower threshold. This mode takes the A/D out of saturation quickly and can remove attenuation when it is no longer needed more rapidly than case 2.

Threshold Setting and Disabling Detectors

The thresholds and bias can be disabled as follows:

1. Immediate threshold: set the threshold to full scale, (0 dBFS)
2. Upper threshold: set the threshold to full scale (0 dBFS)
3. Lower threshold: set the threshold to its minimum value
4. Bias: set the bias increment to zero.

The immediate threshold is usually set a few dB from full scale. If the input is expected to increase rapidly and there is a large delay from the attenuator to the A/D output, the threshold may need to be lower to reduce the time in saturation due to the delay.

The upper threshold is set based on the peak-to-average ratio of the interfering signal. For example, with noise-like signals the threshold might be set to so that A/D saturation occurs at the four standard deviations from the RMS signal. Note that the detectors operate on the average and the average magnitude of a Gaussian random variable is about 2 dB below the standard deviation. If the interfering signal is a sinusoid, the threshold might be set so that the peaks are below the immediate threshold. The RMS-to-average ratio for a sinusoid is usually around 1.11 (0.91 dB), but there are special cases at

Fs/4 and close to DC or Fs/2. At DC or Fs/2, the period of the sinusoid can be longer than the integration period for the detector. At Fs/4 the average can vary from 0.5 to 0.7071 depending on the phase.

The lower threshold is always set above the noise floor of the A/D. When the signal level drops, the lower threshold detector is used to quickly remove attenuation. This lowers the A/D noise floor relative to the RF noise floor and increases the receiver sensitivity. To quickly restore maximum sensitivity, the lower threshold should be set high, close to the upper threshold. The lower threshold can be set farther below the upper threshold to provide hysteresis in the loop.

The bias value sets the maximum time that the receiver sensitivity is reduced due to unneeded attenuation. A large bias step value will remove attenuation move quickly.

Figures 14 illustrate how the thresholds move relative to the RF power as attenuation changes. Figure 15 illustrates choosing thresholds values.

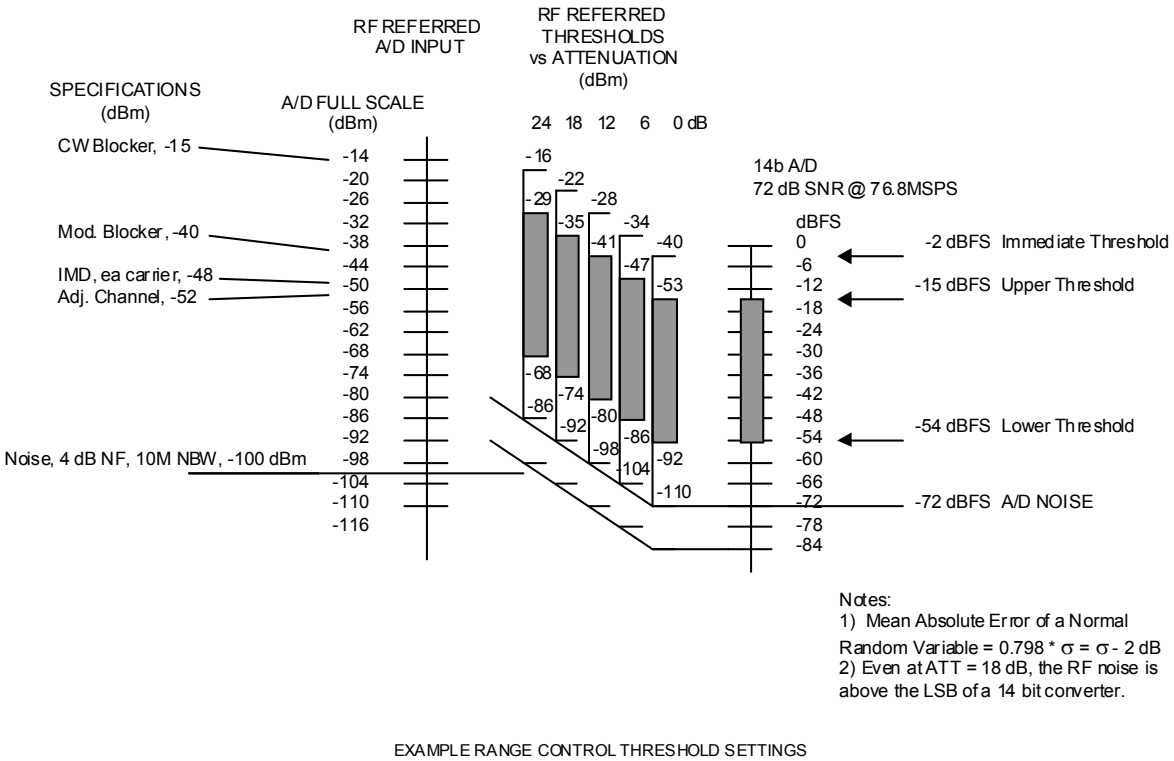
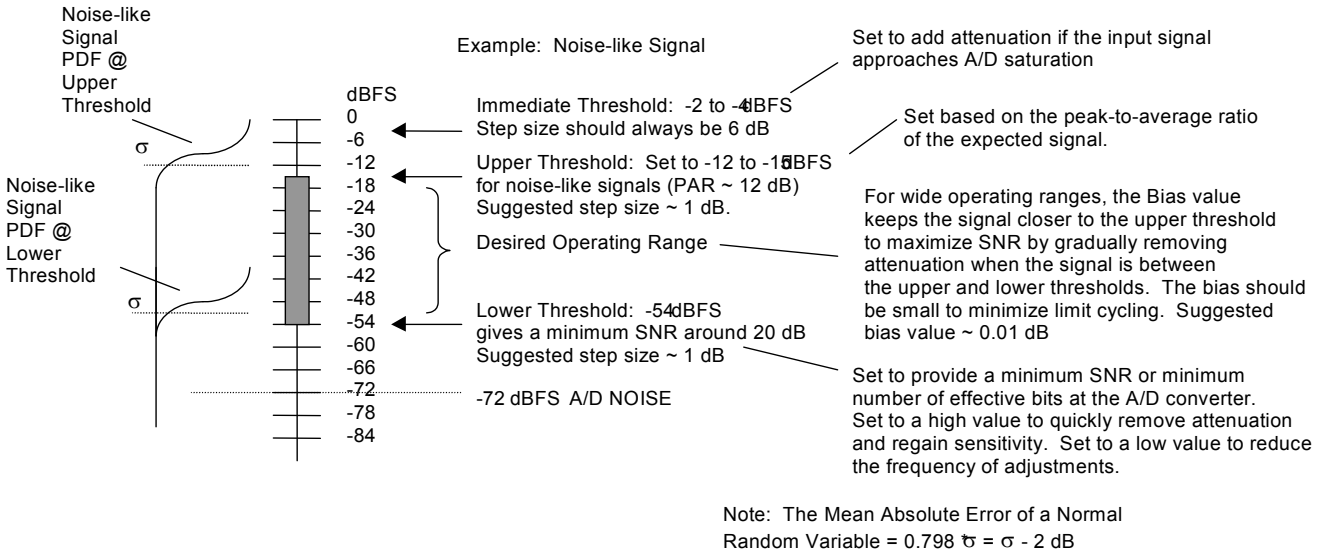


FIGURE 14. THRESHOLD MAPPING



- Integration Time: chosen to be long enough to reduce the standard deviation of the threshold comparison: $\sigma' = \sigma / \mathrm{SQRT}(N)$, and to be short enough to react to the departure of a large signal.
- The slot period must be longer than the integration time.
- Integrations/slot: integration time x integrations / slot must be less than the slot period

FIGURE 15. CHOOSING THRESHOLD VALUES

Attenuator Location

Positioning an RF attenuator before the LNA will impact the receiver noise figure nearly dB for dB as attenuation is added. Putting it after the LNA has less effect on the noise figure but allows the LNA to be overloaded. Using two attenuators-one prior to and one following the LNA can be a good compromise. Equal attenuation can be added at both points or attenuation can be first added after the LNA and only added ahead of the LNA at maximum attenuation when there is the LNA approaches compression.

System Calibration

An attenuator with gain steps smaller than 6 dB together with the extra bits in the range control look-up table can be used during system calibration to equalize the gain between receive channels. The AGC in the ISL5416 can also assist by accurately measure the difference in signal power between channels. After the gain difference between channels is measured, each look-up table can be programmed with a different set of codes to compensate.

Attenuator Options and Vendors

The choice of attenuator will on the specific application, but two sources for digital RF attenuators are M/A-COM (AT90 series GaAs FET attenuators) and Honeywell Solid State Electronic Center (HRF-AT4000 series SOI CMOS). A multiplying D/A converter may suffice at IF. A D/A converter controlling a variable-gain amplifier is another possible solution. The D/A converter would be clocked with the same clock as CLKC.

Transient Effects

In choosing components, the following will have an effect on the range control loop and should be considered.

1. **Filters**: The group delay of the filters between the attenuator and the A/D will increase the response time of the loop. The step response of the filter will show up at every attenuator change and will lengthen the gain transient seen by the A/D converter. Typically, the lower the shape factor of the filter, the longer the delay.
2. **Attenuators**: The attenuator accuracy will dominate the overall linearity of the receiver. The AGC can compensate for the error between steps, but if the AGC is used for signal power measurements, the attenuation value at each step may need to be measured at system calibration so that errors can be removed in the post processing. The attenuator settling time should be short to minimize delay in the loop, but remember that the high frequency components of fast edges can cause other problems in the receiver.
3. **A/D converters**: The pipeline delay of the A/D and the recovery time from an input step or over-range condition should be considered.

Appendices

Appendix 1 provides details on the all-digital test configuration.

Appendix 2 provides details on the test configuration using analog components.

Appendix 3 shows an example receive chain with example spreadsheet calculations for noise floor, minimum detectable signal (MDS), and output SNR for some 3GPP signal specifications.

Appendix 4 reviews the 3GPP FDD basestation receiver specifications and derives the dynamic range requirements for the A/D and DSP.

Appendix 5 is an example calculation of the digital noise contribution to the system noise.

Appendix 6 shows the relative bit weights in the range control data path.

Appendix 1

Test Configuration 1: (all digital)

Tx Configuration - ISL5217

- 61.44MHz clock
- Two transmit channels
- Main channel, CW, 8.5MHz center frequency, output level -54 dBFS
- Interferer, AM modulation, 11MHz carrier, input alternates between (0.7071, 0.7071) and (0.0001, 0.0001), 80 samples of each at a 240ksps rate
- Gaussian transmit shaping filter BT = 0.3
- Output attenuation of 6 dB
- Signal alternates between ~-6 dBFS and -83 dBFS (+48 to -29 dBc)

Gain/Attenuation Stage -- Barrel Shifter

- 24 dB gain at minimum attenuation
- Attenuation added in 6 dB steps

RX Configuration - ISL5416 (file name: vgatest1.416)

- CIC decimation of 4, 31thbf.imp filter decimating by 2, rrc64a22.imp filter decimating by 1.
- AGC enabled
- VGA RF delay = 4 clocks (pipeline delay of shifter board)
- Imm. Thresh = -2 dBFS, 6 dB change
- Upp. Thresh = -15 , 1
- Low Thresh = -30 , 1
- Bias 0.01
- Slot = 129, delay = 1, integ = 128, # integ = 1
- Upper limit = 24, Lower limit = 0

- The CIC input is backed off an extra 24 dB at the CIC barrel shifter to allow for up to 24 dB of gain.

- The AGC adds ~50 dB of gain to bring the target signal to -12 dBFS.

MINIMUM ATTENUATION

		TARGET	INTERFERER	
TX		-54	-6	-83 dBFS
GAIN	+24	-30	+18	-59 dBFS
MIXER	-6	-36	SAT	-65 dBFS
CIC SHIFT	-24	-60		-89 dBFS
AGC	+48	-12		-41 dBFS (-141*)

MAXIMUM ATTENUATION

		TARGET	INTERFERER	
TX		-54	-6	-83 dBFS
GAIN	+0	-54	-6	-83 dBFS
MIXER	-6	-60	-12	-89 dBFS
CIC SHIFT	-0	-60	-12	-89 dBFS
AGC	+48	-12	+36 (-64*)	-41 dBFS (-141*)

NOTE: *RECEIVER OUT-OF-BAND ATTENUATION ~ 100 dB

Appendix 2

Test Configuration 2 (analog components)

Signal Flow:

ISL5217 Digital Up-converter

-> HI5828 DAC, ~-5 to -6 dBm full scale

-> 10.7M LPF

-> Digital Attenuator, 6 dB steps, 2 dB min attenuation

-> Power divider (-4.5 dB gain)

-> 10.7M LPF

-> 14bit A/D, ~72 dB SNR, +4 dBm full scale

-> ISL5416 Digital Down-converter Evaluation Board

At minimum attenuation, there is approximately 17 dB of loss from the ISL5217 (digital) output to ADC/ISL5416 input.

Transmitter:

- ISL5217 Evaluation Board 61.44 MHz clock
- Channel 1: desired signal @ 8 MHz CW @ -30 dBFS at ISL5217, output -47 dBFS at A/D input (-12 dB multiplier, -18 dB (1/8) shift)
- Channel 2: interfering signal @ 11 MHz; Tx pattern - square wave AM with 77 dB modulation repeating sequence of 80 samples each of (0.7071, 0.7071) and (0.0001, 0.0001) at 240 ksps, Interpolated to 61.44 MSPS with a Gaussian interpolation FIR filter, IHBF, and high-order interpolation filter. Alternates between -0.2 and -77 dBFS at the ISL5217 output (-0.2 dB multiplier, shifter scale by 1) and -17 to -94 dBFS at the A/D input.

Receiver:

- ISL5416 Evaluation Board
- Range Control: 11 clock RF delay, -19 dBFS immediate threshold, 6 dB immedediate step, -30 dBFS upper threshold, 1 dB upper threshold step, -45 dBFS lower threshold, 1 dB lower threshold step, 0 dB leak, 128 clock integegration time, attenuation limits: 0, 24 dB
- Filtering: 5th order CIC, decimate by 4, 31 tap HBF, decimate by 2, 64 tap RRC, a=0.22 filter
- AGC: 0 to 96 dB gain range, -12 dBFS set point, 0.1 dB maximum attack, decay slew rates

Desired signal level is -47 dBFS to A/D converter w/ 0 dB attenuation and is -65 dBFS with 18 dB of attenuation.

There is 24 dB of loss in the CIC shifter due to back off to accommodate up to 24 dB of added gain (range control upper limit).

The mixing loss -6 dB because the input signal is composed of upper and lower sidebands, each at -6 dBFS and the tuner selects only one.

The desired signal is -47 - 24 - 6 = -77 dBFS at the CIC input with 0 dB attenuation, and -95 dBFS with 18 dB of attenuation.

To reach the programmed -12 dBFS set point, the AGC adds 64.4 and 65.2 of gain for 0 and 18 dB of attenuation, respectively.

SNR calculations:

The C/N for the desired signal at the output (7.68 MHz BW) with 0 dB attenuation is:

C/N= -47 dBFS - (-72 dB SNR) + (9 dB processing gain) = ~ 34 dB

(C/n_0 = -103 dBc/Hz).

The desired signal C/N at the output (7.68 MHz BW) with 18 dB attenuation is:

C/N = -65 dBFS -(-72 dB SNR) + (9 dB processing gain) = ~ 16 dB.

(C/n_0 = -87 dBc/Hz).

Appendix 3:

Example Calculations for SNR, MDS

The block diagram below shows a possible wide-band, single (analog) conversion receive chain design. There are, of course, many possible receive chain designs. The specifications listed were taken from the data sheets for the parts. The SAW filter loss is typical of low loss SAW filters and is not for any particular part number. If the LC filter is sufficiently sharp, F3 and A6 would not be needed. This architecture has not been built. The attenuators are available with a 31 range in 1 dB steps or a 15.5 dB range with 0.5 dB steps. The range control circuit would control the attenuators to step a single attenuator by 6 dB or each of two attenuators by 3 dB. The extra resolution can be used to compensate for gain variations in the other components. At system test or calibration the system gain could be measured and the attenuator codes in the ISL5416 adjusted to keep the RF/IF gain variation between systems within the resolution of the attenuator control.

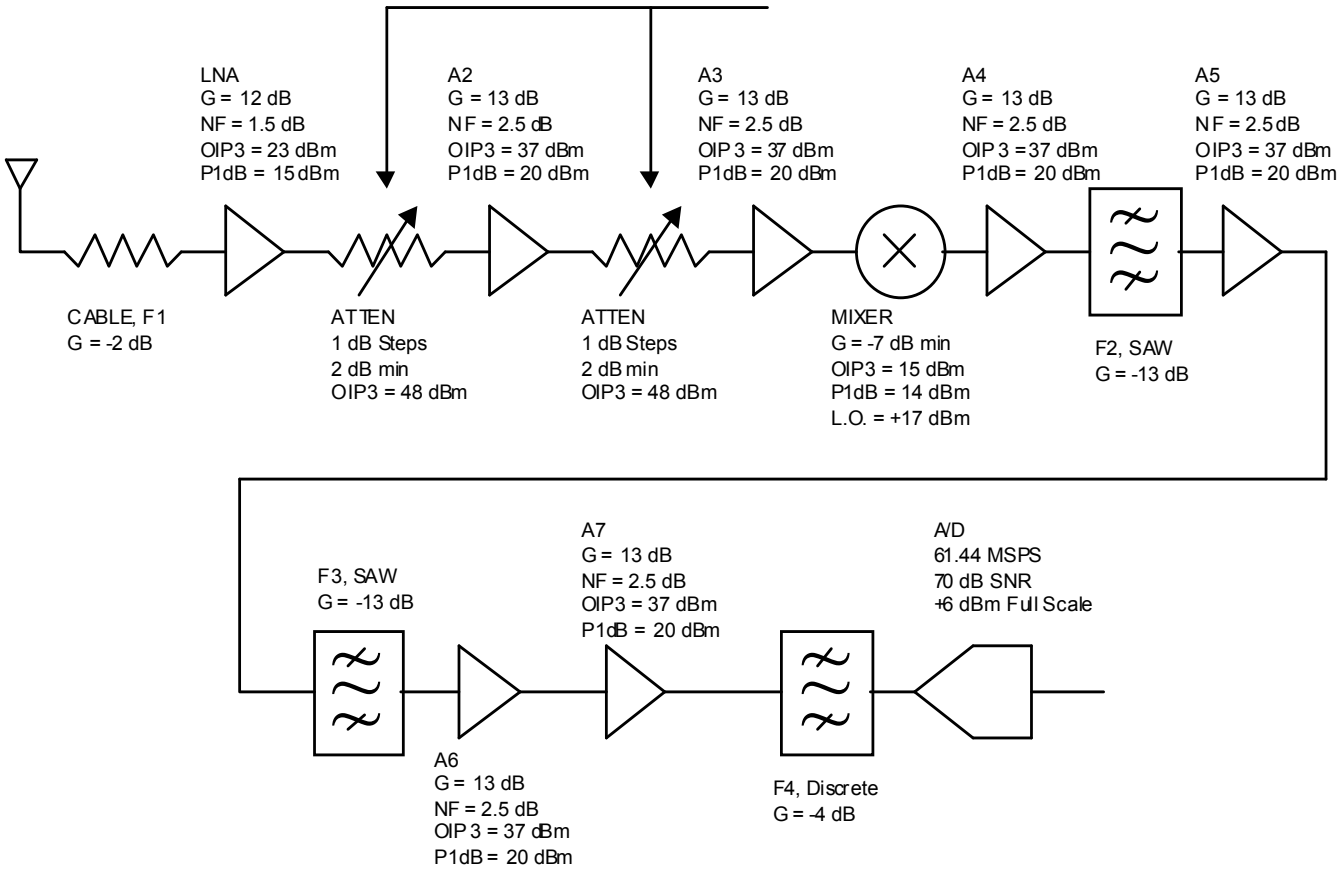


FIGURE 16. WIDE-BAND, SINGLE (ANALOG) CONVERSION RECEIVE CHAIN DESIGN

The table below shows the effects of the added attenuation on the minimum and maximum RF signal levels for the Rx chain shown. The two sets of entries show the difference in noise figure and minimum detectable signal (MDS) when using two 3 dB step attenuators, one before and one after an amplifier versus using a fixed attenuator and a single 6 dB step attenuator before an amplifier.

EFFECTS OF ADDED ATTENUATION ON THE MINIMUM AND MAXIMUM RF SIGNAL LEVELS

ADDED ATTENUATION (dB)	ATTENUATOR 1 (dB)	ATTENUATOR 2 (dB)	A/D FULL SCALE REFERRED TO THE RF (dBm)	MDS AT 5 dB Eb/No (dBm)	CASCADE NOISE FIGURE (dB)
0	2	5	-38	-123.9	4.2
6	5	8	-32	-122.6	5.5
12	8	11	-26	-119.9	8.3
18	11	14	-20	-115.5	12.6
24	14	17	-14	-110.2	17.9
0	2	5	-38	-123.9	4.2
6	8	5	-32	-122.0	6.1
12	14	5	-26	-118.2	10.0
18	20	5	-20	-112.9	15.2
24	26	5	-14	-107.12	21.0

The table below is provided for reference and lists the noise power increase from adding a second noise source versus the relative power of the second noise source.

NOISE POWER INCREASE

RELATIVE POWER (dB)	NOISE POWER INCREASE (dB)	RELATIVE POWER (dB)	NOISE POWER INCREASE (dB)
0	3.01	-10	0.41
-1	2.54	-11	0.33
-2	2.12	-12	0.27
-3	1.76	-13	0.21
-4	1.46	-14	0.17
-5	1.19	-15	0.14
-6	0.97	-16	0.11
-7	0.79	-17	0.09
-8	0.64	-18	0.07
-9	0.51	-19	0.05

Appendix 4

Calculations for 3GPP FDD Basestation RX Specifications

Review of specifications and requirements:

- Chip rate = 3.84 MCPS
- Minimum Detectable Signal (MDS) Requirement (from spec) reference sensitivity level = -121 dBm @ 12.2kbps and <0.001 BER
- In-band interference: Desired Signal: 12.2kbps, -91 dBm, spread to 3.84M; AWGN interference: -73 dBm/3.84M; SNR prior to despread = -91 - -73 = -18 dB in 3.84M NBW; Chip rate = 3.84M, Processing gain = 10*log10(2*3.84e6/12.2e3) = 28 dB (assuming filtering to 3.84M NBW before despread operation)
- SNR after despread = -91 - -73 + 28 = +10 dB in 12.2k NBW

Adjacent Channel/Blocking/IMD Specs

- Adjacent channel BER < 0.001 for a desired signal level of -115 dBm with an adjacent channel level -52 dBm (from spec.)
- Blocking level 1 -- WCDMA w/ one code -40 dBm @ 10M offset peaking of a RRC filter with a=0.22 is approximately 1.7 (4.6 dB). Desired signal is -115 dBm for interference test BER < 0.001
- Blocking level 2 -- CW -15 dBm @ 20M offset from the freq band edge (20+2.5 from the signal center freq). Desired signal is -115 dBm for interference test BER < 0.001
- IMD -- Signal 1 @ -48 dBm, +/-10MHz, CW Signal 2 @ -48 dBm, +/-20MHz, WCDMA w/ one code unless the I.F. filter bandwidth is >20M, signal 2 will be attenuated by the filter and the spec reduces to a CW signal at 10M at -48 dBm (versus -40 dBm for the 10M blocker spec.)

A/D requirements with blocking

CW blocker:

If we set the level at the A/D to handle the -15 dBm CW signal with a 1 dB backoff and we need 7 dB Eb/No for the -115 signal at a sample rate of 61.44M, if the receiver noise is A/D dominated, the A/D would need an SNR of:

Eb = -115 dBm - 10log(12.2k) = -156 dBm

No = -156 dBm - 7 dB = -163 dBm

A/D NBW = 10log(61.44e6/2) = 74.9 dB

N = -163 + 74.9 = -88.1 dBm

A/D FS = -15 dBm + 1 dB = -14 dBm

SNR = -14 - -88.1 = 74.1 dB

If more backoff is desired, the required SNR will increase accordingly.

Note that at a 20 MHz offset, the blocker should be attenuated some by the anti-aliasing filter. The amount depends on the sample rate. For example, at 61.44 MSPS, the band of interest may be 15M spanning from 7.68 to 23.04 MHz. To prevent aliasing of out of band signals, the antialias filter must provide full attenuation at 15.36 MHz from the band edge (7.68M from the DC or the folding frequency). The blocker is >20 MHz from the band edge, so it should be rejected by the anti-alias filter for bandwidths of 15.36M at 61.44 MSPS. The anti-alias filter specs will be easier at a higher sample rate such as 76.8M.

What is fully attenuated? For this test, the processing gain against a CW blocker is 25 dB. If we need 7 dB S/I after despreading, we can have the blocker at +18 dBc after filtering. This means that the anti-aliasing filter must provide 100-18=82 dB of out-of-band attenuation. If the CW blocker was seen by the A/D, this would be the SFDR requirement on the A/D.

Modulated blocker test

The modulated blocker is -40 dBm at +/-10MHz away from the signal, but it can be anywhere in the receive band. For a wide band receiver, we would assume that the desired signal could be at one end of the receive filter and the blocker at the other, i.e. we get no help from the analog filtering.

With a single code transmitted through a RRC filter with a=0.22, the peaks would be approximately 1.7 times the nominal symbol level. This is ~4.6 dB above the nominal. Repeating the calculation for A/D SNR, but allowing for the PAR:

Eb = -115 dBm - 10log(12.2k) = -156 dBm

No = -156 dBm - 7 dB = -163 dBm

A/D NBW = 10log(61.44e6/2) = 74.9 dB

N = -163 + 74.9 = -88.1 dBm

A/D FS = -40 dBm + 4.6 + 1 dB = -34.4 dBm

SNR = -34.4 - -88.1 = 53.7 dB

Any help from the I.F. filter will reduce the SNR requirement. Any additional back off from full scale will increase it.

Assuming the same 18 dB of rejection of the blocker by the despreading (it is actually closer to 21 due to the filtering to 3.84 MHz before despreading), the A/D SFDR needs to be:

-40 (blocker)

- -115 (signal)

+ 7 (desired SNR)

- 18 (processing gain)

+ 5.6 (A/D backoff

69.6 dB

Since the reference sensitivity level is only 6 dB below the signal level for the blocker tests at -121 dBm, increasing the requirements on the A/D by 6 dB could allow us to meet the specifications without an I.F. AGC if the noise is A/D dominated. However, for the reference sensitivity test, the RF noise will come into play, so the A/D specs would have to be improved by more than 6 dB to meet both the blocker and reference sensitivity tests without a variable gain element between the RF and A/D.

Adjacent Channel Interference

This is smaller than the modulated blocker, so the blocker specs are more stringent on the A/D. The adjacent channel spec can be more than one code, so the crest factor may be higher. However, the 12 dB difference in power between the modulated blocker and the adjacent channel should allow for the difference in crest factor. This specification is more of a consideration for the DSP receive processing.

IMD

The total power is less then the modulated carrier, so this should be less stringent. Also, the large frequency to signal 2 should allow the I.F. filtering to attenuate it so that the spec would typically only apply RF/IF components in the system.

If the I.F. filter allowed both signals to pass:

The two signals are each at -48 dBm. This is 8 dB lower than the modulated blocker. If these were both CW, they would have peaks 6 dB higher at -42 dBm. Since one signals is modulated, it could theoretically peak 4.7 dB higher due to filtering to -37.3 dBm. This is slightly lower than the modulated blocker test (-40 + 4.6 = -35.4 dBm).

DSP Processing requirements

Assume full scale at the A/D is -34 dBm (from the modulated blocker test w/o filter attenuation). The MDS is -121 dBm or -97 dBFS. We must filter and output this signal without adding any significant degradation. Any noise in the DSP should ideally be >10 dB below the input noise or interference to cause <0.4 dB of additional degradation or even better >20 dB below for <0.05 dB increase. Since DSP noise is the easiest noise to control, it should be insignificant in the system. If we assume no front end AGC and set the gain so that the input referred noise from the A/D is -169 dBm/Hz for the no AGC case, this is equivalent to an RF noise figure of 5 dB. With an RF noise figure of 5 dB, the total RF and A/D noise would be -166 dBm/Hz for an MDS Eb/No of 4.1 dB.

Given these assumptions, the A/D and RF noise is

-166 - (-34) = -132 dBFS/Hz.

To keep the DSP noise 20 dB below this, it must be -152 dBFS/Hz or less. If the minimum sample rate in the DSP is 2x the chip rate, then the quantization noise is spread across 3.84 MHz of bandwidth. (While complex processing paths have 2x the bandwidth of real processing to spread the noise another 3 dB, the noise in each complex arm is independent, to they add to make the net result the same as real processing.)

RF and A/D noise = -132 dBFS/Hz

DSP noise = -132 dBFS - 20 = -152 dBFS/Hz

BW = 10log10(3.84e6) = 65.8 dB

Ndsp = -152 + 65.8 = 86.2 dBFS @ 7.68 MSPS

This is the total noise from all DSP sources. The dominant noise source will usually be at the narrowest bandwidth. The others will contribute according to their bandwidths. The calculation says the minimum bit width could be as low as 15 bits at the FIR output, but to allow for any signal attenuation in the DSP processing and for any back off to allow for peaking in the filters, the bit width should probably 2-4 bits more than this or 17-19. Any additional headroom required at the A/D will increase this requirement as well. The ISL5416 provides a minimum 20 bits through the filtering to the AGC.

AGC range requirement calculations

Full scale signal into the DSP -34 dBm

RF + A/D noise -166 dBm/Hz

A/D NBW 10*log10(61.44/2) 74.9 dB

(not considering the I.F. filter

effect on RF noise)

Output NBW 10*log10(3.84e6) 65.8 dB

N into A/D -91.1 dBm

N in channel -100.2 dBm

MDS -121 dBm

DSP gain/loss and backoff 12 dB

Output backoff 12 dB

The minimum signal power in the channel will be the noise at -100.2 dBm (this will put the MDS at 21 dB below the noise and 33 dB below full scale at the output to the DSP.)

Maximum signal in the channel

Not specified, but assume that it is equal to the adjacent channel interference level at -52 dBm.

Gain needed through the DSP for a noise dominated output

max gain: minimum signal = input noise

-34 dBm full scale

- -100.2 dBm minimum signal (noise)

+ 12 dB DSP loss, backoff

- 12 dB desired output level

66.2 dB max gain needed

min gain: max signal

-34 dBm full scale

- -52 dBm max signal in channel

+ 12 dB DSP loss, backoff

- 12 dB desired output level

---

18 dB min gain needed

Minimum AGC adjustment range needed = 66.2 - 18 = 48.2 dB

Appendix 5

Digital Noise Floor Calculations with A/D Range Control

Each processing block in the data path adds quantization noise to the signal as it passes through the ISL5416. The data path was sized to minimize the degradation of the input signal to noise by these noise sources. An example calculation of the noise contributions is given below and shown pictorially in figure 17.

Assumptions:

1. A/D range control adjustment range: 18 dB
2. RF input for A/D full scale (no RF attenuation): -30 dBm (chosen to put the A/D noise 6 dB below the RF noise for an RF noise figure of 3 dB)
3. A/D sample rate: 61.44 MSPS
4. A/D SNR: 72 dB

Because the CIC shifter adds gain to compensate for RF attenuation, there is a net 18 dB of attenuation from full scale when there is no RF attenuation.

The combination of the mixer, CIC barrel shifter, and the CIC can have from 6 to 12 dB of attenuation. This is due in part to the non-power-of-two gain in the CIC that cannot be fully compensated by the shifter. There is also a 6 dB loss in the mixer because the tuner selects only the upper or lower sideband of the real input signal. After the unwanted sideband is filtered out, 6 dB of gain can be added.

Worst case A/D full scale level vs data path full scale: -24 dB (18 dB for the RF shift and max of 6 dB for uncompensated CIC gain).

Data path full scale referred to the RF input: -6 dBm

AN EXAMPLE OF THE NOISE CONTRIBUTIONS

	BITS	SAMPLE RATE (MHz)	QUANTIZATION NOISE (dBFS/Hz)**	dBm/Hz @ RF
INPUT	16 + 4*	61.44	-194	-200
L.O.	19 + 4*	61.44	-212	-218
MIXER OUTPUT	≥ 24 + 4*	61.44	-242	-248
SHIFTER OUTPUT	≥ 24	61.44	-218	-224
CIC OUTPUT	24	15.36	-212	-218
GAIN STAGE 1	20	15.36	-188	-194
FIR1 OUTPUT	24	7.68	-209	-215
GAIN STAGE 2	20	7.68	-185	-191
FIR2 OUTPUT	24	7.68	-209	-215
TOTAL				-188

NOTE: * These noise sources are prior to the shifter, so the bits of shifter backoff are added.

NOTE: ** Nq = full scale - 20*log10(#bits) 1.76 dB - 10*log10(Fs/2) + 3.01

1

The A/D noise referred to RF is:

n_o = RF_for_A/D_full_scale - $10*\log_{10}$(Fsamp/2) - A/D_SNR = -30 dBm - $10*\log_{10}$(61.44e6/2) - 72 dB = -177 dBm/Hz referred to RF.

The total ISL5416 quantization noise from above = -188 dBm/Hz referred to RF.

The input noise from the front end noise figure = -171 dBm/Hz.

The A/D noise adds about 0.97 dB to the RF front-end noise: -170.03 dBm/Hz.

The ISL5416 adds an additional 0.07 dB to bring it to: -169.96 dBm/Hz

Increasing the attenuator range to 24 dB would bring it to: -169.76 dBm/Hz due to the 6 dB increase in the ISL5416 noise floor.

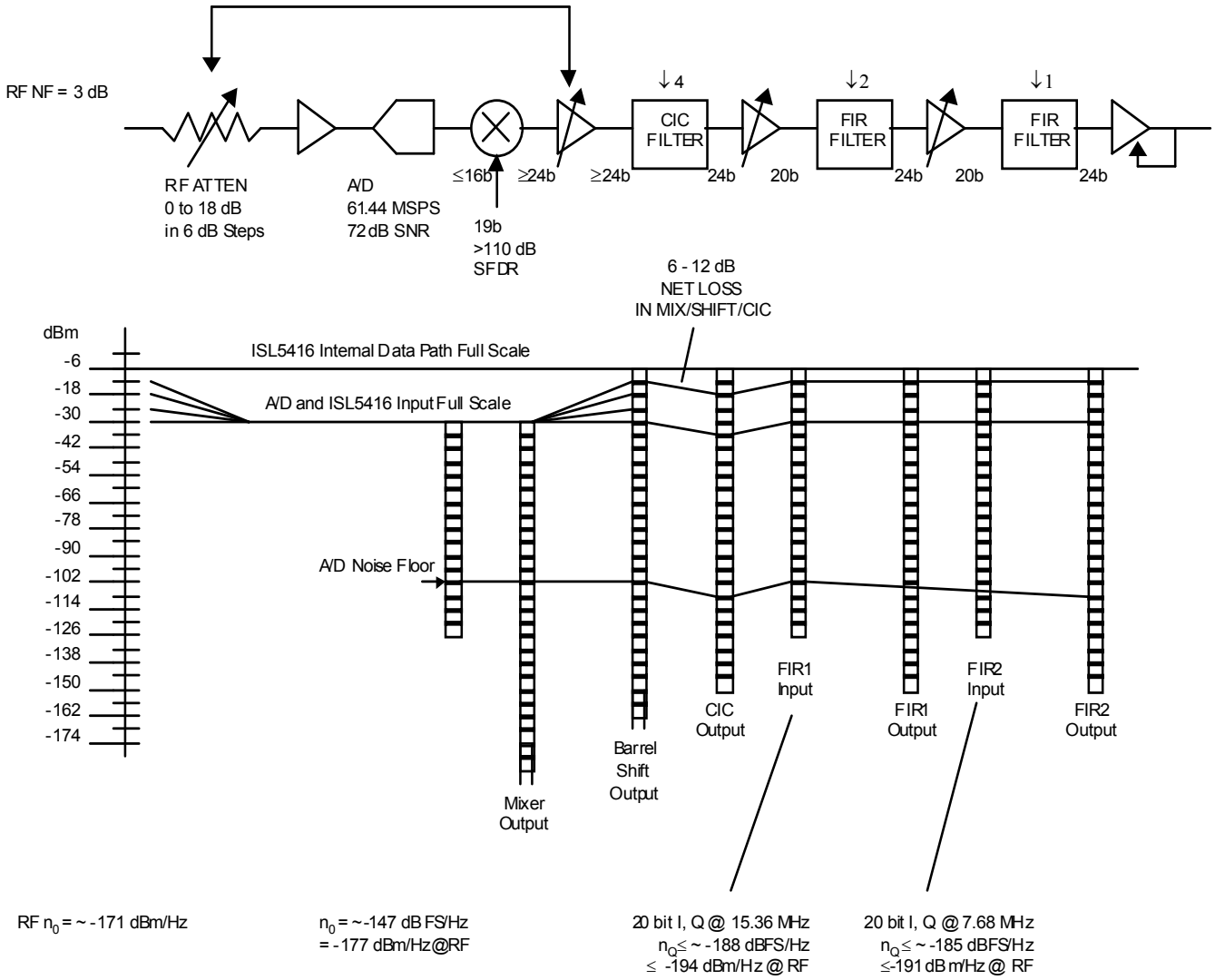
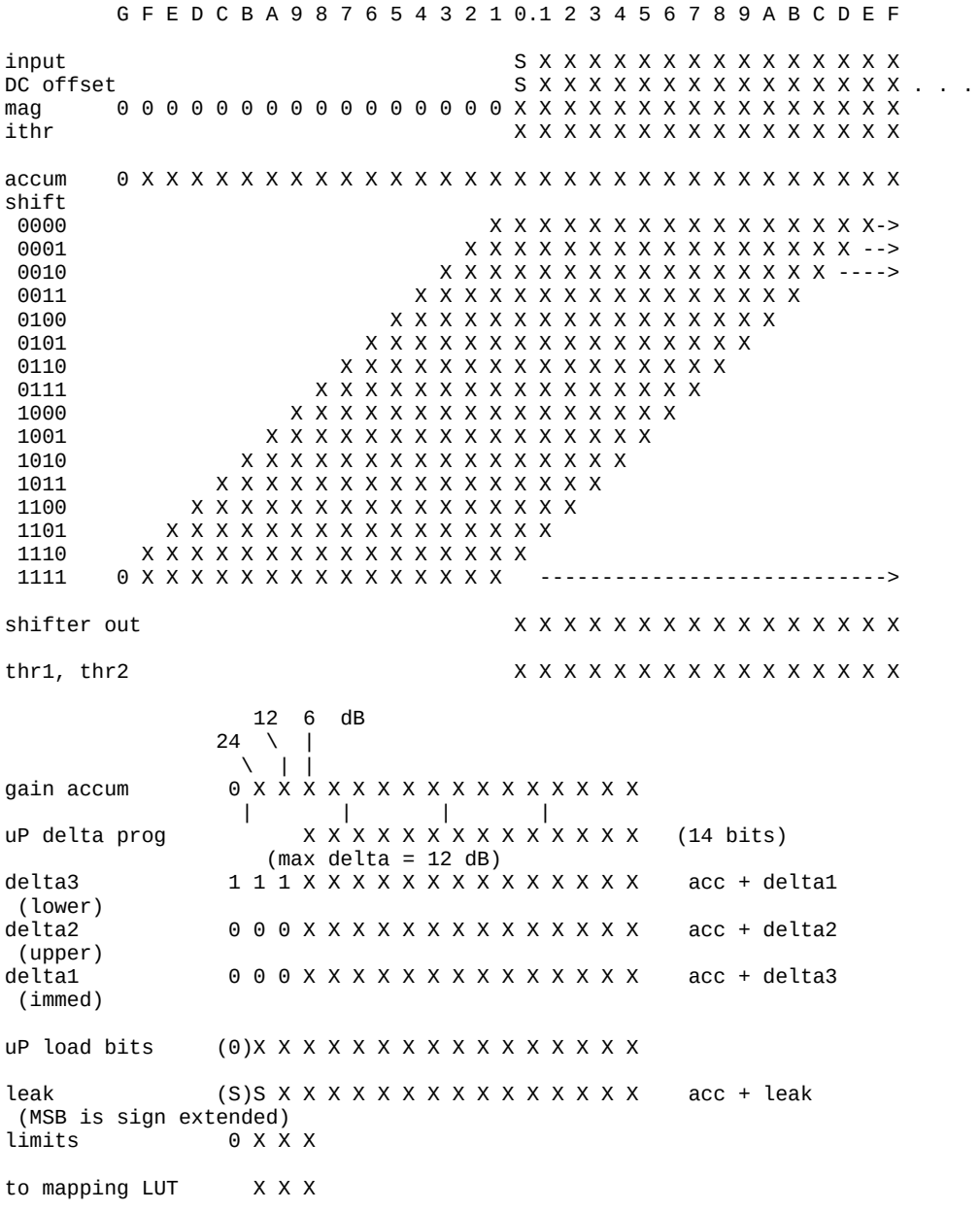


FIGURE 17. NOISE FLOOR CONTRIBUTIONS

Appendix 6 - Range Control Data Path Bit Weighting



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