Compendium of Application Circuits for Renesas Digitally-Controlled (XDCP) Potentiometers

Introduction

This application note (AN1145) lists a number of application circuits for Renesas' digitally-controlled (XDCP) potentiometers. The application circuits illustrate the wide variety of possible functions which can be implemented using the variability of the potentiometer in conjunction with standard active devices like operational amplifiers and comparators. The types of circuits include control circuits, converters, filters, signal processing circuits, regulators, wave shapers, analog computing circuits and signal sources. The circuits are shown in basic form and do not include supply decoupling or proper grounding techniques. The user must account for these in the final design.

Renesas' potentiometers are controlled through the 2-wire, I^2C, 3-wire, or SPI computer serial-interfaces or buses. For front panel, push-button type applications, Renesas' push-pots are recommended.

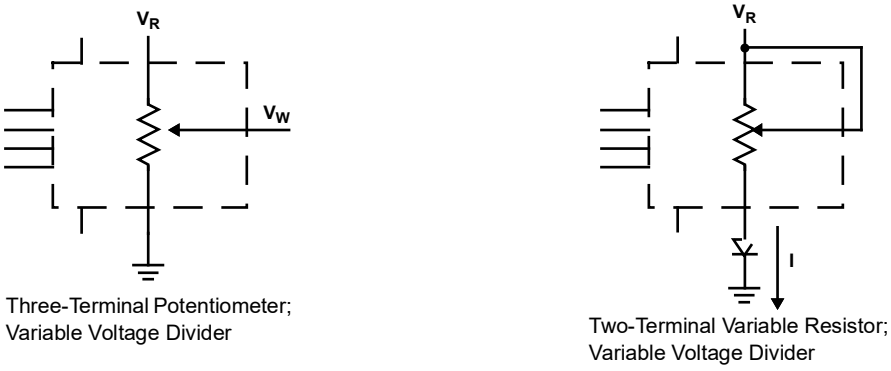
Electronic digitally-controlled (XDCP) potentiometers provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer.
2. The flexibility of computer-based digital controls.
3. The retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

In addition, the packages of the potentiometers are completely compatible with other electronic components and, therefore, reduce manufacturing assembly costs.

Contents

1. Applications



Three-Terminal Potentiometer;
Variable Voltage Divider

Two-Terminal Variable Resistor;
Variable Voltage Divider

Figure 1. Basic Configurations of Electronic Potentiometers

2. Application Circuits

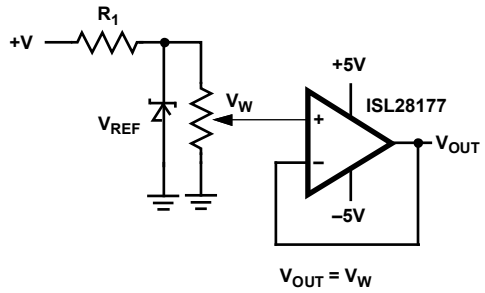


Figure 2. Buffered Reference Voltage

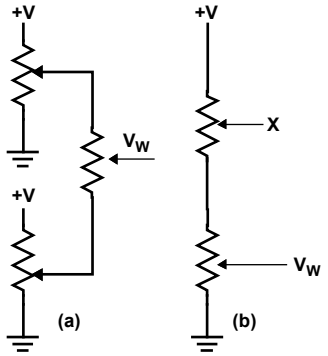


Figure 3. Cascading Techniques

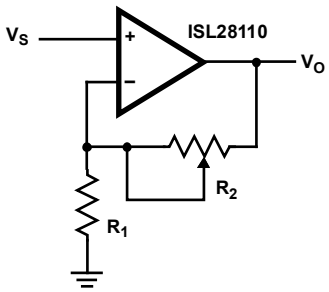


Figure 4. Non-Inverting Amplifier

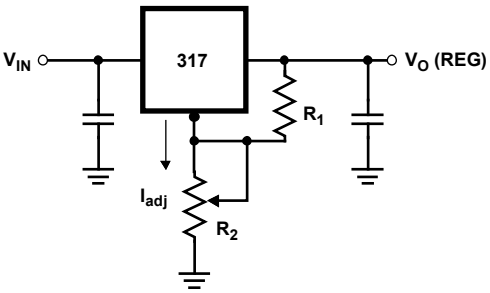


Figure 5. Voltage Regulator

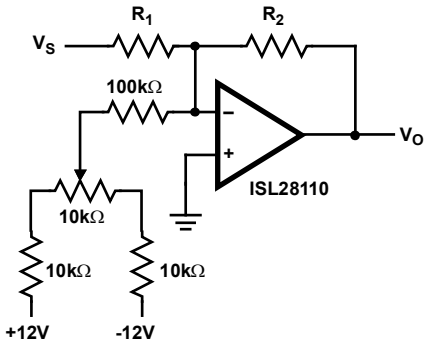


Figure 6. Offset Voltage Adjustment

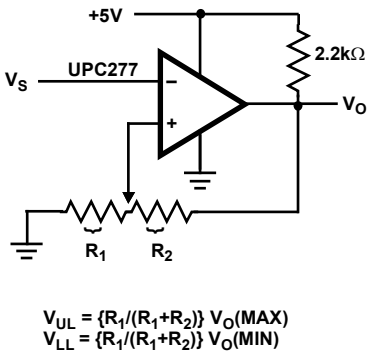
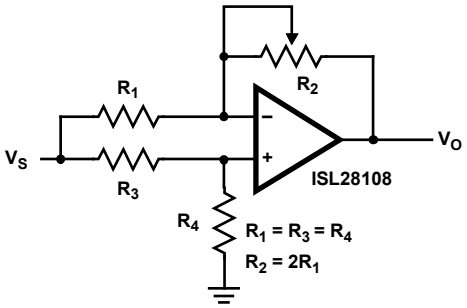
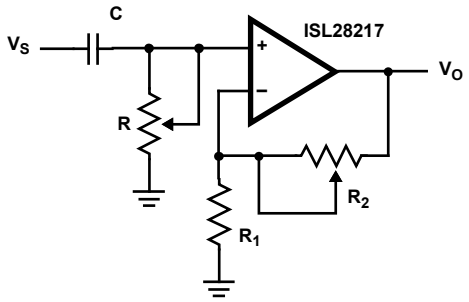


Figure 7. Comparator with Hysteresis



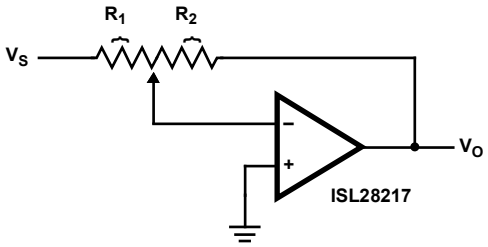
$V_O = G\ V_S$
$-1/2 \le G \le +1/2$

Figure 8. Attenuator



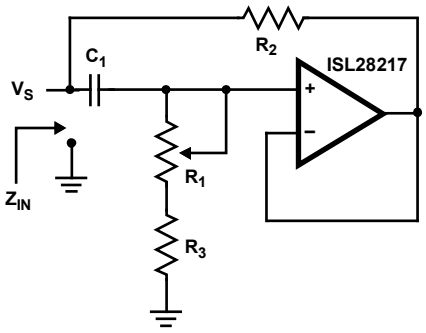
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

Figure 9. Filter



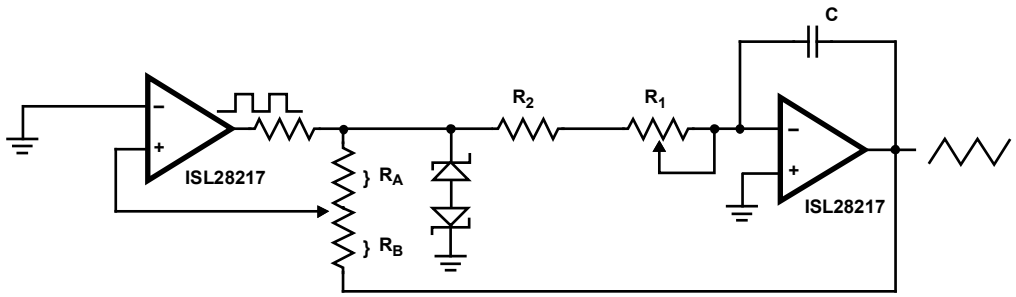
$V_O = G\ V_S$
$G = -R_2/R_1$

Figure 10. Inverting Amplifier



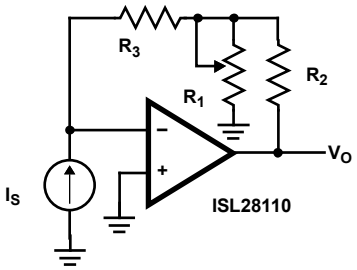
$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

Figure 11. Equivalent L-R Circuit



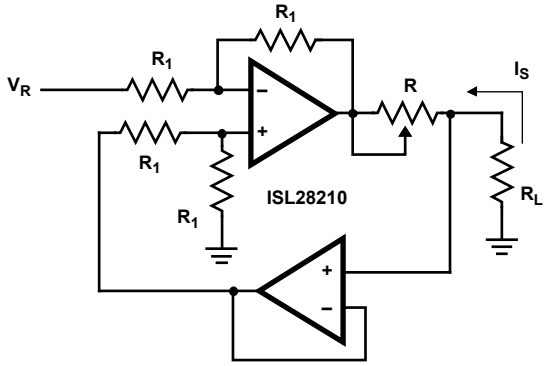
FREQUENCY $\propto R_1, R_2, C$
AMPLITUDE $\propto R_A, R_B$

Figure 12. Function Generator



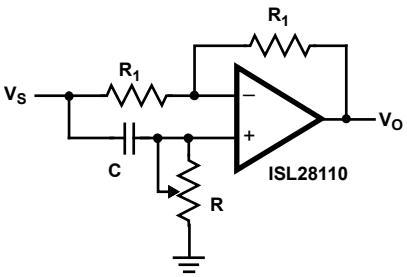
$V_O / I_S = -R_3(1+R_2/R_1) + R_2$

Figure 13. I to V Converter



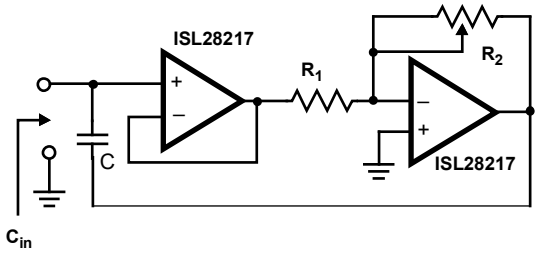
$I_S = V_R/R$

Figure 14. Current Source



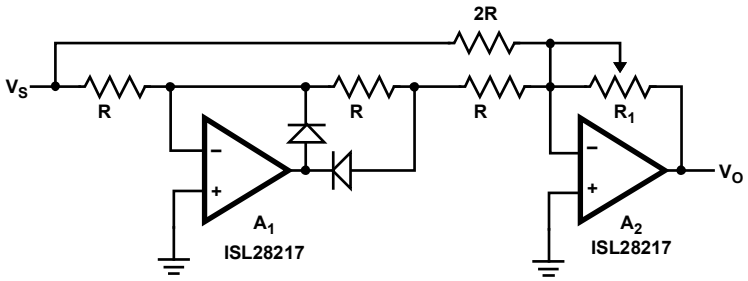
$\angle V_O/V_S = 180° - 2\tan^{-1}\omega RC$

Figure 15. Phase Shifter



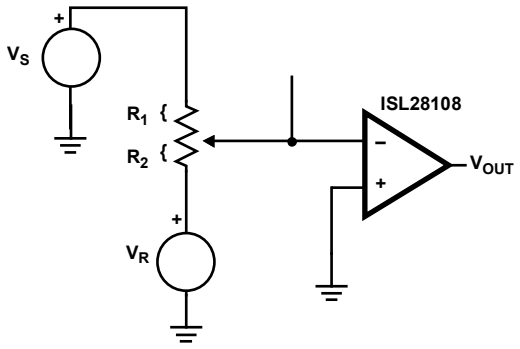
$C_{IN} = C (1 + R_2/R_1)$

Figure 16. Capacitance Multiplier



$V_O = |V_S| \frac{R_1}{R}$

Figure 17. Absolute Value Amplifier with Gain

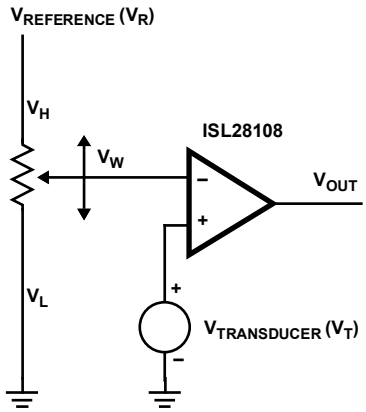


V_{OUT} = HIGH FOR $V_S \leq \frac{R_1}{R_2} V_R$

V_{OUT} = LOW FOR $V_S \geq \frac{R_1}{R_2} V_R$

$R_1 + R_2 = R_{POT}$

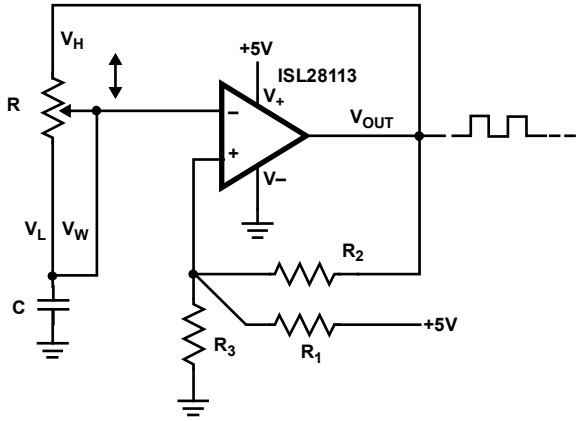
Figure 18. Level Detector



$V_T > V_W$, V_{OUT} = HIGH

$V_T < V_W$, V_{OUT} = LOW

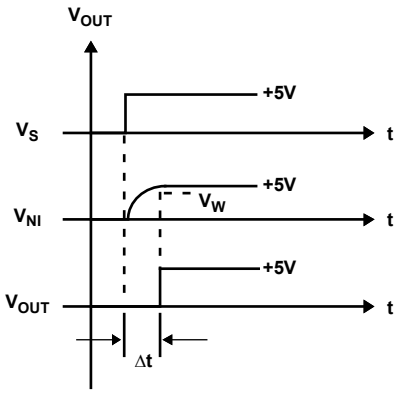
Figure 19. Level Detector



Frequency ∝ R, C

Duty Cycle ∝ R_1, R_2, R_3

Figure 20. Oscillator



$$\Delta t = RC\ln\left(\frac{5V}{5V - V_W}\right)$$

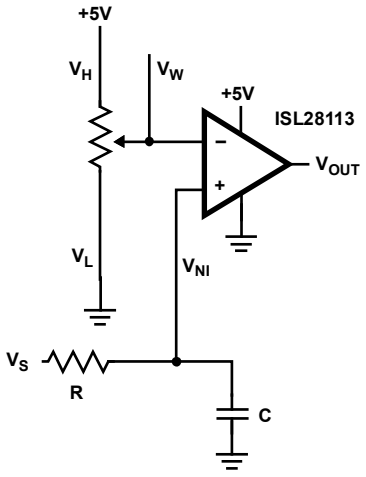


Figure 21. Time Delay

3. Revision History

Revision	Date	Description
2.00	Aug 4, 2026	▪ Updated Figure 7 ▪ Updated part numbers in Figure 9, Figure 10, and Figure 11 ▪ Reformatted document to the latest template
1.00	Jan 9, 2013	Updated the circuits that involve op amps to reflect Intersil parts.
0.00	Apr 27, 2005	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.