

Using Renesas Digitally Controlled Potentiometers in Commercial RF Power Amplifier Applications

Introduction

Traditional techniques for setting bias conditions on RF power amplifiers use either an unreliable mechanical potentiometer or an 8-bit DAC. Mechanical potentiometers reduce system reliability and adversely affect MTBF calculations. An 8-bit DAC increases cost because the application does not require the full performance capabilities of the DAC.

An XDCP (Renesas digitally controlled potentiometer) provides a cost-effective and reliable method for setting the bias conditions of RF power amplifiers. This capability is particularly useful in demanding applications such as cellular base stations that use high-linearity, high-efficiency LDMOS technology.

The XDCP provides the reliability, programmability, and cost characteristics required for this application.

Current-generation XDCPs do not contain charge pumps. Therefore, the wiper does not introduce additional noise during programming. The XDCP can be dynamically reprogrammed while maintaining continuous-wave (CW) power to the amplifier because the wiper resistance transitions smoothly between the previous and new settings. This capability enables amplifiers that support different modulation standards to be rebiasd for the operating point required for optimum performance.

XDCPs have accumulated millions of hours of reliable operation in commercial power amplifiers (PAs) installed in communication networks worldwide.

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1. Power Amplifier Overview – Architectures and Applications

Power amplifier design requires consideration of several key parameters. These parameters include output power, efficiency, linearity, and bandwidth. Together, these parameters determine the amplifier operating class and circuit technology.

The operating class specifies the conduction angle of the MOS amplifier (Table 1), which is the portion of the input signal that is amplified. The gate voltage sets the conduction angle.

Table 1. Power Amplifier Classes, Conduction Angles, and Theoretical Maximum Efficiency

Class	Conduction Angle (θ)	Theoretical Maximum Efficiency
A	360	50
AB	$180 < \theta < 360$	50–78.5
B	180	78.5
C	$\theta < 180$	>78.5

Other classes of operation are possible, although the spectrum of available efficiencies is adequately illustrated with the previous examples. It is important to understand that linearity and efficiency are inversely related.

The choice of circuit technology is evolving. For frequencies below 2.5GHz and output power above 1W, LDMOS is commonly used. Gallium arsenide (GaAs) and bipolar technologies are popular for this combination of power and frequency, but cannot match the salient characteristics of LDMOS. An LDMOS transistor biased class AB gives a better linearity/efficiency characteristic than both GaAs and bipolar formats even when the latter are biased class A.

Amplifier architecture depends on the application requirements. The amplifier specification dictates the choice. There are three options; single-ended, balanced, and push-pull. The simplest of these is the single-ended amplifier.

Single-ended amplifiers consist of a single high-power transistor, and present the greatest design challenge, and as stand alone amplifiers have the greatest susceptibility to reverse inter-modulation. It is difficult to design a high-power amplifier that has good VSWR while achieving the required output power, efficiency, and linearity. Poor VSWR causes degraded or non-optimum performance from an amplifier chain. Out-of-band uncontrolled VSWR can cause oscillations.

Single-ended amplifiers represent the best solution in terms of PCB real estate and power transistor costs (cost per watt). A 60W amplifier constructed from a single 60W transistor occupies less than one half of the real estate of an amplifier using 2 x 30W transistors operating balanced or push-pull. The component costs to generate a unit of power are lower for the single-ended case.

Applications with stringent space and cost constraints dictate the use of single-ended amplifiers.

The next architecture is the balanced amplifier, it uses two transistors operating with a conduction angle offset of 90° between them. This option has several advantages.

The most important is the isolation that the 3dB 90° hybrid offers from (and to) the RF subsystems both upstream and downstream. The isolated port transfers and terminates common mode reflections caused by poor VSWR from the transistor and its matching network. Therefore, this reduces the amount of reflected power from the input and output ports that can cause integration problems.

Two transistors share the overall output power requirement. From a thermal management point of view, the waste heat generated can be spread across a larger area.

The number of transistors operating in a balanced amplifier configuration can be more than two. It is possible to balance 2n transistors using a network of 3dB 90° hybrids. This is a common method to achieve high-output-power levels without the use of large transistors while improving the degree of redundancy (continued operation if one transistor fails).

The illustration in [Figure 1](#) shows a (3dB 90°) splitter hybrid at the input, two gain blocks, and a combiner hybrid at the output. The system impedance terminates the diagonally opposite ports.

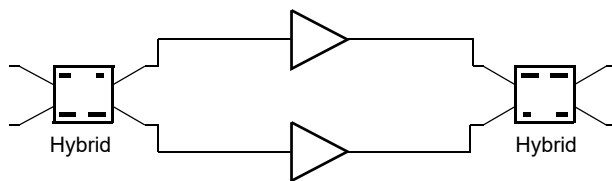


Figure 1. Balanced Power Amplifier Architecture

Independent signals apply to each port in applications where it is possible to trade off inter-modulation performance for redundancy. Both amplifiers amplify the signals, then the output hybrid separates them into their original components.

Multistage amplifiers use the balanced amplifier, or in other applications where it is important to present low VSWR to adjacent stages in order to prevent the problems noted previously. It offers improved isolation against reverse inter-modulation distortion over the single-ended option.

A push-pull amplifier uses two transistors with conduction angles offset by 180°. This architecture is used in high-efficiency, high-power applications, such as constant-envelope FM transmission.

The even harmonic rejection is the main advantage of the push-pull configuration, and the ease with which large impedance transformations can be achieved, as the balun transformer steps the impedance. With the balanced amplifier, two transistors share the workload between them, therefore the job of thermal management is easier.

The introduction of surface mount balun transformers (well-suited to automated production methods) increase the popularity of this architecture, and the balun realizes lengths of hand-soldered coaxial cable that are not suited for commercial applications, greatly increasing production labor costs ([Figure 2](#)).

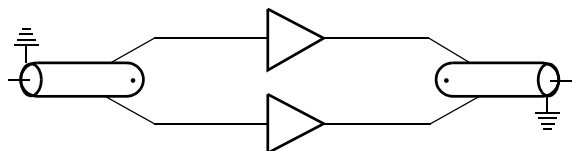


Figure 2. Push-Pull Power Amplifier Architecture

High-efficiency (constant envelope) applications use push-pull architecture. FM transmission offers improved isolation against reverse inter-modulation distortion over the single-ended option to improve harmonic performance.

2. Biasing Issues

The biasing network is one of the most important aspects of the power amplifier (PA). The bias network must reject the RF power using high-impedance sources where possible. To maintain a good decoupling regime use low-impedance sources and maximize the transistor's performance.

Use a low impedance bias supply at the FET drain (GaAs or LDMOS). For transistors not biased class A, the current versus output power characteristic is dynamic, and any residual power supply impedance causes amplitude modulation of the drain voltage.

Most commercial power amplifiers have a bandwidth typically of a maximum 10%. This allows drain current to be supplied through an RF shorted quarter-wave section (transforms to an open circuit at the feed point). Use a lumped inductor to feed bias to the drain for wide-band applications (octave plus).

The bias voltage feeds onto the transistor gate matching network via a surface mount resistor. The resistance is a few hundred ohms to ensure that minimal RF power leaks through the resistor into the biasing network. As the gate is extremely high impedance and therefore the current requirement is negligible, use the smallest package size readily available (typically 0603) to reduce the effect of any package parasitic resonance, maximizing stability and performance.

Use a simple analog compensation scheme or a DSP to control the XDCP for thermal compensation on LDMOS application. The gate voltage change with respect to temperature (for constant drain current) is around $-2\text{mV}/^\circ\text{K}$. The compensation constant is different to this to maintain a constant gain versus temperature response.

The biasing (quiescent current) requirement varies between applications, but for a typical single carrier power amplifier (SCPA) single carrier power amplifier, a quiescent current tuning resolution of 1% of I_{dq_opt} is required. To achieve this, use an 8-bit XDCP, X9258T or X9250T with 256 wiper positions.

Table 2. XDCP Resolution Requirements by Power Amplifier Application^[1]

Application	Resolution
MCPA (Multi Carrier Power Amplifier)	8-bit or 2 x 6-bit
Large Dynamic Conduction Angle Variation	2 x 6-bit
SCPA (Single Carrier Amplifier)	6-bit or 8-bit

1. I_{dq_opt} is the typical bias condition, which offers maximum dynamic gain flatness and almost optimum two-tone third order intermodulation distortion when a device is biased class AB.

Multicarrier power amplifier (MCPA) requires finer bias control or greater dynamic range to optimize dynamic gain flatness. To change the bias class (conduction angle) completely, from A through AB to B and beyond, use two XDCPs and a weighted summing network at the op-amp (Figure 3). Two combined 6-bit (64 positions) XDCPs achieve 12-bit (4096 positions) resolution.

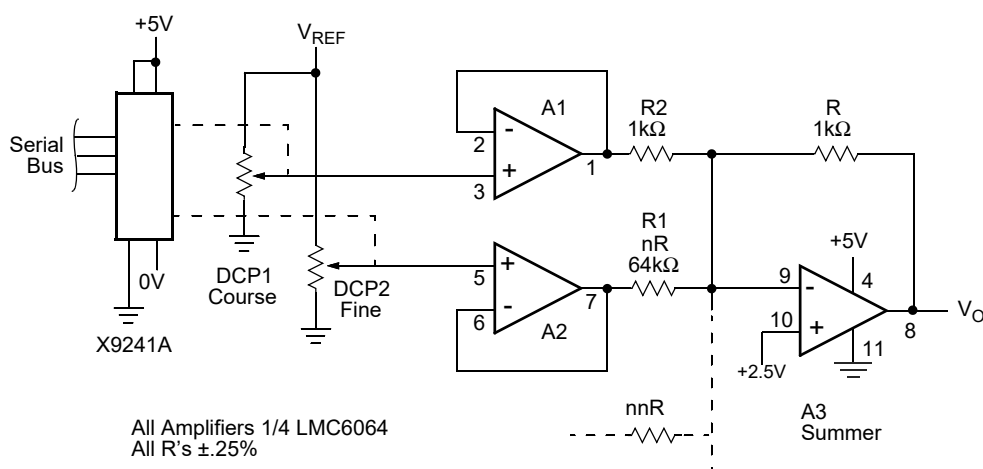


Figure 3. High-Resolution LDMOS Bias Control Using Two XDCPs

To achieve a dividing resolution of more than 4000 wiper positions, select the ratio $R1/R2$ to be the same as the number of tap points (in this case 6-bits = 64 positions). This arrangement is adequate to provide high-resolution biasing of LDMOS devices, while giving maximum flexibility to bias the transistor in any class of operation.

The X9250 8-bit potentiometer gives the required voltage resolution, especially when the range of voltage outputs is conditioned. This is accomplished by selecting upper and lower limits for the high and low-side of the potentiometer. Additionally, the op-amp buffer allows further flexibility for range adjustment and the introduction of an offset.

An LDMOS transistor requires a change of approximately 2.5mV in gate voltage to effect a 1% change in drain current (gradient of the linear region on [Figure 4](#)). Use a single 8-bit potentiometer to tune over a range of 0.6V with 1% resolution. Use the 2 x 6-bit potentiometer example to give the potential for 1% resolution over a 5V range.

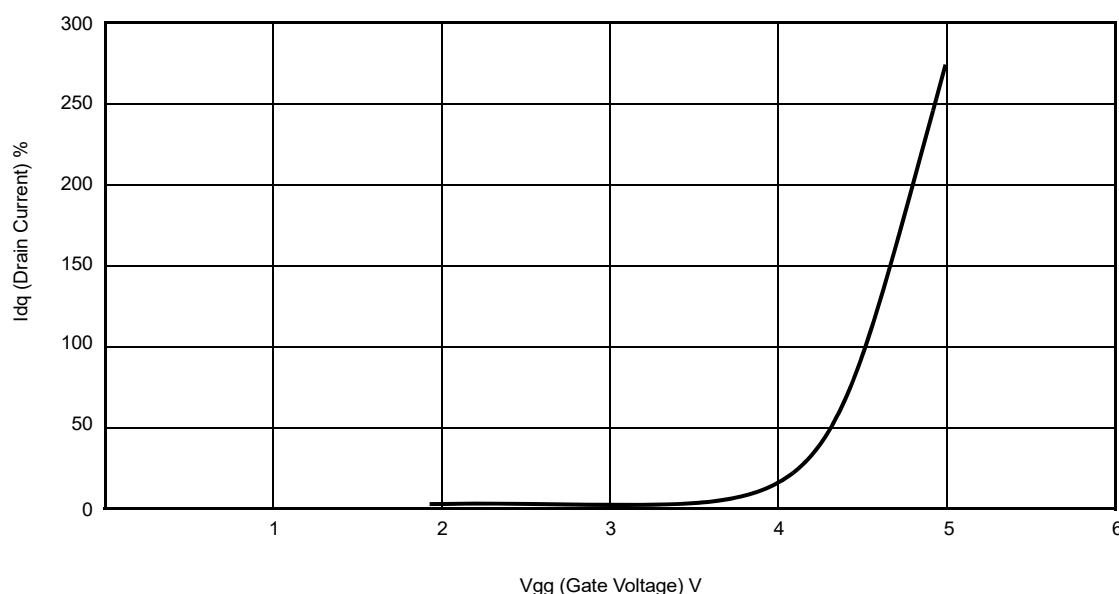


Figure 4. LDMOS Drain Current vs. Gate Voltage

On-chip memory is another feature incorporated in most of the XDCP range. This allows the designer to load a set of four values for each potentiometer, which assigns the memory register dynamically to the potentiometer at any point in time.

Using the on-chip memory is optional; settings can instead be stored and controlled by an external processor memory. Reloading new values to the wiper register does not result in any spurious noise at the wiper. This allows the PA bias to be reprogrammed dynamically while setting while hot with RF power, with no detrimental (or even detectable) effect.

This is the worst time possible to change bias conditions on the transistor, as spikes on the bias supply could result in large amounts of current drawn by the transistor, enhanced by the RF power, with possibly terminal consequences.

The memory settings are most likely to be utilized for many power amplifier design features.

- Digital thermal compensation
 - The system microcontroller monitors the thermal conditions. The controller uses a lookup table or algorithm to calculate the best operating point for the transistor. A preset list of discrete values is loaded into the memory at production time, and into the wiper register when necessary.
- V_g/I_d drift compensation
 - LDMOS transistors suffer from performance drift over time ([Figure 5](#)). To maintain a given drain current requires an increase in gate voltage. LDMOS processes are refined continually, and current drift figures are typically 5% over 20 years. Most of this drift occurs during the factory testing, which effectively burns in the device before delivery. The drift is proportional to the process cutoff frequency.

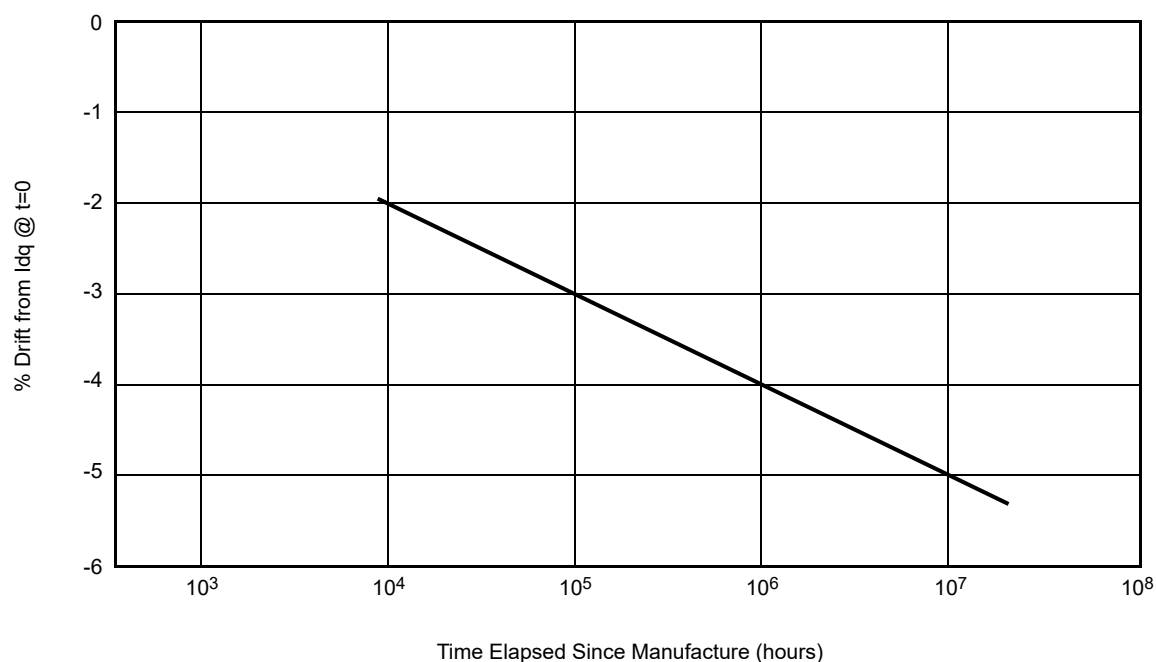


Figure 5. LDMOS Performance Drift Over Time

3. PCB Layout/Configuration and Production Interface

The PCB layout is sourced from Renesas.

4. Other RF Applications: An Example

Other RF applications use the XDCP. The vector modulator is a good example. The vector modulator manipulates an arbitrary signal, allowing the variation and control of the amplitude and phase. It is a popular method for complex gain adjustment in linearized amplifier systems, including both feed forward and predistortion.

The vector modulator consists of a 3dB 90degree hybrid, an in-phase combiner, and two variable attenuators, realized either with a pair of mixers or two further 3dB 90° hybrids with diodes. The analysis of the vector modulator is straightforward.

The XDCP provides the same advantages over a DAC in vector modulator applications as in power amplifier applications. The vector modulator demonstrates another RF application for the XDCP

5. Summary

The XDCP provides the reliability and flexibility of a DAC at a cost comparable to a mechanical potentiometer.

The software interface supports prototyping of a dynamic programming environment with minimal hardware.

The flexibility of the XDCP also supports applications in PA peripheral and control circuitry beyond transistor biasing. The XDCP can replace a DAC in cost-sensitive RF subsystems.

6. Glossary

XDCP – Renesas Digital Controlled Potentiometer; a component that obsoletes mechanical potentiometers and enhances dynamic circuit control.

DAC – Digital to Analog Converter; generates an output voltage proportional to a digital word.

LDMOS – Laterally Diffused MOS; A new semiconductor technology in the commercial RF Power market. Has much better operating characteristics than bipolar and other FET technologies, and the first choice technology in power amplifier applications up to 2.5GHz.

CW – Continuous Wave; describe a signal operating at a constant power/envelope (such as FM radio transmission), describe an amplifiers ability to handle a continuous high power signal.

PEP – Peak Envelope Power; a PEP signal a signal envelope whose amplitude changes with time, and is usually described by a peak to mean ratio.

VSWR – Voltage Standing Wave Ratio; when a signal is incident on a boundary/discontinuity, an amount of the signal reflects and interferes with the incident signal to create a standing wave (the sum of two waves traveling in opposite directions).

SCPA – Single Carrier Power Amplifier; a power amplifier used to boost the signal level of a single signal (although many signals maybe transmitted through a SCPA when multiplexed in the time domain). A SCPA is less efficient and cost effective than a MCPA.

MCPA – Multi Carrier Power Amplifier; a power amplifier to boost the level of several channels simultaneously. Inter-modulation distortion is the limiting factor in the implementation of MCPA subsystems, especially for the GSM standard.

X9250T = 256 steps, Quad, SPI, Low noise/power.

X9258T = 256 steps, Quad, IIC, Low noise/power

7. Revision History

Revision	Date	Description
1.00	Oct 22, 2026	▪ Applied latest template ▪ Added Revision History section
0.00	May 5, 2005	Initial release

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