Introduction

The ISL1561 is a fixed gain dual port class-G differential amplifier design for driving ADSL2+ and VDSL2 at reduced power consumption, compared to class AB amplifiers. The line driver operates on a single +12V to +14V supply and will generate a higher supply voltage when boosting is detected. The quiescent current can be programmed with a 12-bit command through the 3 pin serial port interface (SPI).

Highlights

The ISL1561 is Intersil's most efficient dual port line driver for ADSL2+ and VDSL2 applications operating on a +14V supply. A new feature supported on the ISL1561 is programming of the quiescent current through SPI. Given a targeted MTPR performance, quiescent current can be adjusted accordingly to reduce power (500µA steps). When transmitting 8b VDSL2, power consumption can be 25% less compared to class AB operation (refer to page 1 in the datasheet). The ISL1561 is very "robust" in handling transients; passing ITU-T K.20 standard tests.

Power Consumption

Figure 1 shows the power consumption comparison for 8b and 17a VDSL2 profiles. For 8b 19.5dBm, the ISL1561 only consumes 600mW while achieving missing band power ratio (MBPR) of -64dBc, and for 17a 14.5dBm, the ISL1561 consumes 400mW while achieving MBPR of -60dBc.

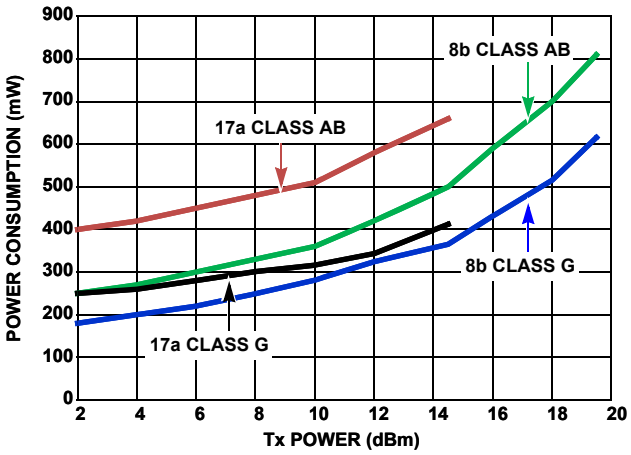

FIGURE 1. CLASS AB vs CLASS G POWER CONSUMPTION

SPI Control

The ISL1561 supply current can be programmed separately for each port with the USB micro-controller integrated on the evaluation board. The micro-controller uses four logic signals (SCLK, SDI, SDO and CS) to communicate with the ISL1561's three pin SPI: (SCLK, SDATA and CS). Since SDATA for the ISL1561 is used for both data in and out, a series 10kΩ is placed between SDI and SDO. Therefore, SDI must be connected directly to SDATA in order for the micro-controller to read the registers in the ISL1561.

Power Sequencing and Reset

The SPI pins can be left floating or pulled low before applying the power supply. An internal 5V VDD is generated for the digital interface. The SPI and BOOST pins are internally biased as follows:

- BOOST Pin: internal pull-up to VDD
- CS Pin: internal pull-up to VDD
- SDATA Pin: internal pull-down to GND
- SCLK Pin: internal pull-down to GND

The serial interface counter will reset while a clock cycle is received with CS high. When CS is driven high, SCLK pulse will reset the serial counter on the falling edge of SCLK.

Evaluation Software

The GUI software is available to program the ISL1561 evaluation board. Running "ISL1561_Installer_V1.0.exe" will install the needed drivers for the program.

The program files will be installed in:
"C:\Program Files\Intersil\ISL1561" and the file to run is "ISL1561.exe".

NOTE: When running the program, be sure the micro-controller is connected to the computer's USB port.

Figure 2 shows that the ISL1561 starts up in disable mode. Clicking "Read All" will have both registers display "80". The two register boxes allow users to write and read. For example, when a user clicks in the box and types "0F", the program also puts back in the same box the read register value, which is also "0F". If a different value is displayed, the register is not programmed correctly.

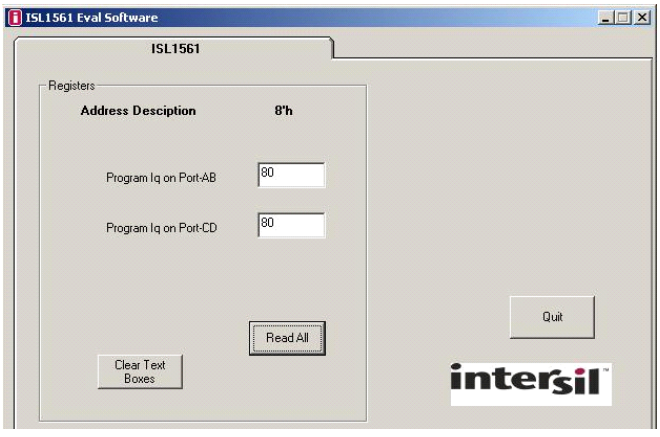

FIGURE 2. WINDOW GUI

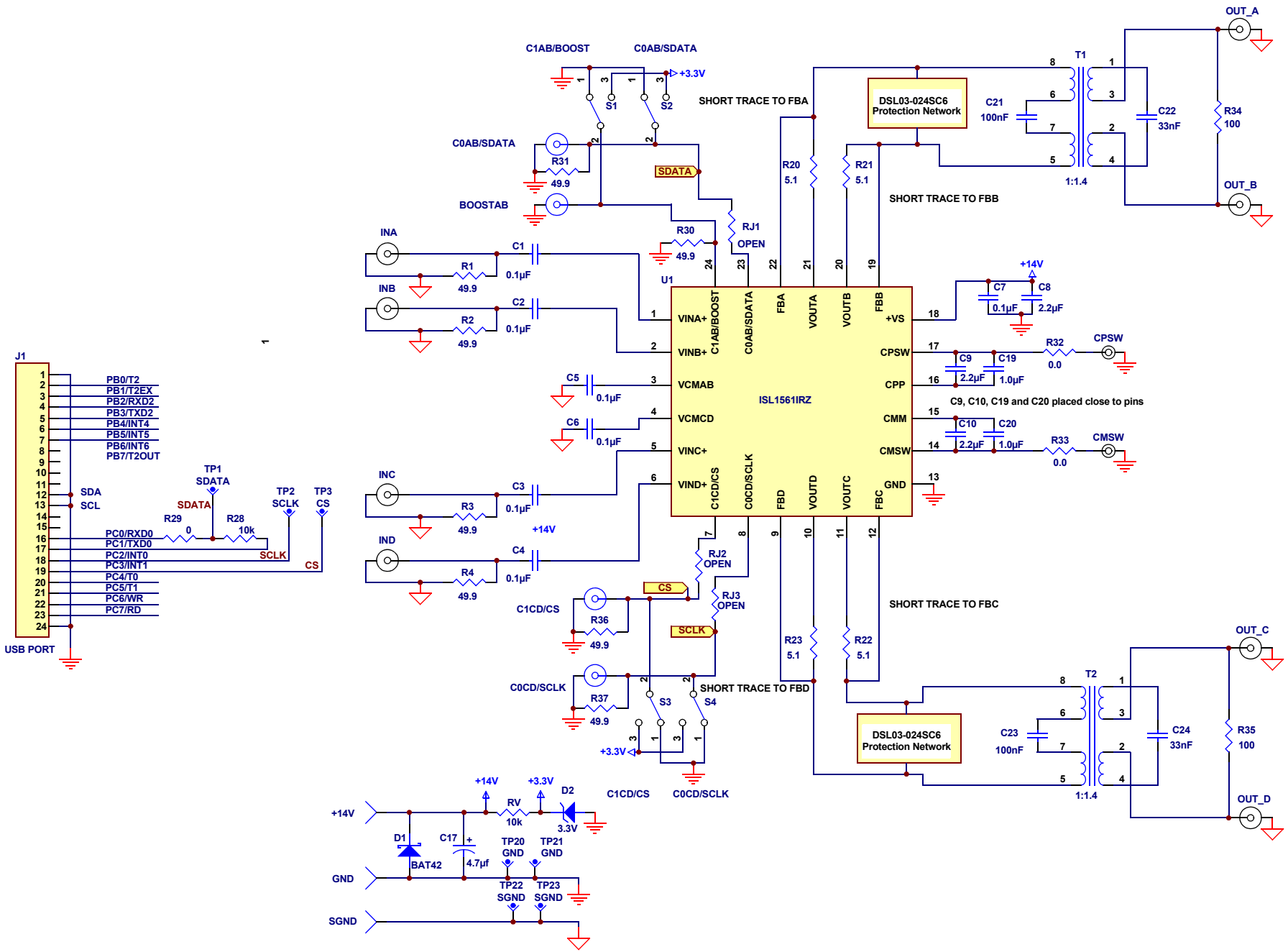

FIGURE 3. EVALUATION BOARD SCHEMATIC

Programming Quiescent Current

Table 1 is the representation of quiescent current given the values entered in the register boxes. The register boxes in the GUI accept hexadecimal. A complete Iq vs. Reg Values is shown in Figure 20 of the ISL1561 datasheet. Entering “0F” in the box will change the quiescent current to 7.2mA for that port. To change to a different value, users can click in the box to highlight the previous value and enter a new value.

TABLE 1. REGISTER VALUES vs Iq

VALUES IN PORTAB OR PORTCD BOX (8’h)	Iq PER PORT (mA)
80	2.5
0F	7.2
1C	10.3
7F	19.5

When the previous value is highlighted, users can also use the up and down arrow keys on the keyboard to change the value. If current value is “0F”, pressing the arrow key down will change the value to “0E” and pressing the key up will change the value to “10”. Each step changes quiescent current by 500µA for the selected port.

The range of quiescent current for each port with the most significant bit (MSB) low is 8’h00 to 8’h7F and with MSB high is 8’h80 to 8h’FF. To change the quiescent current to 10.3mA/port, entering “1C” is the same as entering “9C” in the registers. The latter sets the MSB high. Be careful when setting the MSB high for both ports because this will over-ride boost operation as discussed in “Boost Signal and Operation” on page 4.

When verifying reading and writing to the registers on an oscilloscope, note the least significant bit (LSB) is loaded first and the MSB is loaded last. The scope will display a “F0” instead of a “0F” because the micro-controller reads MSB first. Bit swapping was implemented on the software to load LSB first.

Figure 4 is a scope capture of SDATA in yellow, SCLK in red and CS in blue. From left to right, SDATA shows the first bit is low, which defines read. The next 3 bits, 110, defines reg3 as being read. The following 8 bits, 11110000, defines reg3 has the value of “F0”. Reading and writing to the register only occurs when CS, is held low. Figure 5 illustrates the 12-bit command to program the quiescent current of each port in the ISL1561.

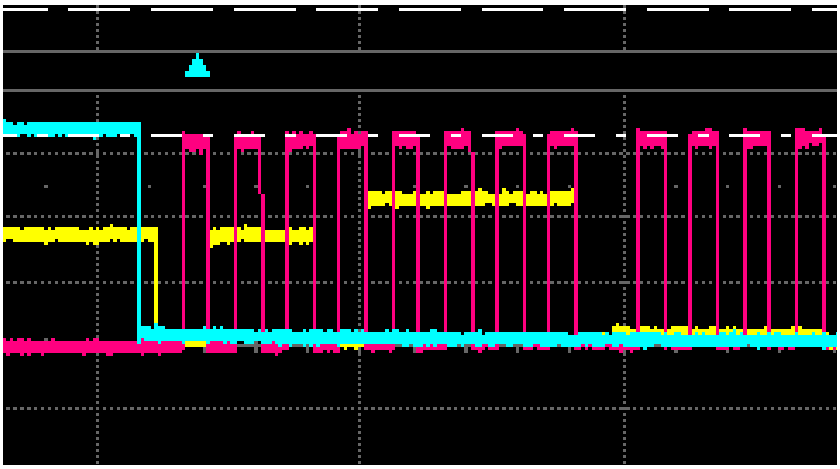

FIGURE 4. SDATA = “F0” IN PORTAB (REG3)

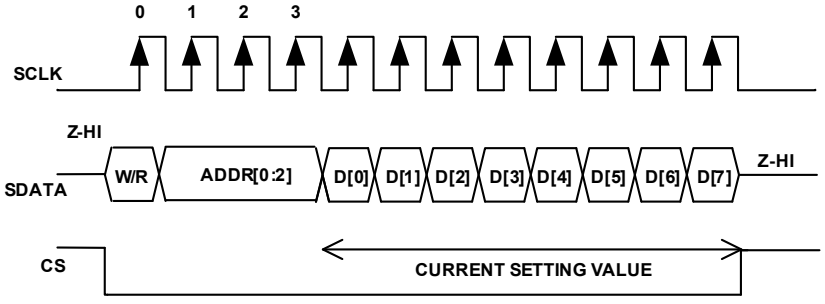

FIGURE 5. 12-BIT COMMAND FOR SDATA

Table 2 outlines the first 4-bit to read and write to reg3 and reg7. Combining Table 1 and 2 gives the 12-bit command line. The following are examples of commands:

1. After start-up, users want to read reg3. Default reg3 value is 8'h08. [011000000001]
2. Users want to change the quiescent current in reg3(PortAB) to 10.3mA. This is the same as writing the value of 8'hC1 in reg3. [111000111000]
3. Users want to change the quiescent current in reg7(PortCD) to 10.3mA. [111100111000]
4. Users want to disable reg3. [111000000001]

TABLE 2. 4-BIT COMMAND TO READ AND WRITE TO REGISTERS

REGISTERS	READ	WRITE
REG3(PORTAB)	0110	1110
REG7(PORTCD)	0111	1111

Boost Signal and Operation

The boost pin has an internal pull-up to help detect the presence of the ISL1561 in Broadcom's reference design. Do not place an external resistor to ground on the boost pin since this will conflict with Broadcom's firmware to detect the ISL1561 as the line driver. Putting the ISL1561 in boost mode with the boost pin high at power up is not recommended because this can result in excess power dissipation by putting the driver in permanent boost mode. In order to satisfy the firmware in detecting the ISL1561 at start-up with boost pin pulled high, boost operation had to be over-ridden and turned off. Having the MSB high for both reg3 and reg7 will over-ride boost operations. By default, the ISL1561 turns boost operation off with reg3 and reg7 having values of 8'h08 to over-ride boosting and resolve any undesirable power-up states. Table 3 shows boost operation is turned off when MSB for both registers is high, even with the presence of a boost signal.

TABLE 3. REGISTER MSB ON BOOST OPERATION

REG3 8'h[7]	REG7 8'h[7]	BOOST PIN	BOOST OPERATION
0	X	1	1
X	0	1	1
1	1	X	0
X	X	0	0

NOTE: X = do not care

Figure 6 shows normal boost operation with the boost signal in red, voltage on the CPSW pin in blue, and the output signal in green. The port has the value of 8'hC1 representing the MSB low.

NOTE: Figure 6 also shows the look-ahead boost timing is 100ns, as recommended in Figure 29 of the datasheet.

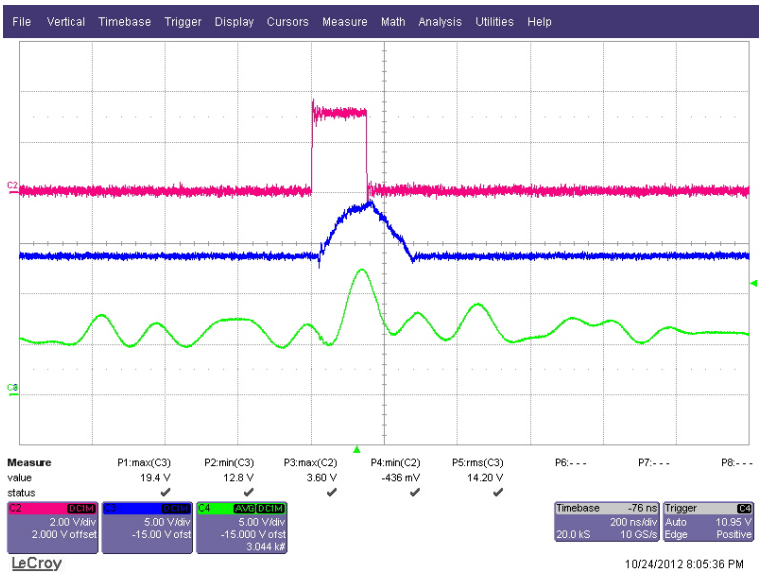

FIGURE 6. BOOST OPERATIONS

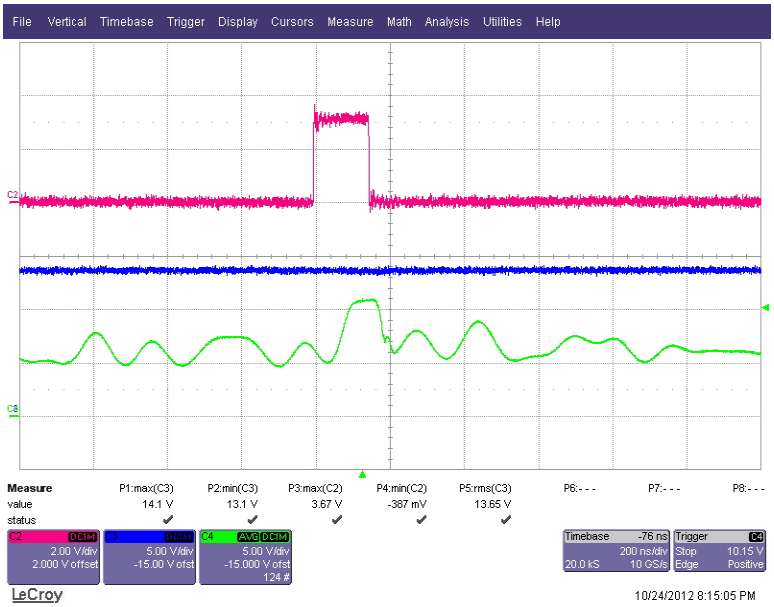

FIGURE 7. OVER-RIDING BOOST OPERATIONS

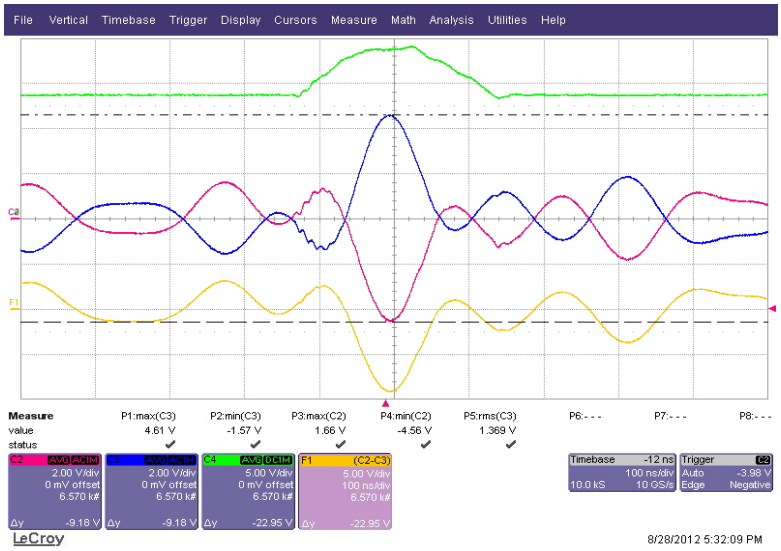

FIGURE 8. BOOST SIGNAL (GREEN), OUTA (BLUE), OUTB (PINK), DIFFOUTAB (YELLOW)

Figure 7 shows over-riding of boost operation. Both ports are programmed to a value of 8'hC9 (MSB high). Even with a boost signal present, the supply voltage is not boosted because boosting is disabled when MSB is high for both ports. With boosting disable, the output signal is clipped because the output is being over driven hitting the supply headroom.

Figure 8 shows scope captures of the output waveform with the supply voltage being boosted. A noticeable ringing at each of the output happens during the rising edge of each boost. The ringing is common mode and does not affect differential performance as the bottom curve shows no ringing in the differential the output.

Board Design Recommendation

It is recommended to operate ISL1561 with less than 45pF of common mode parasitic on any of the four outputs. To minimize parasitic capacitance in the ISL1561 design, consider laying out short output traces, and selecting low capacitance protection devices, and line transformers with low interwinding capacitance in the signal path.

Close placement of the boost capacitors to the boost pins is necessary to minimize parasitic inductance in the boost supply path. On the ISL1561 evaluation board, 1µF and 2.2µF capacitors are used instead of one in order to place the smaller footprint 1µF capacitor close to the boost pins. An increase in ringing at the outputs caused by the rising edge of each boost event is observed if the boost capacitors are moved away from the package pins. Adding 5Ω in series with the boost capacitors will help reduce this common mode ringing.

The supply decoupling capacitors are also placed close to the supply pins to minimize parasitic inductance in the supply path. High frequency load currents are typically pulled through these capacitors so close placement of 0.1µF capacitors on the supply

pin will improve dynamic performance. The higher 2.2µF value capacitors can be placed further from the supply pins as it provides low frequency decoupling.

The thermal pad for the ISL1561 should be connected to ground. For good thermal control, running vias to a bottom pad helps dissipate heat away from the package.

Lightning Surge Robustness

The ISL1561 is very robust to lightning transients at the output. Intersil recommends using a tertiary protection device, TISP4C035L1N, along with a line protection device, 420V GDT (both from Bourns), to pass 10/700µs, 4kV surges and 600Vrms power induction tests. An alternate tertiary protection device, ST's DSL03-024SC6, also is shown to pass k20e tests.

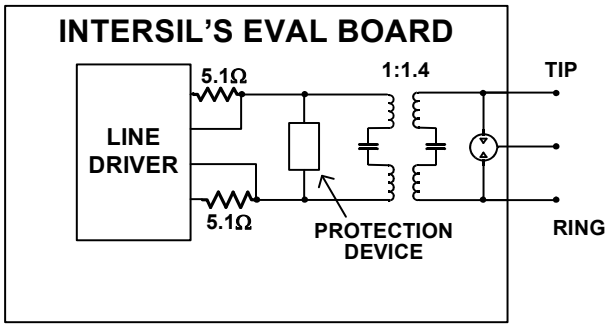

FIGURE 9. CIRCUIT PROTECTION CONFIGURATION

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