
Abstract

This application note describes how to use the SPICE model for the [ISL70001SRH](#), [ISL70001SEH](#) Radiation Hardened and SEE Hardened 6A Synchronous Buck Regulator. This SPICE model was developed to help system designers evaluate the operation of this IC prior or in conjunction with prototyping a system design. This model accurately simulates typical performance characteristics at room temperature (+25 °C) such as loop analysis, transient analysis and start-up. Functionality has been tested on CADENCE ORCAD 16.3. Other SPICE simulators may be used, however, the model may require translation.

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Power Blocks

The model has a parameter named PBLOCK, which is equivalent to the number of LX nodes connected to the ISL70001SRH in a given application. By double clicking the text you can modify the number of blocks to match the prototype board.

Inductor Value

The average model is based on a mathematical representation of the ISL70001SRH. The value of the inductor is needed for the model to accurately simulate the regulator. The model has an added pin LOUT, which is connected to a current source I1 and resistor R7. These create a voltage that is fed into the pin and into

the inductor U2. U2 translates the voltage into inductance by the equation $L_{1V} = 1\mu$, for every volt on LOUT the inductor value is $1\mu\text{H}$. To change the inductor value to say for example 500nH , one must change R7 to 0.5Ω .

VOUT Value

The output voltage must also be known for the average model to work correctly. The VOUT pin is added to read the output voltage and feed into the internal equations within the ISL70001SRH model. For proper simulation of the model V_{OUT} must be connected to the output voltage of the ISL70001SRH application schematic.

Simulation Performance Curves

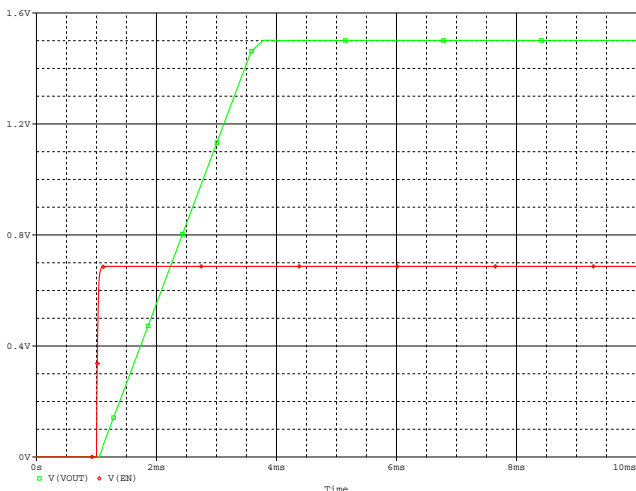


FIGURE 2. SIMULATED START-UP

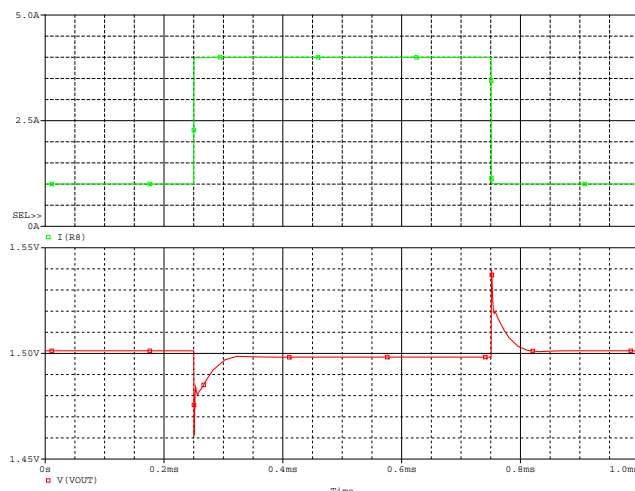


FIGURE 3. SIMULATED 3A TRANSIENT RESPONSE

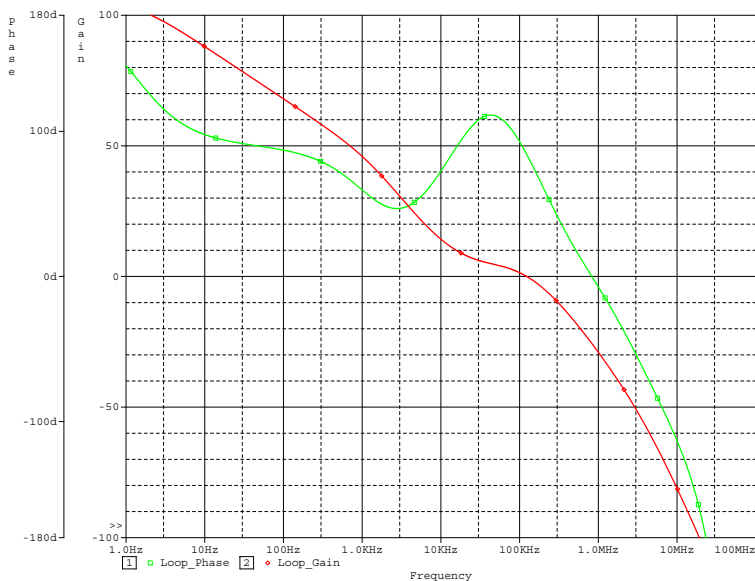


FIGURE 4. SIMULATED LOOP RESPONSE

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338