Maximizing AT25EU Product Service Life

The AT25EU is a new NOR flash product family that features outstanding low energy consumption, excellent write-performance, and low cost.

Products in this family typically support a minimum endurance of 10K program/erase cycles. This application note discusses maximizing the product's service life and predicting the product's longevity based on the application's usage pattern.

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1. AT25EU Feature Summary

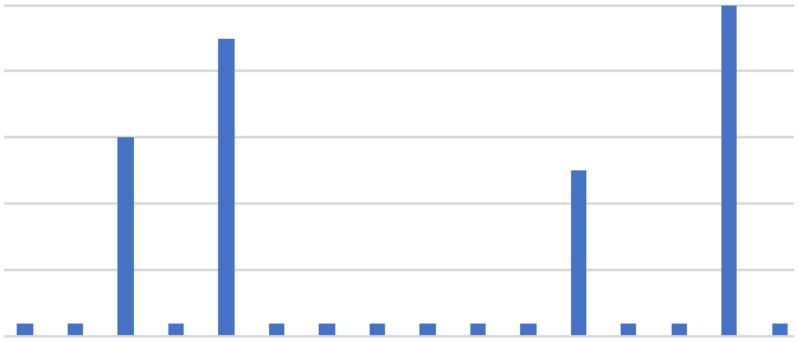
The AT25EU features extremely low power consumption for read, erase and program operations. The power consumption numbers are a fraction of the equivalent numbers for standard flash products. Also, the AT25EU erase operation has an outstanding time efficiency, lasting only 8 ms (typical value) for any size of erased memory. See application note AN406 for more details.

The endurance of the AT25EU family is 10,000 cycles; thus, it is guaranteed that every memory block or page can be erased and programmed at least 10,000 times without performance degradation.

The product can be used for different types of applications, storing code, data, or both. This note focuses on applications that write data often, such as frequent information logging. This type of application is more likely to reach the device's endurance limit, due to frequent data writing. However, with efficient management of data writing, the device's lifetime can be maximized.

2. The Endurance Challenge

Consider a system in which most data writing takes place in a few specific physical memory blocks. The memory block cycling distribution can look uneven, as is illustrated in the diagram below, which shows a few heavily cycled memory blocks and many lightly cycled memory blocks.



After some time, one or more of the heavily cycled memory blocks can reach the endurance limit of 10K cycles. At that point, the flash is not guaranteed to function correctly or optimally. This may signal a premature end-of-life for this system. And all the while there are many memory blocks which could be cycled many more times and haven been barely used.

3. What is a Cycle?

One cycle consists of one erase operation and one program operation. When a memory cell is erased and programmed, this is considered one cycle applied to that cell.

Unlike program operations that can be applied to any individual byte, an erase operation is carried out in bulk. In standard flash devices the minimum memory size for an erase operation is a 4Kbyte block. The AT25EU product family supports a smaller memory size of 256 bytes for an erase operation (known as page-erase). This creates better granularity for write operations.

If the system erases a page and then programs all of it with one program command, every memory cell in that page goes through one cycle. Similarly, if the system erases a page and then programs it in chunks (for example: 4 x program commands, 64 bytes each), one cycle is still applied to each cell.

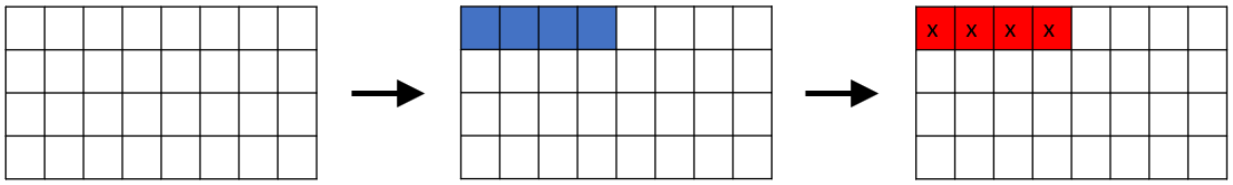
4. Wear Levelling

Because there is a limit to the number of erase/program cycles that can be applied to each memory block, it makes sense to spread erase/program cycles across the memory blocks as much as possible. This is a technique known in the non-volatile memory world as wear-levelling. It is intended to prolong the flash memory's service life.

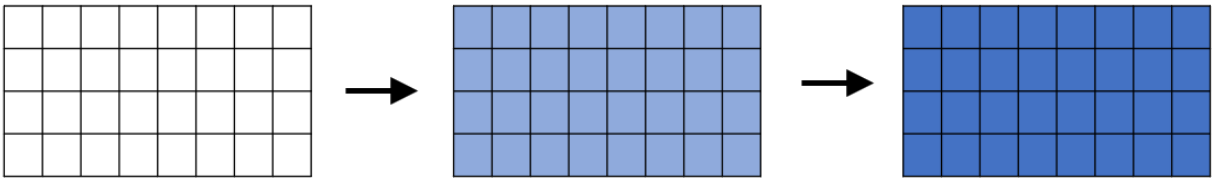
The way wear-levelling is applied to the flash-memory depends on the application's use of the flash memory. At a high-level, wear-levelling manages the distribution of erase/program operations across the memory array. It ensures that no single memory block prematurely fails by exceeding its endurance limit. To do that it spreads writing to as many memory blocks as possible, thus maximizing the number of write cycles that can be done during the system's lifetime.

Below are two simplistic illustrations of flash cycling state transitions during its lifetime. The squares represent memory blocks. A blank cell represents a non-cycled block; a blue cell represents a cycled block. The darker the blue color is, the more the block has been cycled. A red cell with 'x' represents a block that has exceeded its cycling limit.

The first illustration represents a device where wear-levelling is not implemented. Four memory blocks are cycled repeatedly, and finally all of them exceed their cycling limit before most available memory blocks have been touched.



The second illustration represents a device where wear-levelling is implemented. Cycling is distributed between all memory blocks. The block cycling level increases uniformly across the memory array.



The illustrations demonstrate the principle of wear-levelling in the simplest way. Of course, the scenario can be more complicated. For example, half of the memory could be used for data logging while the other half could have a relatively stable image of code or data. At some point in the system's life, it would make sense to swap the two halves so that the frequently cycled region moves into memory blocks that have not been cycled much so far.

In the NOR flash world, wear-levelling is typically implemented by an algorithm running on the host. This algorithm controls the physical mapping of logical data to physical block. It must change this mapping dynamically to ensure that wear-levelling is in effect.

For further reading, see the Wear Levelling Wikipedia article and its references.

5. Cycling Budget

Essentially, a flash part has a life-time cycling budget. For example, if we take the 4-Mbit (512-Kbyte) product from the AT25EU family (AT25EU0041A):

- Each flash device has 128 4-Kbyte blocks. Each block can be cycled 10000 times. So the device has a total budget of 128x10000 = 1,280,000 block cycles during its lifetime.
- Alternatively, working on the device at a finer resolution, each flash device has 2048 256-byte pages. The device has a total budget of 2048*10000= 20,480,000 page cycles during its lifetime.

Efficient use of this lifetime cycling budget requires some sort of wear-levelling. This ensures that no block or page is cycled more than 10000 times, and the cycling budget is fully (or almost fully) used by the system, maximizing its service life.

6. Memory Longevity

If we can calculate the time it takes the system to reach its flash memory cycling budget limit, we can predict the flash memory's longevity in that system. To be able to do that, we need to know how frequently a cycling operation is done in the system on average.

For example, assuming the system performs cycling at the page level. As calculated above, its lifetime cycling budget is 20,480,000 cycles, with wear-levelling. If the system erases and programs a page every 30 seconds, it executes 120 page cycling operations per hour, or 2880 per day. The number of elapsed days before reaching the cycling budget limit is 20,480,000 / 2880 = 7111, giving a lifetime of 7111 / 365 = 19.5 years.

We can also calculate backwards. For a given lifetime requirement, we can calculate the minimum time period (on average) between cycling operations or, otherwise, the maximal page cycling frequency (in terms of cycling operations per time period period).

The following table provides examples of required lifetimes and the cycling implications.

Required Lifetime			min average time between cycling (seconds)	max cycling frequency (cycling per minute)
Years	Days	Seconds		
20	7300	630720000	30.80	1.95
15	5475	473040000	23.10	2.60
12	4380	378432000	18.48	3.25
10	3650	315360000	15.40	3.90

7. Summary

The AT25EU is a NOR flash product family distinguished by its low energy consumption and fast write speed thanks to its short erase time. In terms of endurance, it is guaranteed to allow at least 10,000 erase/program, cycles per memory block. Wear-levelling can help extend the AT25EU cycling budget to the maximum by evenly spreading writes across the memory array. Once the cycling budget and the cycling frequency are known, it is possible to calculate the flash memory's lifetime. Conversely, if the flash memory lifetime requirement is known, it is possible to calculate the average cycling frequency for meeting that requirement.

8. Revision History

Revision	Date	Description
A0	12/2023	Initial release.

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