Using the HS-26C(T)32RH Radiation Hardened RS-422 Line Receiver

Introduction

Renesas' radiation hardened RS-422 line receiver is pin and functional compatible with commercial 2632 types. The HS-26C32 and HS-26CLV32 have CMOS enable pin input levels and the HS-26CT32 accepts TTL-level enable signals. The two circuits are identical except for the configuration of the logic input buffers. The HS-26C32RH and HS-26CLV32 have the same input characteristics (impedance, hysteresis, fail-safe) as commercial types.

This application note explores the electrical characteristics, input/output behavior, and system-level advantages of the families of Radiation Hardened RS-422 Transmitters and Receivers, including their superior noise immunity, ground tolerance, and suitability for low-power, high-speed differential data buses in space-grade designs.

The family of radiation hardened RS-422 Transmitters include HS-26C31EH, HS-26C31RH, HS-26C31RH-T, HS-26CT31EH, HS-26CT31RH, HS-26CLV31EH, and HS-26CLV31RH.

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Contents

1. Description

The HS-26C(T)32RH is a radiation hardened RS-422 line receiver which is pin and functional compatible with commercial 2632 types. The HS-26C32RH has CMOS enable pin input levels and the HS-26CT32RH accepts TTL-level enable signals. The two circuits are identical except for the configuration of the logic input buffers. The HS-26C32RH has the same input characteristics (impedance, hysteresis, fail-safe) as commercial types.

2. Pin Assignments

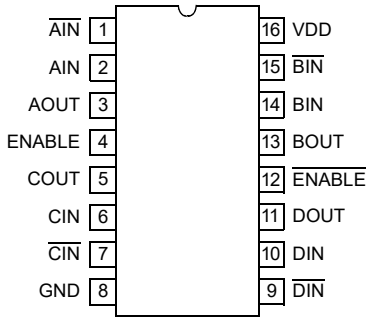


Figure 1. Pin Assignments - Top View

3. Line Input Characteristics

The HS-26C(T)32RH presents a resistive impedance of approximately 10kΩ to the line. This impedance is the composite of the input divider network. No protection devices are present on the line side; there are internal protection devices at the inner end of the input resistor but these do not become active under normal power-up or down conditions.

The input network is fully isolated from the substrate. There are no parasitic junctions. When the device is powered off the input remains at 10kΩ.

The line inputs allow current to be fed from the line into device power and VDD rails. However, this current is not enough to activate the device with VDD off or open; under worst case conditions with both inputs at 5V, the VDD rail will power up to less than 400mV and the output will remain high impedance (off). There is no possibility of the line providing sufficient supply voltage to activate the ’32 or attached logic.

Figure 2 is the schematic of the HS-26C(T)32RH input structure.

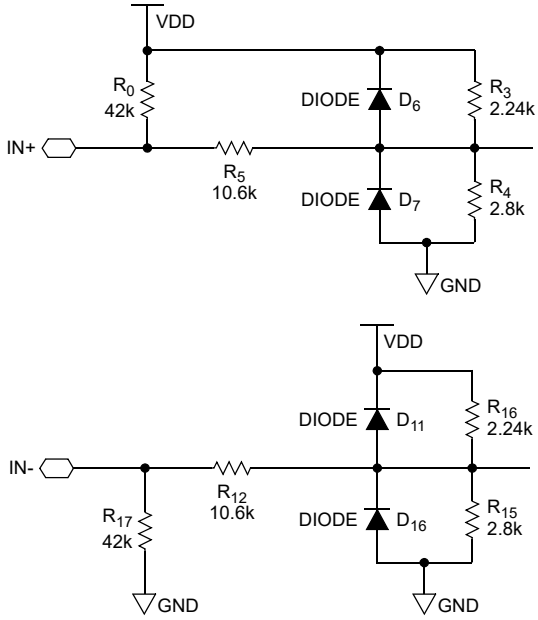


Figure 2. HS-26C(T)32RH Line Input Structure

4. Cross-Strapping

In space systems it is vital to have a data communications bus structure which provides resistance to single point failures. One common technique is the use of redundant bus drivers and receivers in parallel, sometimes called cross-strapping. In this arrangement one driver and receiver are active and another pair is quiescent. The desire to minimize power leads to the need to power down the redundant circuits. This poses a problem for typical CMOS output structures and input protection circuits. The parasitic diodes in the P-Channel output drivers and the input clamp diodes will tend to clamp the signal unless the supply voltage to the quiescent parts remains above the bus signal range.

The HS-26C(T)31RH transmitter provides RS-422 compliant output characteristics, including power-off isolation. The output stage presents a high impedance to the line with power off (VDD < 3V). This prevents any significant amount of current flow over an output voltage range of 0.25V to 6V with respect to device ground.

The use of a BiCMOS output stage provides an output characteristic very similar to LSTTL devices and superior to standard CMOS. Figure 3 shows what the NPN, NMOS and PMOS device physical structures look like.

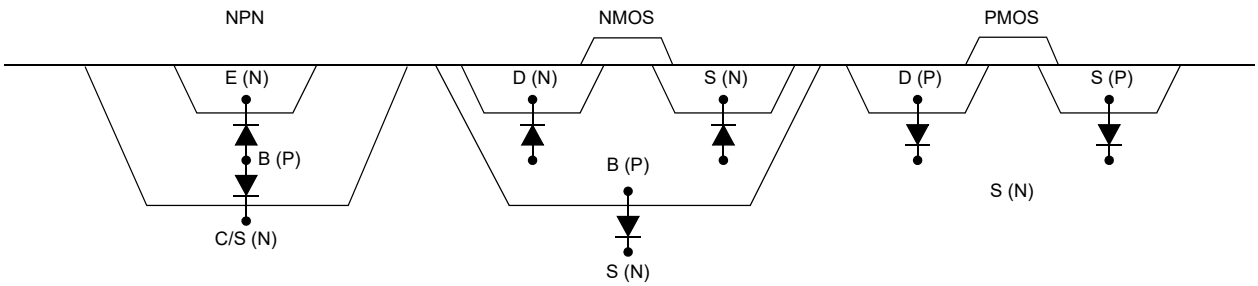


Figure 3. NPN, NMOS and PMOS Device Physical Structures

Figure 4 through Figure 7 illustrate the four standard output topologies and their associated parasitic diodes. The standard P-well CMOS structure presents an undesirable characteristic to the line when the supply is at 0V. This is due to the P-Channel driver's parasitic drain-body diode, which becomes forward-biased at voltages above ground. (See Figure 4.).

N-Channel source-follower high-side drivers and NPN-based output drivers have parasitic diodes which remain reverse-biased with VDD at 0V and output voltages above ground. These output types will not conduct until the E-B or S-B diodes break down, typically above 7V. (See Figure 5 and Figure 6.)

The HS-26C31RH line driver is produced in a radiation hardened CMOS process but uses a NPN bipolar output driver to provide both high output drive and power-off output isolation. The output can be run from ground to over 6V without significant leakage, with the supply off, unlike standard CMOS logic types. This allows the outputs of active and inactive drivers to be paralleled without complications. (See Figure 7.)

The HS-26C32RH line receiver has an input structure which provides a ±10V maximum input signal range with respect to device ground. The input impedance of the receiver is typically 10,000Ω, with no clamping devices at the pin. A powered-down device simply adds its input impedance in parallel to the other devices on the line.

A curve tracer can demonstrate the difference in behavior between a standard CMOS input and output with power off and the HS-26C31/32RH devices' line inputs and outputs. The inactive CMOS devices clamp whatever line they are attached to at less than a volt, drawing many milliamperes. The line pins of the Renesas RS-422 chip set are well-behaved, acting as a tri-state output and a 10kΩ input.

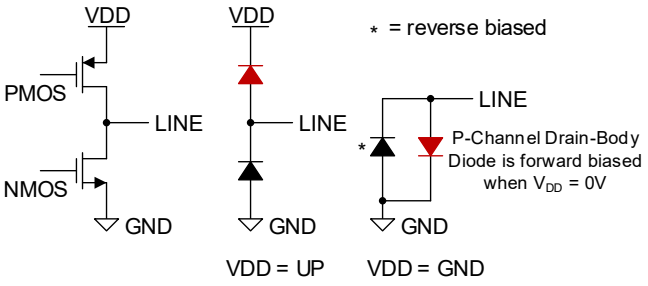


Figure 4. Standard CMOS Output Stage Topology

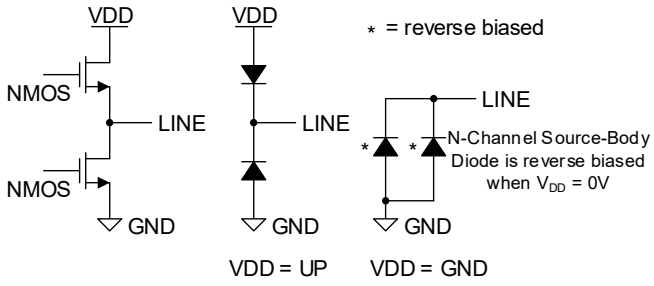


Figure 5. NMOS-Only Output Stage Topology

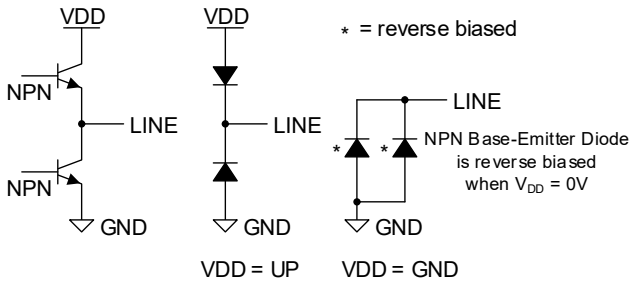


Figure 6. Standard LSTTL Output Stage Topology

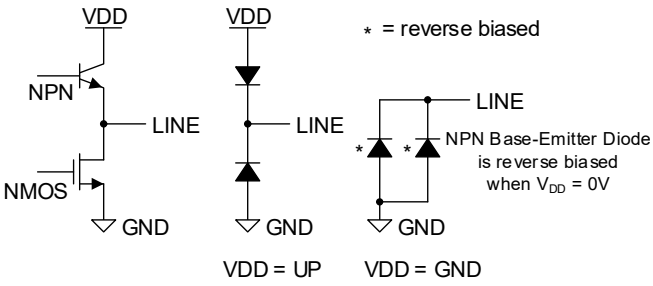


Figure 7. Renesas BiCMOS Output Stage Topology

5. System Noise

Another primary benefit of a balanced, differential line standard such as RS-422 is the cancellation of radiated EMI from the data lines. A shielded twisted-pair data line has primary EMI cancellation by virtue of the anti-phase signals and Faraday shielding as well. In applications where sensitive analog circuitry has to reside near the data bus, this type of bus standard can significantly improve system noise levels and signal quality.

Using this chip set, a 10MHz, low power, quiet bus system with cross-strapped redundant data paths can be implemented easily. The Renesas radiation-hardened CMOS solution cuts power compared to bipolar chip sets and allows configurations not possible with standard CMOS logic.

The large voltage swings, low typical line impedance and differential bus also provide superior immunity to both supply and radiatively-coupled noise. The normal signal span is 8V (+4 to -4) for the HS-26C31/32RH, less than 5V for standard single-ended CMOS and less than 4V for LSTTL. In addition, the HS-26C32RH can tolerate differences between driver and receiver ground levels which would render standard logic either unreliable or completely nonfunctional. For example, an LSTTL or CMOS input whose ground supply is more than 1V below the driving device's may never switch because its VIL(min) level cannot be met. The HS-26C32RH functions properly with its inputs ±7V from device ground. This also minimizes the chances of ground bounce or supply spikes causing false logic states.

5.1 Substrate Connection

The substrate of the HS-26C(T)32RH circuits is connected internally to the VDD pin. If the '32 Receiver is used in die form for hybrid applications, the die should be mounted to an electrically isolated surface. If there is any electrical connection to the back side of the die there will be a low value resistance to the VDD pin. However, the value of the resistance of the substrate and mounting material are not necessarily low or well enough controlled to use as a supply feed.

5.2 Power Dissipation

The HS-26C(T)32RH dissipates about 15mA IDD current at standby. About half of this is used by the divider network and the balance by the input comparators' analog circuitry.

Operating current at frequency is the sum of the standby current and the dynamic operating current given by (CPD) (VDD) (frequency). For the HS-26C(T)32RH the CPD (per active channel) is 40pF. This is equivalent to other '32 types.

5.3 Input Fail Safe

The HS-26C(T)32RH is designed to produce a logic "1" output state when the transmission line inputs are open. This is a special case fault tolerance feature. The fail-safe works by a designed imbalance in the input resistor structure, which produces an inherent error voltage when the inputs are high impedance. The error voltage must be greater than the minimum input differential signal.

Fail-safe operation depends on a true high impedance condition at the inputs. Some circuit or termination schemes may mask or reduce effectiveness of the fail-safe mechanism if they produce a low impedance across the input terminals. The minimum impedance permissible for adequate fail-safe operation is that which results in an input differential voltage of 400mV, the worst case VTH(in).

The relationship between input fail-safe differential voltage and external input impedance is shown below. In order to produce an acceptable differential under an open-line fault condition, any input network external to the chip must present no less than 10kΩ to the line inputs. See plot in Figure 8.

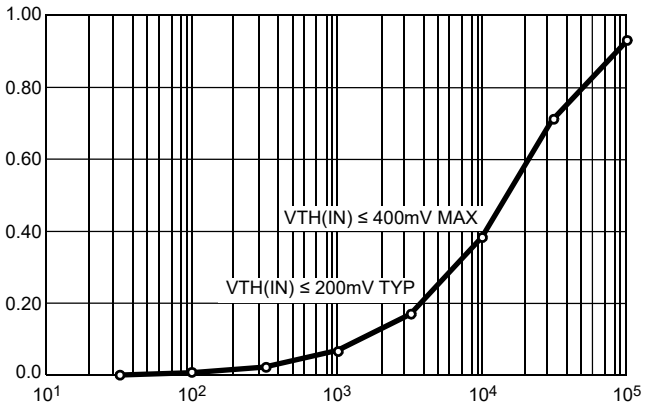


Figure 8. Input Fail Safe Differential vs ZIN (Open)

The practice of simple resistor shunt termination (100Ω across lines) will inhibit fail-safe operation because the shunt resistor will mask the open line condition. If a shunt termination scheme is to be used, it becomes necessary to design a termination which restores the differential bias to the front end. The schematic on the next page shows one possible implementation.

Figure 9 produces too small an input differential voltage in the open-line fault condition. The internal input bias network is shunted by the termination resistor.

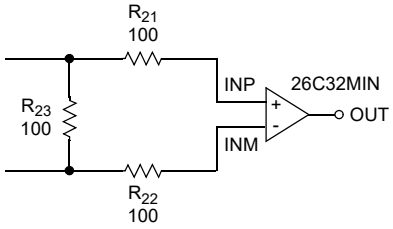
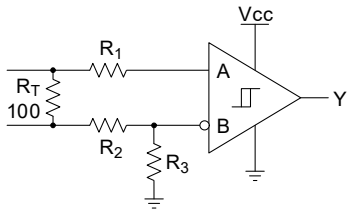


Figure 9. Incorrect Resistor Input Structure

Figure 10 produces an adequate input differential voltage in the open-line fault condition. The internal input bias network is supplemented externally to compensate for the termination resistor.



Receiver	HS-26C(T)32	HS-26CLV32
$V_{CC\,(nom)}$	5.0V	3.3V
R_1, R_2, R_3	1kΩ	2kΩ

Figure 10. Resistor Input Structure for Adequate Input Differential Voltage

The active signal amplitude will be reduced by about 25%, due to the resistive division, but the amplitude is still about 5x to 8x $V_{TH(min)}$, assuring adequate noise margin and speed.

The HS-26C(T)31RH and HS-26C(T)32RH have been fully characterized to 300kRAD total dose. A sample of each wafer lot is evaluated to 300kRAD (Si) total dose, and all post rad electricals (in accordance with the datasheet) must pass.

In addition, Single Event Upset (SEU) and Single Event Latch-up (SEL) testing on these two parts demonstrate that the SEU and SEL thresholds are each >80MEV/mg/cm^2. The testing was performed by NASA Goddard Space Flight Center, and is published in the 1994 IEEE Radiation Effects Data Workshop. (IEEE publication # 94TH06841, *Single Event Effect Proton and Heavy Ion Test Results for Candidate Spacecraft Electronics*, by K. LaBel et al).

6. Revision History

Revision	Date	Description
4.01	Sep 3, 2025	Placed in the latest template. Updated Figures 4-7, 10. Added Revision History section.

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