Using the HS-26C(T)32RH Radiation Hardened RS-422 Line Receiver

Introduction

Renesas' radiation-hardened RS-422 line receiver is pin and functional compatible with commercial 2632 types. The HS-26C32 and HS-26CLV32 have CMOS enable pin input levels and the HS-26CT32 accepts TTL-level enable signals. The two circuits are identical except for the configuration of the logic input buffers. The HS-26C32RH and HS-26CLV32 have the same input characteristics (impedance, hysteresis, fail-safe) as commercial types.

This application note explores the electrical characteristics, input/output behavior, and system-level advantages of the families of Radiation Hardened RS-422 Transmitters and Receivers, including their superior noise immunity, ground tolerance, and suitability for low-power, high-speed differential data buses in space-grade designs.

The family of radiation-hardened RS-422 Transmitters includes HS-26C31EH, HS-26C31RH, HS-26C31RH-T, HS-26CT31EH, HS-26CT31RH, HS-26CLV31EH, and HS-26CLV31RH.

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1. Description

The HS-26C(T)32RH is a radiation-hardened RS-422 line receiver which is pin and functional compatible with commercial 2632 types. The HS-26C32RH has CMOS enable pin input levels and the HS-26CT32RH accepts TTL-level enable signals. The two circuits are identical except for the configuration of the logic input buffers. The HS-26C32RH has the same input characteristics (impedance, hysteresis, fail-safe) as commercial types.

2. Pin Assignments

Figure 1 shows the pin assignments for the radiation-hardened RS-422 line receivers.

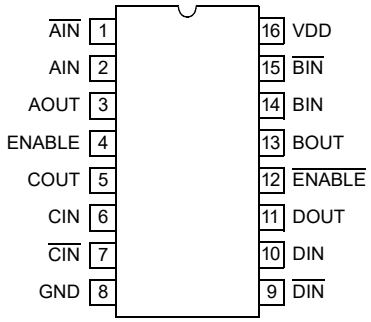


Figure 1. Pin Assignments - Top View

3. Line Input Characteristics

The HS-26C(T)32RH presents a resistive impedance of approximately 10kΩ to the line. This impedance is the composite of the input divider network. No protection devices are present on the line side; there are internal protection devices at the inner end of the input resistor but these do not become active under normal power-up or power-down conditions.

The input network is fully isolated from the substrate. There are no parasitic junctions. When the device is powered off, the input remains at 10kΩ.

The line inputs allow current to be fed from the line into device power and VDD rails. However, this current is not enough to activate the device with VDD off or open; under worst case conditions with both inputs at 5V, the VDD rail powers up to less than 400mV and the output remains high impedance (off). There is no possibility of the line providing sufficient supply voltage to activate the ’32 or attached logic.

Figure 2 is the schematic of the HS-26C(T)32RH input structure.

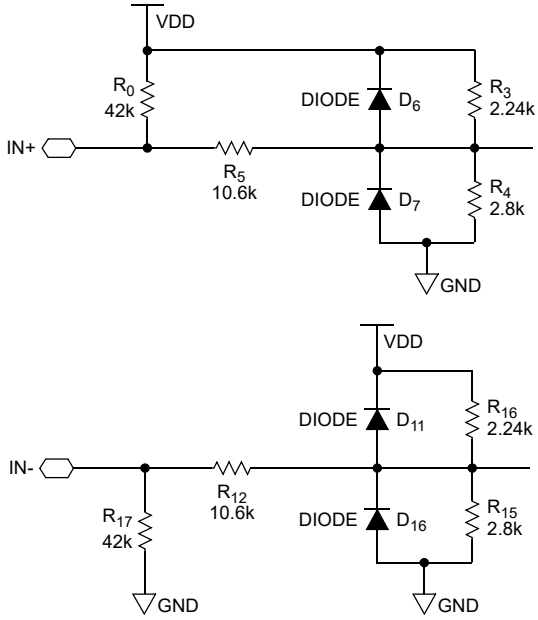


Figure 2. HS-26C(T)32RH Line Input Structure

4. Cross-Strapping

In space systems it is vital to have a data communications bus structure which provides resistance to single point failures. One common technique is the use of redundant bus drivers and receivers in parallel, sometimes called cross-strapping. In this arrangement one driver and receiver are active and another pair is quiescent. The desire to minimize power leads to the need to power down the redundant circuits. This poses a problem for typical CMOS output structures and input protection circuits. The parasitic diodes in the P-Channel output drivers and the input clamp diodes tend to clamp the signal unless the supply voltage to the quiescent parts remains above the bus signal range.

The HS-26C(T)31RH transmitter provides RS-422 compliant output characteristics, including power-off isolation. The output stage presents a high impedance to the line with power off (V_{DD} < 3V). This prevents any significant amount of current flow over an output voltage range of 0.25V to 6V with respect to device ground.

The use of a BiCMOS output stage provides an output characteristic very similar to LSTTL devices and superior to standard CMOS. Figure 3 shows the NPN, NMOS, and PMOS device physical structures.

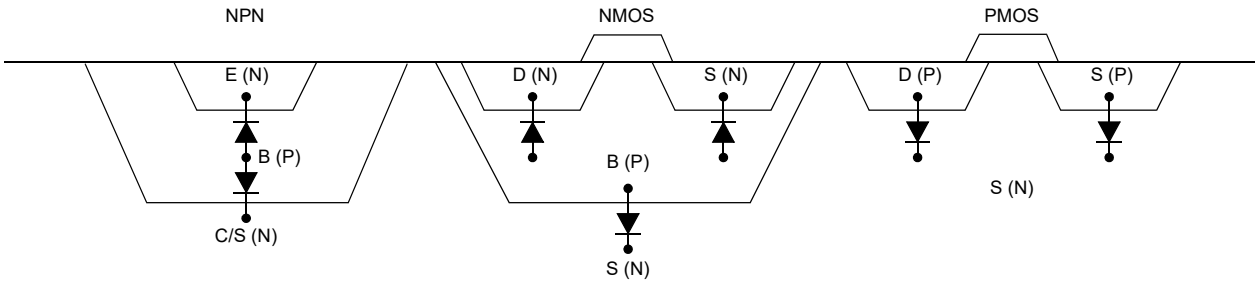


Figure 3. NPN, NMOS, and PMOS Device Physical Structures

Figure 4 through Figure 7 illustrate the four standard output topologies and their associated parasitic diodes. The standard P-well CMOS structure presents an undesirable characteristic to the line when the supply is at 0V. This is due

to the P-Channel driver's parasitic drain-body diode, which becomes forward-biased at voltages above ground. (See Figure 4.).

N-Channel source-follower high-side drivers and NPN-based output drivers have parasitic diodes which remain reverse-biased with VDD at 0V and output voltages above ground. These output types do not conduct until the E-B or S-B diodes break down, typically above 7V. (See Figure 5 and Figure 6.)

The HS-26C31RH line driver is produced in a radiation-hardened CMOS process but uses an NPN bipolar output driver to provide both high output drive and power-off output isolation. The output can be run from ground to over 6V without significant leakage, with the supply off, unlike standard CMOS logic types. This allows the outputs of active and inactive drivers to be paralleled without complications. (See Figure 7.)

The HS-26C32RH line receiver has an input structure which provides a ±10V maximum input signal range with respect to device ground. The input impedance of the receiver is typically 10kΩ, with no clamping devices at the pin. A powered-down device simply adds its input impedance in parallel to the other devices on the line.

A curve tracer can demonstrate the difference in behavior between a standard CMOS input and output with power off and the HS-26C31/32RH devices' line inputs and outputs. The inactive CMOS devices clamp whatever line they are attached to at less than a volt, drawing many milliamperes. The line pins of the Renesas RS-422 chip set are well-behaved, acting as a tri-state output and a 10kΩ input.

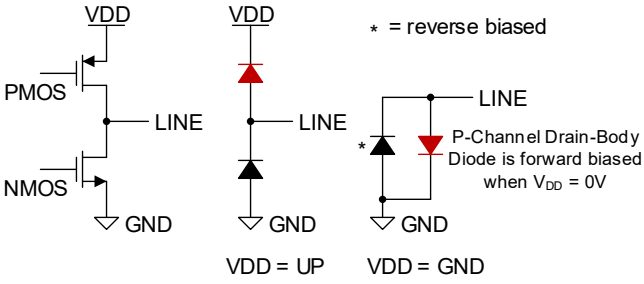


Figure 4. Standard CMOS Output Stage Topology

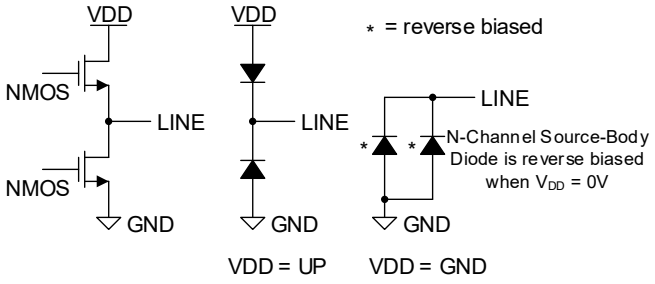


Figure 5. NMOS-Only Output Stage Topology

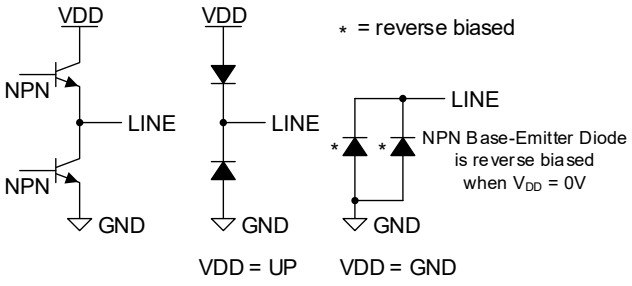


Figure 6. Standard LSTTL Output Stage Topology

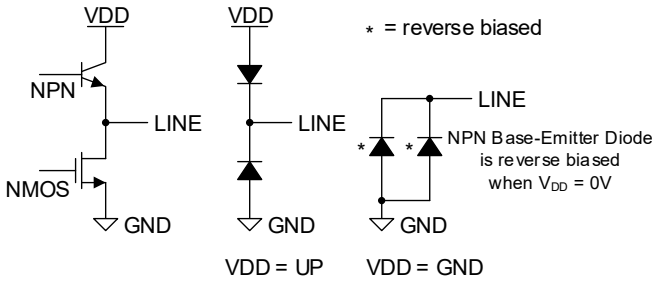


Figure 7. Renesas BiCMOS Output Stage Topology

5. System Noise

Another primary benefit of a balanced, differential line standard such as RS-422 is the cancellation of radiated EMI from the data lines. A shielded twisted-pair data line has primary EMI cancellation by virtue of the anti-phase signals and Faraday shielding as well. In applications where sensitive analog circuitry has to reside near the data bus, this type of bus standard can significantly improve system noise levels and signal quality.

Using this chip set, a 10MHz, low power, quiet bus system with cross-strapped redundant data paths can be implemented easily. The Renesas radiation-hardened CMOS solution cuts power compared to bipolar chip sets and allows configurations not possible with standard CMOS logic.

The large voltage swings, low typical line impedance and differential bus also provide superior immunity to both supply and radiatively coupled noise. The normal signal span is 8V (±4) for the HS-26C31/32RH, less than 5V for standard single-ended CMOS and less than 4V for LSTTL. In addition, the HS-26C32RH can tolerate differences between driver and receiver ground levels which would render standard logic either unreliable or completely nonfunctional. For example, an LSTTL or CMOS input whose ground supply is more than 1V below the driving device's may never switch because its VIL(min) level cannot be met. The HS-26C32RH functions properly with its inputs ±7V from device ground. This also minimizes the chances of ground bounce or supply spikes causing false logic states.

5.1 Substrate Connection

The substrate of the HS-26C(T)32RH circuits is connected internally to the VDD pin. If the '32 Receiver is used in die form for hybrid applications, the die should be mounted to an electrically isolated surface. If there is any electrical connection to the back side of the die there is a low value resistance to the VDD pin. However, the value of the resistance of the substrate and mounting material is not necessarily low or well enough controlled to use as a supply feed.

5.2 Power Dissipation

The HS-26C(T)32RH draws approximately 15mA (I_{DD}) current at standby. About half of this is used by the divider network and the balance by the input comparators' analog circuitry.

Operating current at frequency is the sum of the standby current and the dynamic operating current given by (CPD) (VDD) (frequency). For the HS-26C(T)32RH the CPD (per active channel) is 40pF. This is equivalent to other '32 types.

5.3 Input Fail-Safe

The HS-26C(T)32RH is designed to produce a logic 1 output state when the transmission line inputs are open. This is a special case fault tolerance feature. The fail-safe works by a designed imbalance in the input resistor structure, which produces an inherent error voltage when the inputs are high impedance. The error voltage must be greater than the minimum input differential signal.

Fail-safe operation depends on a true high impedance condition at the inputs. Some circuit or termination schemes may mask or reduce the effectiveness of the fail-safe mechanism if they produce a low impedance across the input terminals. The minimum impedance permissible for adequate fail-safe operation is that which results in an input differential voltage of 400mV, the worst case VTH(in).

The relationship between input fail-safe differential voltage and external input impedance is shown below. To produce an acceptable differential under an open-line fault condition, any input network external to the chip must present no less than 10kΩ to the line inputs. See plot in Figure 8.

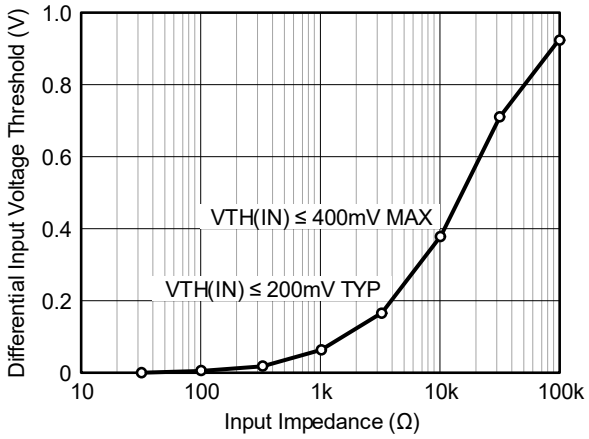


Figure 8. Input Fail-Safe Differential vs ZIN (Open)

The practice of simple resistor shunt termination (100Ω across lines) inhibits fail-safe operation because the shunt resistor masks the open line condition. If a shunt termination scheme is to be used, it becomes necessary to design a termination which restores the differential bias to the front end. The schematics in the next section show three possible implementations.

5.4 Line Terminations

5.4.1 Parallel Termination

Parallel termination uses a 100Ω termination resistor at the remote (receiver) end of the transmission cable (Figure 9).

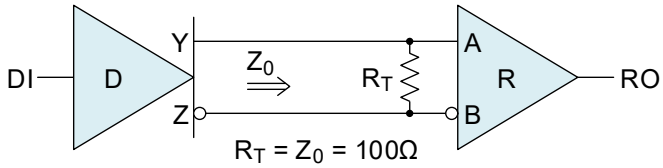


Figure 9. Parallel Termination Configuration

A disadvantage of parallel termination is that it does not support idle-bus fail-safe if the driver is disabled. In this case, R_T forms a voltage divider with the high-impedance receiver inputs, which reduces the differential bus voltage to 0V and causes the receiver output state to be undefined.

Therefore, pausing a transmission requires either keeping the driver permanently enabled while idling the bus on a steady high or low state, or disabling driver and receivers simultaneously to conserve power.

5.4.2 Power Termination

Power termination is a type of parallel termination with added fail-safe biasing. Adding two biasing resistors (R_B) in pull-up and pull-down configuration forms a voltage divider with R_T (Figure 10). When the driver is disabled, its outputs are high-impedance. Then, voltage divider action creates a differential voltage across R_T that is large enough to drive RO high.

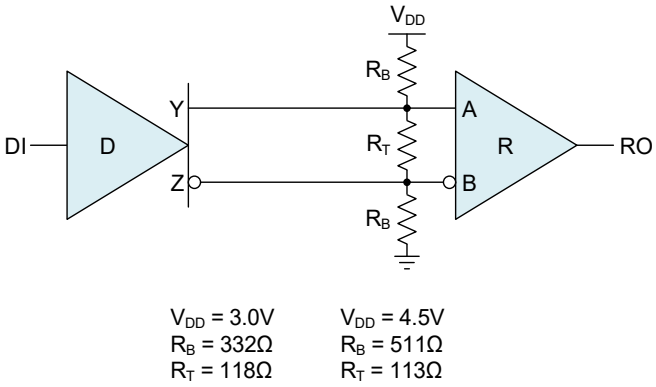


Figure 10. Power Termination Configuration

A slight disadvantage of power termination is high power consumption as the fail-safe voltage divider constantly drains current from the receiver supply when the driver is disabled.

5.4.3 AC Termination

AC termination eliminates the high power consumption of the power termination by placing a termination capacitor, C_T, in series with the termination resistor, R_T (Figure 11).

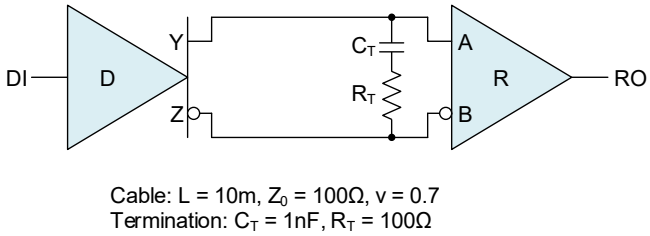


Figure 11. AC Termination for 10m Cable

Therefore, the bus lines are effectively terminated only during signal transitions, while during the signal's steady states, driver output current is minimized. This reduces driver power dissipation while allowing for large output signal swing and high noise margin.

When the driver is disabled, the receiver inputs are floating. In this case, the receiver generates internally its open-bus fail-safe voltage that turns RO high.

A drawback of AC termination is that its use is limited to lower data rates of around 300kbps due to the low-pass filter characteristic of the R_T-C_T unit.

Two requirements govern the value of the R-C time constant.

- The R-C time constant must match the cable's round-trip delay: $R_T \times C_T = \frac{2 \times L_{cable}}{v \times c}$. Making R_T = 100Ω and solving for C_T gives the capacitor value with:

(EQ. 1) $$C_T = \frac{2 \times L_{cable}}{R_T \times v \times c}$$

where

- L_{cable} = Cable length (m)
- v = Cable velocity (typical 0.7)
- c = Speed of light (3×10^8m/s)

- The R-C time constant must be less than or equal to 1/10th of the bit width: $R_T \times C_T \leq \frac{t_{bit}}{10} = \frac{0.1}{DR}$, therefore, limiting the maximum data rate to:

(EQ. 2) $$DR \leq \frac{0.1}{R_T \times C_T}$$

Note: The values for R_T and C_T remain the same for 3.3V and 5V receivers.

5.4.4 Alternate Termination

Alternate Termination uses a more complex resistor network to provide fail-safe biasing when the driver is disabled and when the bus lines are shorted (Figure 12).

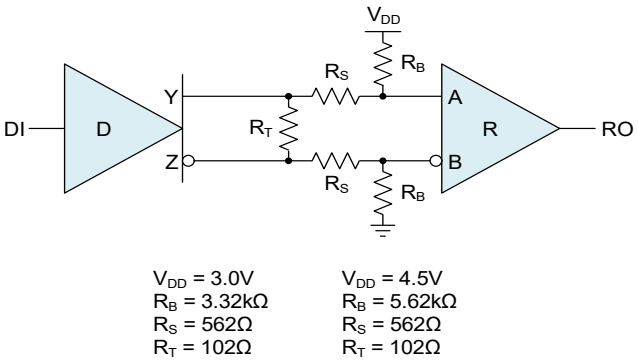


Figure 12. Alternate Termination Configuration

In the short-circuit condition, the termination resistor R_T is shunted and fail-safe voltage developed across the two R_S resistors is large enough to turn RO high.

In the idle-bus condition, when the driver is disabled, the fail-safe voltage occurs across the two R_S resistors and the termination resistor, R_T.

Note: During normal data transmission, the receiver inputs are no longer driven by the low-impedance driver outputs directly. Instead, the series resistors (R_S) modify the DC bias of the receiver inputs during transmission such that the DC operating point of input A differs from that of input B. This causes the magnitude of the differential input voltage to vary between logic states. Consequently, alternate termination should be limited to shorter cable lengths with reduced signal loss and sufficient input voltage magnitude to trigger RO.

6. Ground Potential Difference (GPD) Caution

The RS-422 Standard assigns a large common-mode voltage range to the receiver inputs but none to the driver output. *Note*: During data transmission, the total common-mode voltage at the receiver input is the sum of driver output common-mode, the longitudinally coupled noise into the bus wires, and the ground potential difference (GPD) between driver and receiver.

When the driver is disabled, the total common-mode voltage at the high-impedance driver outputs is the sum of the open receiver input fail-safe voltage and the GPD. Consequently, a large GPD can increase the common-mode voltage beyond the absolute maximum ratings of the driver outputs and damage the device.

7. Radiation Hardness

The HS-26C(T)31RH and HS-26C(T)32RH have been fully characterized to 300krad(Si) total dose. A sample of each wafer lot is evaluated to 300krad(Si) total dose, and all post-radiation electricals (in accordance with the datasheet) must pass.

In addition, Single Event Upset (SEU) and Single Event Latch-up (SEL) testing on these two parts demonstrates that the SEU and SEL thresholds are each >80MeV•cm^2/mg. Testing was performed by NASA Goddard Space Flight Center and is published in the 1994 IEEE Radiation Effects Data Workshop. (IEEE publication # 94TH06841, *Single Event Effect Proton and Heavy Ion Test Results for Candidate Spacecraft Electronics*, by K. LaBel et al).

8. Revision History

Revision	Date	Description
4.02	Sep 24, 2026	▪ Updated Input Fail-Safe section. ▪ Added Line Terminations section and subsections. ▪ Added Ground Potential Difference (GPD) Caution section. ▪ Added Radiation Hardness section. ▪ Updated Figure 8.
4.01	Sep 3, 2025	▪ Placed in the latest template. ▪ Updated Figures 4-7, 10. ▪ Added Revision History section.

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