CCE4511

Typical Application Circuitry

This application note describes the typical external circuitry to use the 4-Channel IO-Link Master Transceiver with integrated Frame Handler.

Contents

Figures

Tables

1. References

[1] CCE4511, Datasheet, Revision 1.00, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

2. External Circuitry

2.1 Basic External Circuitry

This chapter describes the external basic circuitry necessary to ensure proper functionality of the CCE4511.

It is recommended that any design is carefully evaluated, and that the basic external circuitry is extended to meet all the requirements of the finished product.

2.1.1 Power Supply

For proper power supply, a decoupling and stabilization network at the power supply pins of the CCE4511 is required. Figure 1 shows the required decoupling and stabilization capacitors at VS, VDDIO, VDDD and VDDA.

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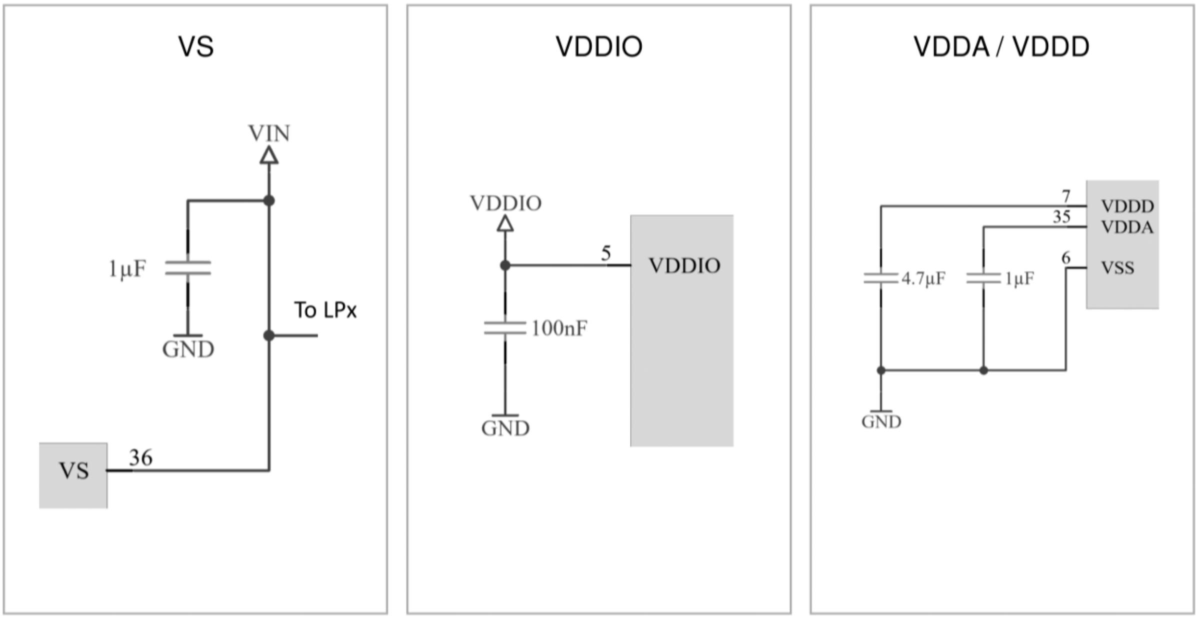

Figure 1. Power Supply Decoupling and Stabilization Network

It is recommended to use Class 2 X5R, X7R or higher graded MLCC capacitors. Capacitor values might need to be adapted to fit the target application. Place all capacitors as close to the corresponding pin as possible, with the smallest capacitor placed closest to the pin.

Do not connect any external load to VDDA and VDDD!

2.1.2 Crystal Oscillator

The CCE4511 uses an external 14.7456 MHz crystal at pins XTAL1 and XTAL2 for clock generation. Figure 2 shows the typical connection of the external crystal using two load capacitors (C_{P1} and C_{P2}) and the option to daisy chain multiple CCE4511.

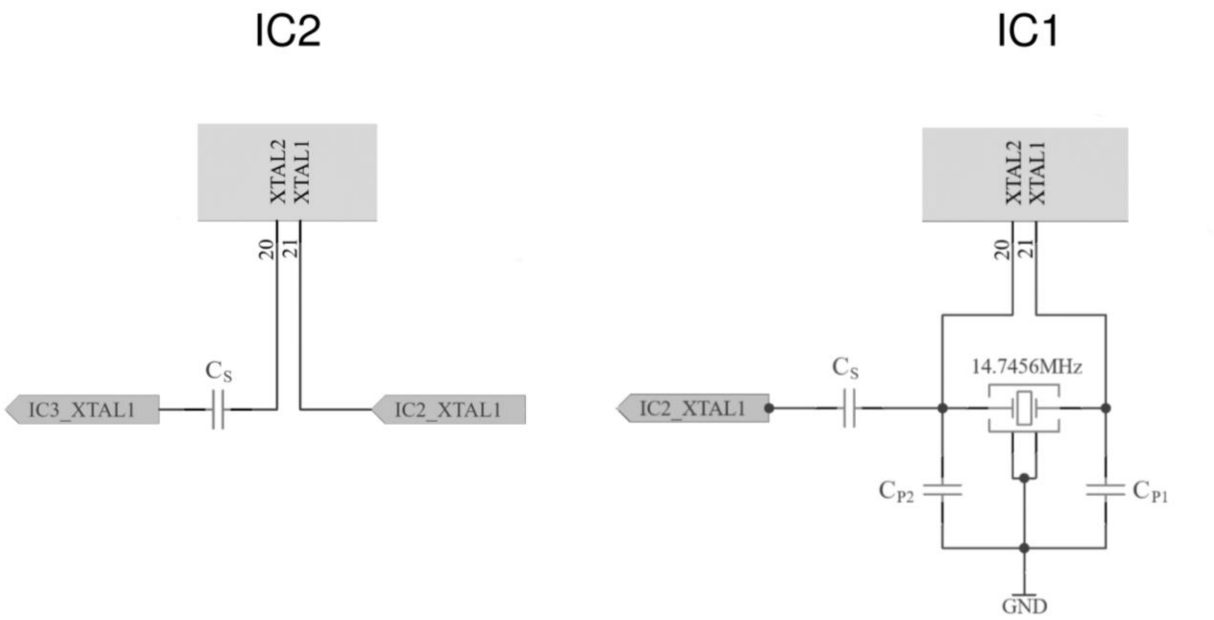

Figure 2. Crystal Oscillator Connection

The load capacitor values depend on the crystals requirements which can be found in the crystals datasheet and can be calculated using Equation 1 and Equation 2, where:

- C_L = crystal load capacitance
- C_{P1} / C_{P2} = external load capacitors
- C_{PX} = stray capacitance + capacitance of XTAL1 and XTAL2 pins
- C_S = capacitor for daisy chain clock signal

C_S should always be selected as 100 pF. If the crystal is placed close to the CCE4511, a value of $C_{PX} \approx 2$ - 3 pF can be assumed.

No Daisy Chain	$C_{P1} = C_{P2} = 2C_L - 3C_{PX}$	**Equation 1**
Daisy Chain	$C_{P1} = C_{P2} = 2C_L - 4C_{PX}$	**Equation 2**

Example calculation without daisy chain, with C_L = 18pF and C_{PX} = 3pF:

$$C_{P1} = C_{P2} = 2C_L - 3C_{PX} = 2 \cdot 18\,pF\ - 3 \cdot 3\,pF = 27\,pF$$

Please be aware that this calculation is for reference only and designers need to make sure that the calculation is specifically done for each design.

2.1.3 IO-Link Channel

The CCE4511 has four independent IO-Link channels. Each channel can utilize its own external circuitry to accomplish any specific application use case. However, it is very common for all channels to use the same external circuitry. In this chapter, the basic circuit is shown as an example for channel 0.

Please be aware that additional external circuitry is needed to switch inductive loads! For more information see 2.2.2 IO-Link Channel.

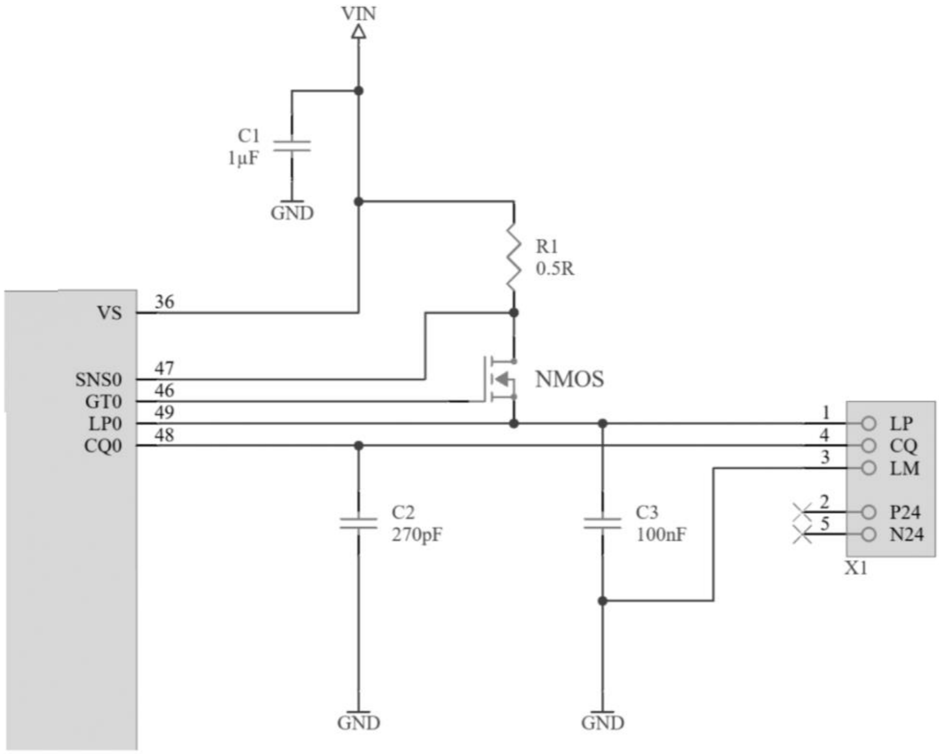

Figure 3. IO-Link Channel 0

An external N-Channel MOSFET (NMOS) is used to switch the power supply (LP) of the channel. For safe operation, a shunt resistor (R1) is used to monitor the current for the internal overcurrent protection and enable the CCE4511 to shut down the power supply of the channel if safe limits are exceeded.

An overcurrent (I_{SENSE_OVC}) is flagged if the voltage across this shunt resistor exceeds V_{SENSE_OVC} (240 mV).

To calculate the necessary shunt value for the application specific overcurrent detection threshold, Equation 3 can be used.

$$R_{SENSE} = \frac{V_{SENSE\_OVC}}{I_{SENSE\_OVC}} = \frac{240\text{ mV}}{I_{SENSE\_OVC}} \quad \textbf{Equation 3}$$

Example calculation for I_{SENSE_OVC} = 2 A:

$$R_{SENSE} = \frac{V_{SENSE\_OVC}}{I_{SENSE\_OVC}} = \frac{240\text{ mV}}{2\text{ A}} = 120\text{ m}\Omega$$

For detailed information about the overcurrent protection and overcurrent limitation feature, please see the CCE4511 Datasheet.

When choosing the external N-channel MOSFET, make sure $V_{GS,MAX}$ is ≥ +15 V and V_{DS} is ≥ VIN of the application.

To ensure a stable slew rate, a capacitor (C2) of 270 pF at CQ is required. Depending on the application and allowed device supply and switching current, a capacitor (C3) at LP is required. A minimum value of 100 nF is recommended. If a higher value for C3 is chosen, make sure to also adjust the value of C1 to guarantee stability of VIN.

Example combinations of C1 and C3:

Table 1: Example Combinations of C1 and C3

C1	C3
1 µF	100 nF
100 µF	1 µF

2.1.4 SPI / UART Interface

Communication with the microcontroller can be done either by SPI, UART or a combination of SPI and UART. However, communication with UART is limited to direct channel control and does not allow to write or read the configuration registers of the CCE4511.

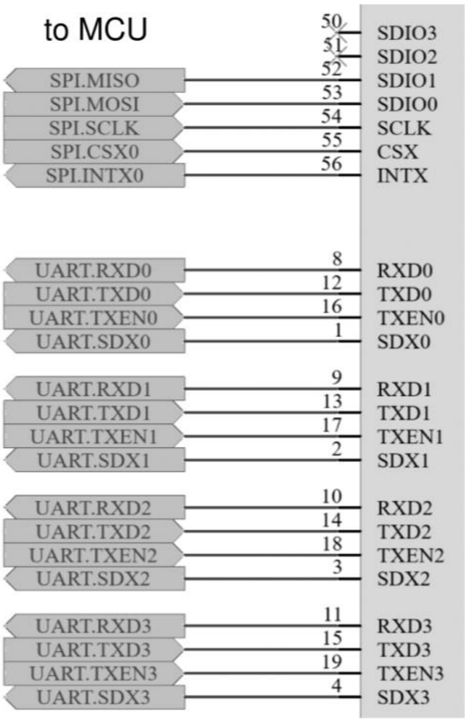

Figure 4. SPI / UART Interface

No additional external circuitry is required for SPI or UART.

2.2 Extended External Circuitry

This chapter describes the recommended extended external circuitry to utilize the complete feature set of the CCE4511 and to successfully pass all necessary environmental and functional tests for IO-Link communication.

Please note that all the information described in the previous chapter also applies to this chapter.

It is recommended that any design is carefully evaluated, and that the circuitry is adapted to meet all the requirements of the finished product.

2.2.1 Power Supply

To extend the power supply decoupling and stabilization network, an additional 4.7 µF capacitor at VDDIO and a reverse polarity protection diode (D1) in series at VIN is used. See Figure 5 for details.

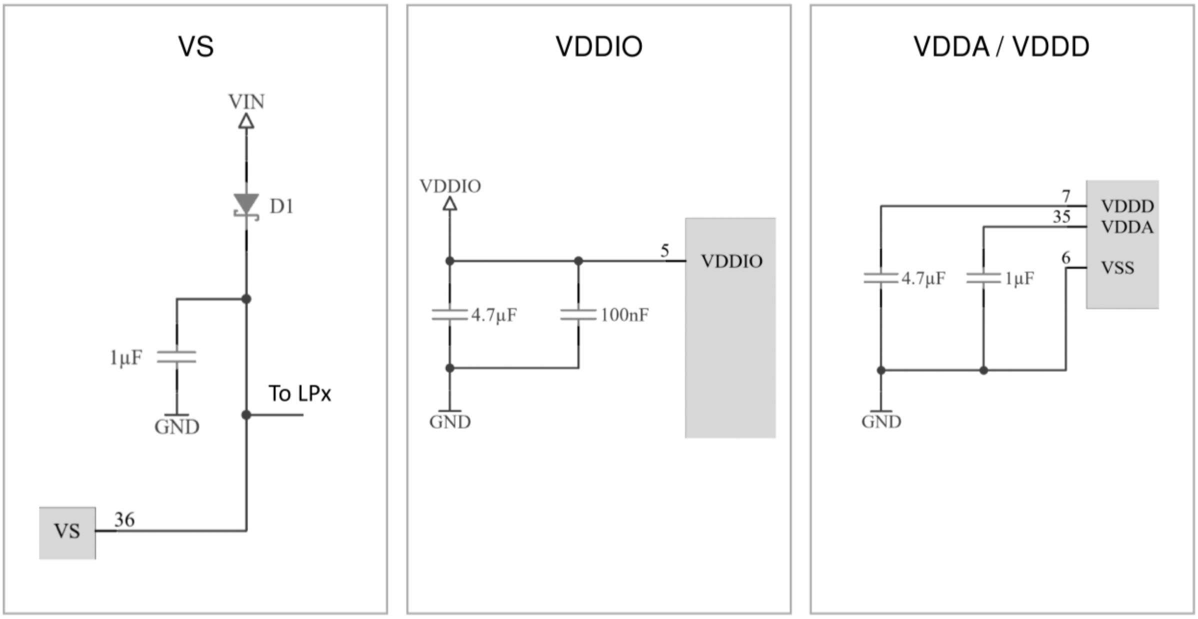

Figure 5. Power Supply Decoupling and Stabilization Network

An example for D1 would be SBRT5A50SA-13 (*Diodes Inc.*). With a high DC blocking voltage of 50 V, an average rectified output current of 5 A and a low forward voltage drop of max. 0.53 V it is suited for applications with a device supply current of 1 A per channel.

An additional 4.7 µF capacitor at VDDIO ensures a more stable power supply. If space is not a limiting factor or of high significance, it is highly recommended to add the additional capacitor.

At VDDD / VDDA, there are no changes to the external circuitry.

2.2.2 IO-Link Channel

To switch inductive loads and to achieve additional protection for each channel, extended external circuitry is required. See Figure 6 for details.

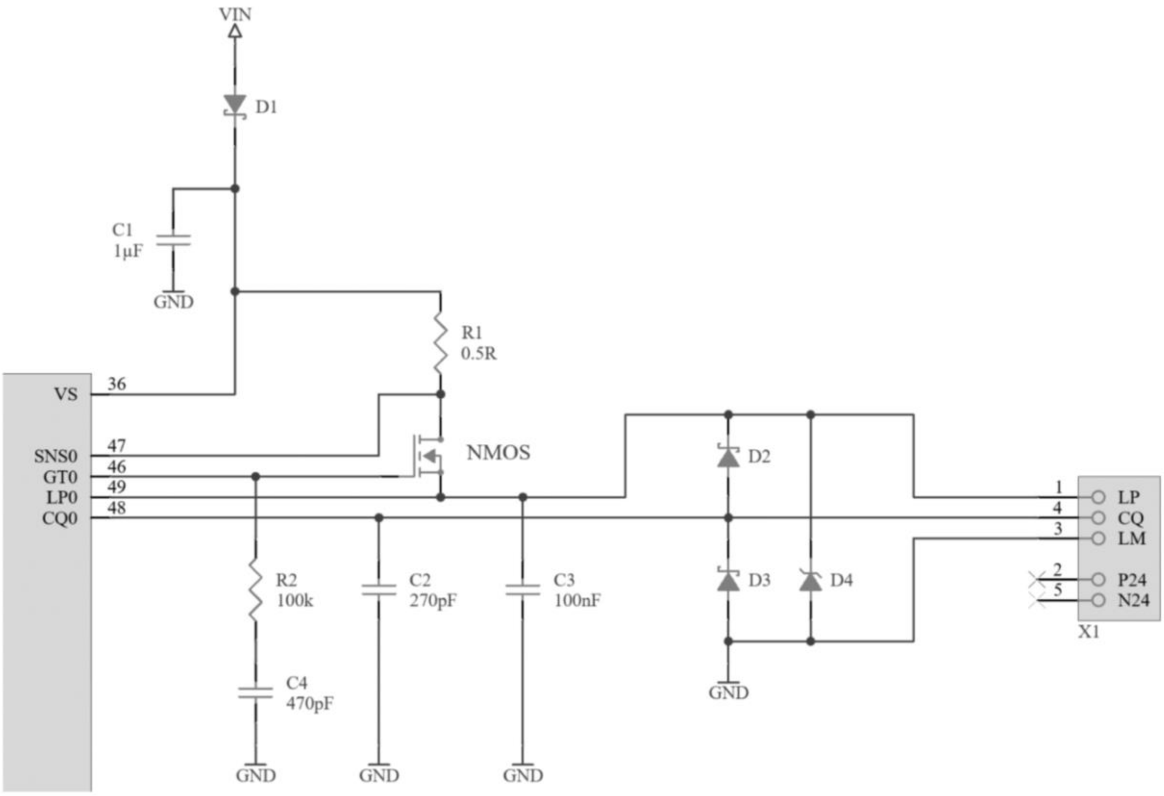

Figure 6. IO-Link Channel 0 Extended Circuitry

If switching inductive loads is a required feature of the IO-Link channel, an additional compensation network (R2 and C4) is necessary at GTx. This ensures the stability of the current limit feature. The values of R2 and C4 are not to be changed.

Diodes D2, D3 and D4 are used for extended protection of the IO-Link channel.

D2: Protects CQ pin from voltage levels higher than LP. It is mandatory to use a Schottky diode due to its low forward voltage. A suitable example is SBR2U60S1F-7 (*Diodes Inc.*)

D3: Protects CQ pin from voltage levels lower than LM. It is mandatory to use a Schottky diode due to its low forward voltage. A suitable example is SBR2U60S1F-7 (*Diodes Inc.*)

D4: Protects the IO-Link interface from surge pulses. An example for D4 is SMF4L33A (*Littlefuse Inc.*). With a breakdown voltage (V_{BR}) of 36.7 V to 40.6 V and a reverse standoff voltage (V_R) of 33 V, it allows for a supply voltage range of up to 36 V.

Revision History

Revision	Date	Description
01.00	Aug 07, 2024	Initial version.

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