Choosing the Correct Crystal or XO for FemtoClock 3 and FemtoClock 3 Wireless

This document highlights the characteristics to consider when choosing a crystal or XO for FemtoClock™3 (FC3) devices and FemtoClock 3 Wireless (FC3W) devices. It also contains a list of recommended crystals to be used with FC3 or FC3W.

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Tables

1. Introduction

The FemtoClock 3 (FC3) and FemtoClock 3 Wireless (FC3W) families of devices use a crystal (or XO) as a reference for the analog PLL (APLL). All FC3 and FC3W outputs are synthesized from the APLL. When choosing the crystal or XO for an FC3 or FC3W device, several characteristics must be considered to ensure optimal performance and minimized output jitter. The following sections highlight these crystal or XO characteristics so that the correct crystal is chosen for a given project. Table 1 provides a summary of the FC3 crystal input (XIN) requirements, and Table 2 provides a summary of the FC3W crystal input (XIN) requirements.

Table 1. FC3 XIN Input Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
-	Mode of Oscillation	-	Fundamental			-
F_{IN}	Input Frequency	Using a crystal, APLL in Integer mode [1]	25	-	80	MHz
		Using an XO, APLL in integer mode.	25	-	150	MHz
		Using a crystal, APLL not in Integer mode [2]	25	-	73	MHz
		Using an XO, APLL not in Integer mode [2]	25	-	63	MHz
f_{VCO}	Analog PLL VCO Operating Frequency	-	9.7	-	10.75	GHz
Requirements for Crystals						
ESR	Equivalent Series Resistance	$8pF \leq C_L \leq 10pF$	-	-	50	Ω
C_O	Shunt Capacitance	-	-	-	4	pF
C_L	Load Capacitance	-	-	8	12	pF
Drive	Drive Level	C_L = 8pF	-	160	-	µW
		C_L = 10pF	-	225	-	µW
F_{TOL} [3]	Frequency Tolerance	-	-450	-	450	PPM
Requirements for XOs						
V_{BIAS}	Bias Point for XIN	Over-driving crystal input	-	0.6	-	V
V_{IVS}	Input Voltage Swing for XIN	Over-driving crystal input	0.6	-	1.2	V
Vslew [4]	Input Slew Rate for XIN	Over-driving crystal input	0.6	-	-	V/ns

1. APLL configured with integer_mode = 1, apll_fb_div_frac = 0, and the DPLL configured with dpll_mode = 0 (Freerun). Note that this configuration does not permit the APLL to be steered by the DPLL/DCO.
2. APLL configured with integer_mode = 0, apll_fb_div_frac ≠ 0.
3. These parameters are customer/application dependent. Common maximum values are F_{TOL} = ±20ppm, F_{STAB} = ±20ppm, and Aging = ±5ppm/10years. The customer is free to adjust these parameters to their particular requirements.
4. The slew rate is calculated by measuring at the midpoint of the rising waveform using a window of ±50mV.

Table 2. FC3W XIN Input Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
-	Mode of Oscillation	-		Fundamental		-
F_{IN}	Input Frequency	Using a crystal	25	-	80	MHz
		Over-driving crystal input	25	-	100	MHz
f_{VCO}	Analog PLL VCO Operating Frequency	A100 devices	9.8	-	10.35	GHz
		A200 devices	9.3	-	9.85	GHz
Requirements for Crystals						
ESR	Equivalent Series Resistance	$8pF \leq C_L \leq 10pF$	-	-	50	Ω
C_O	Shunt Capacitance	-	-	-	4	pF
C_L	Load Capacitance	-	-	-	10	pF
Drive	Drive Level	C_L = 8pF	-	160	-	µW
		C_L = 10pF	-	225	-	µW
F_{TOL} [1]	Frequency Tolerance	-	-450	-	450	PPM
Requirements for XOs						
V_{BIAS}	Bias Point for XIN	Over-driving crystal input	-	0.6	-	V
V_{IVS}	Input Voltage Swing for XIN	Over-driving crystal input	0.6	-	1.2	V
Vslew [2]	Input Slew Rate for XIN	Over-driving crystal input	0.6	-	-	V/ns

1. These parameters are customer/application dependent. Common maximum values are F_{TOL} = ±20ppm, F_{STAB} = ±20ppm, and Aging = ±5ppm/10years. The customer is free to adjust these parameters to their particular requirements.
2. The slew rate is calculated by measuring at the midpoint of the rising waveform using a window of ±50mV.

2. Frequency

2.1 FC3 Frequency Parameters

For synthesizer applications (APLL in Integer mode), FC3 supports crystals with frequencies in the range of 25MHz to 80MHz. Crystal oscillators with frequencies in the range of 25MHz to 150MHz can be used by overdriving the crystal input. The best performance is obtained by selecting a frequency that is an integer multiple of the VCO frequency to allow all dividers to run in integer mode.

For jitter attenuator (JA) applications (APLL not in Integer mode), the maximum frequency is 73MHz when using a crystal and 63MHz when over-driving the crystal input. The best performance is obtained by selecting a crystal that is not an integer of the VCO or the output frequency to reduce the likelihood of boundary spurs. Attention should also be paid to the harmonic frequencies of the crystal and outputs to avoid boundary spurs. Boundary spurs are produced when the phase-locked loop (PLL) feedback loop fractional divider ratio is programmed to a value that is close to an integer. Boundary spurs occur because the harmonics of the phase and frequency detector (PFD) frequency mix with the VCO (or its harmonics) and the resultant intermodulation frequency components fall within the loop bandwidth. Ideally, the ratio of an output frequency or its harmonics to the crystal frequency (or the crystal frequencies harmonics) should not have a fractional component close to .0 or 0.5, with the best cases being a fractional component of 0.25 or 0.75. For a detailed explanation of boundary spurs, see the application note, Integer Boundary Spurs in Fractional Feedback Phase-Locked Loops (PLLs).

Table 3 shows several recommended crystal frequencies for common output frequencies. The recommended crystal frequencies differ depending on whether synthesizer mode or jitter attenuator mode is being used. For 100MHz, 125MHz, 156.25 MHz, and 312.5MHz synthesizer applications, Renesas recommends that 62.5MHz be selected as the primary option, 50MHz be used as a secondary option, and 10GHz be used for a VCO frequency. For 106.25MHz, 212.5MHz, and 425MHz synthesizer applications, Renesas recommends that 68MHz be selected as the primary option, 50MHz be used as a secondary option, and 10.2GHz be used for a VCO frequency. These crystal frequency/VCO frequency combinations ensure that there is an integer relationship between the crystal frequency and the VCO, as well as between the VCO and the output frequency. These integer relationships decrease the likelihood of fractional spurs.

Table 3. Recommended Output Frequency / Crystal Frequency Pairs for FC3

Mode	Output Frequencies (MHz)	Recommended Crystal Frequencies (MHz)	Recommended VCO Frequency
Synthesizer	100, 125, 156.25, 312.5	78.125, 62.5, 50	10GHz
	106.25, 212.5, 425	68, 63.75, 50	10.2GHz
Jitter Attenuator	100, 106.25, 125, 156.25, 212.5, 312.5, 425	68, 54, 49.152	10GHz
		73, 60, 48	10.625GHz

For jitter attenuator applications using output frequencies of 100MHz, 106.25MHz, 125MHz, 156.25MHz, 212.5MHz, 312.5MHz, and 425MHz, Renesas recommends that 54MHz be selected as the primary option with a VCO frequency of 10GHz; 73MHz can be selected as a secondary option with a VCO frequency of 10.625GHz. This ensures that the APLL is not operating in integer and reduces the likelihood of integer boundary spurs.

For jitter attenuator applications, the RMS jitter of outputs can be improved by selecting a crystal that is slightly offset from the goal crystal input frequency. A crystal's frequency will naturally vary as the temperature of the crystal changes. A crystal's frequency stability expresses the degree to which the frequency will vary over a crystal's operational temperature range. Additionally, a crystal's tolerance indicates the difference between the actual frequency of the crystal from the nominal frequency value at 25°C.

Figure 1 shows RMS jitter data for an FC3 output as the crystal input frequency varies over a range of 60MHz ±100ppm while the goal of the crystal input frequency programmed on the device remains at 60MHz. Frequency variations from the crystal can cause significant changes in performance. Smaller frequency offsets from the goal frequency yield larger increases in jitter. As the offsets applied to the crystal input become larger, the RMS jitter of the output decreases and eventually begins to level out. This is significant as many crystals have a stability rating <= ±30ppm and a tolerance rating <= ±20ppm, meaning that they will operate within ±50ppm of the nominal frequency (the region with the worst performance). Using a crystal with nominal frequency that is slightly offset from the goal frequency can improve performance by ensuring that the crystal input frequency remains in the frequency range that performs best. The RMS jitter improves with larger offsets from the goal frequency as the walking spurs caused by the crystal frequency variation can be better filtered by the DPLL loop, compared to the walking spurs created by smaller offsets.

Example: Using an arbitrary crystal with a frequency of 59.9952MHz (60MHz to 80ppm), with a stability of ±15ppm and a tolerance of ±5ppm, the frequency of the crystal will be somewhere in the range of 60MHz – 100ppm to 60MHz – 60ppm. This means the RMS jitter of the output will be between 60.7fs and 64.4fs based on the data in Table 4. If an arbitrary crystal with nominal frequency of 60MHz is used instead with the same stability and tolerance, the frequency range will be 60MHz ±20ppm, and the RMS jitter of the output will be between 56.5fs and 105.3fs, based on the data in Table 4.

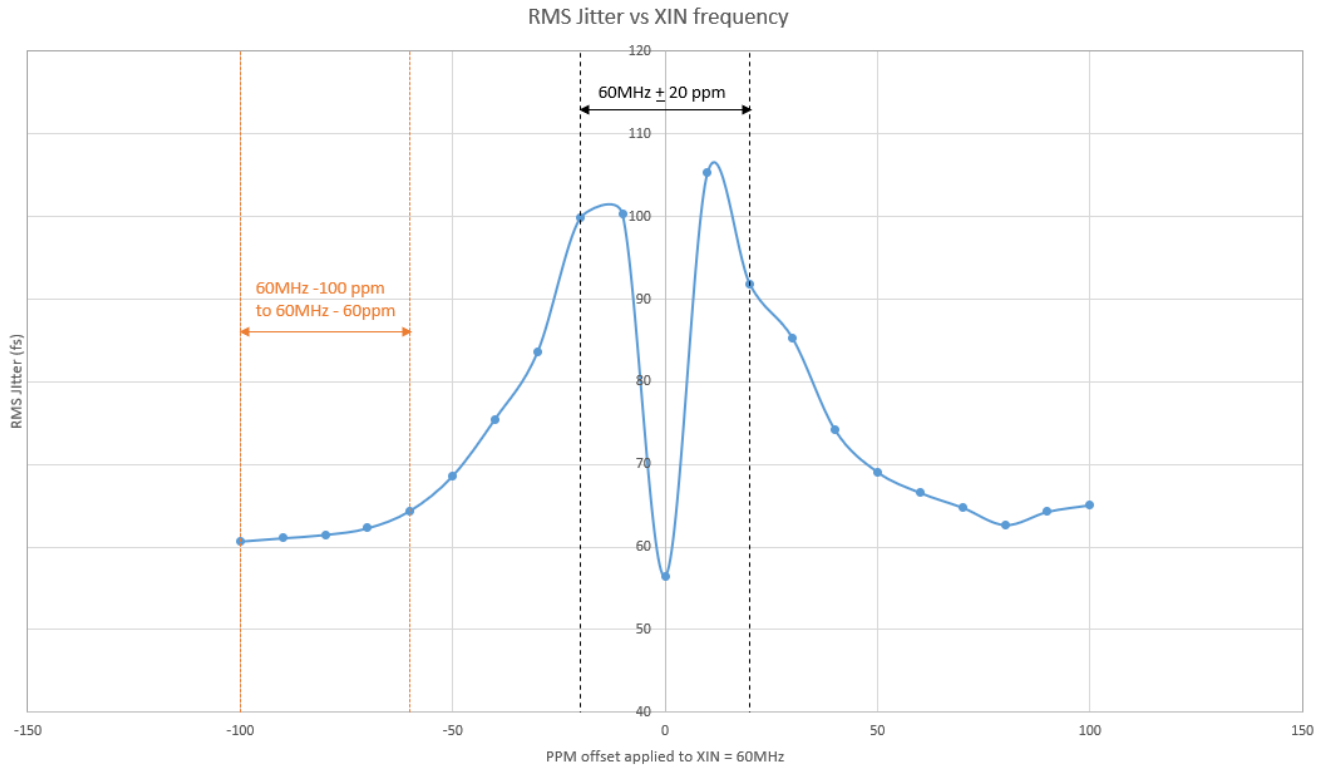

Figure 1. RMS Jitter Plot of a 156.25MHz FC3 Output in JA Mode as the XIN Freq. Varies over 60MHz ±100ppm

Table 4. RMS Jitter of a 156.25MHz FC3 Output in JA Mode as the XIN Freq. Varies over 60MHz ±100ppm

Offset of XIN from 60MHz (ppm)	RMS Jitter (fs)
-100	60.7
-90	61.1
-80	61.5
-70	62.3

Offset of XIN from 60MHz (ppm)	RMS Jitter (fs)
-60	64.4
-50	68.6
-40	75.5
-30	83.6
-20	99.8
-10	100.3
0	56.5
10	105.3
20	91.8
30	85.3
40	74.2
50	69.1
60	66.6
70	64.8
80	62.7
90	64.3
100	65.1

2.2 FC3W Frequency Parameters

FC3W is supported in two different hardware revisions, A100 and A200. The A100 revision supports a VCO range of 9.8GHz to 10.35GHz, and the A200 revision supports a VCO range of 9.3GHz to 9.85GHz. Both hardware revisions support crystals with frequencies in the range of 25MHz to 80 MHz, and frequencies in the range of 25MHz to 100MHz when overdriving the crystal inputs.

For applications that have DPLLs in synthesizer mode, the best performance is obtained by selecting a frequency that is an integer multiple of the VCO frequency to allow all dividers to run in integer mode.

For applications that have DPLLs in jitter attenuator mode, the best performance is obtained by selecting a crystal frequency that is not an integer of the VCO or the output frequency. Following this recommendation will reduce the likelihood of boundary spurs. Attention should also be paid to the harmonic frequencies of the crystal and outputs to avoid boundary spurs. Boundary spurs are produced when the phase-locked loop (PLL) feedback loop fractional divider ratio is programmed to a value that is close to an integer. Boundary spurs occur because the harmonics of the phase and frequency detector (PFD) frequency mix with the VCO (or its harmonics) and the resultant intermodulation frequency components fall within the loop bandwidth. Ideally, the ratio of an output frequency or its harmonics to the crystal frequency (or the crystal frequencies harmonics) should not have a fractional component close to .0 or 0.5, with the best cases being a fractional component of 0.25 or 0.75. For a detailed explanation of boundary spurs, see the application note, Integer Boundary Spurs in Fractional Feedback Phase-Locked Loops (PLLs).

2.2.1 FC3W A100 Frequency Parameters

FC3W A100 devices are recommended for wireless applications. Table 5 shows several recommended crystal frequencies for common output frequencies used on FC3W A100 devices. For best overall performance with FC3W A100 devices, Renesas recommends using a 68MHz crystal.

Table 5. Recommended Output Frequency / Crystal Frequency Pairs for FC3W A100 Devices

DPLL Mode	Output Frequency (MHz)	Recommended XTAL Frequencies (MHz)	Recommended VCO Frequency (GHz)
Jitter Attenuator	491.52, 245.76, 122.88	38.88	9.8304
	491.52, 245.76, 122.89	60	9.8304
	491.52, 245.76, 122.90	68	10321.92
	491.52, 245.76, 122.91	68	10321.92
	491.52, 245.76, 122.92	73	10321.92

2.2.2 FC3W A200 Frequency Parameters

FC3W A200 devices are recommended for wireline applications. Table 6 shows several recommended crystal frequencies for common output frequencies used on FC3W A200 devices. For the best overall performance with FC3W A200 devices, Renesas recommends using a 54MHz crystal for jitter attenuator mode applications and a 62.5MHz crystal for synthesizer mode applications.

Table 6. Recommended Output Frequency / Crystal Frequency Pairs for FC3W A200 Devices

DPLL Mode	Output Frequency (MHz)	Recommended XTAL Frequencies (MHz)	Recommended VCO Frequency (GHz)
Jitter Attenuator	625, 390.625, 312.5, 156.25	49.152	9.375
	625, 390.625, 312.5, 156.25	54	9.375
	625, 390.625, 312.5, 156.25	73	9.375
Synthesizer	625, 390.625, 312.5, 156.25	50	9.375
	625, 390.625, 312.5, 156.25	62.5	9.375

3. Load Capacitance

For FC3 and FC3W, Renesas recommends using a crystal that has a nominal load capacitance between 8pF and 10pF. FC3 and FC3W do not use physical tuning capacitors, but instead use an internal, adjustable load capacitance. The internal load capacitance can be adjusted in the programmed configuration file or via register writes to the device.

The total load capacitance can be modeled as seen in Figure 2, where C_{pcb1} and C_{pcb2} are the stray capacitance of the circuit board, C_{f1} and C_{f2} are the fixed capacitance internal to FC3/FC3W on each leg of the oscillator, C_{s1} and C_{s2} are the internal stray capacitance of the FC3/FC3W device, and C_{d1} and C_{d2} are the internal tuning caps (digicaps) of the FC3/FC3W device. For all capacitances, C_{xx1} refers to capacitances on the XIN pin and C_{xx2} refers to capacitances on the XOUT pin.

The load capacitance (C_L) for the XIN pin is:

$$C_L = \frac{1}{\frac{1}{C_{totalXIN}} + \frac{1}{C_{totalXOUT}}}$$

where

$$C_{totalXIN} = C_{f1} + C_{s1} + C_{d1} + C_{pcb1}$$

$$C_{totalXOUT} = C_{f2} + C_{s2} + C_{d2} + C_{pcb2}$$

For FC3 devices, C_{s1} = C_{s2} = 8.7pF, and for FC3W devices, C_{s1} = C_{s2} = 9.9pF. By default, it is assumed that C_{pcb1} = C_{pcb2} = 2.5pF for both FC3 and FC3W. The circuit board stray capacitance values can be manually changed by setting the values of **xin_pcb_capacitance** and **xout_pcb_capacitance** in the RICBox GUI.

The fixed capacitance varies slightly between FC3 and FC3W. For FC3 device, C_{f1} = C_{f2} = 5.5pF and the fixed capacitance is always present. For FC3W devices, C_{f1} = C_{f2} = 5.965pF and can be enabled/disabled. By default, the FC3W fixed capacitance is disabled.

For both FC3 and FC3W, the capacitance of the internal tuning capacitor for XIN can be controlled via the **TOP.XO.XO_CNFG.xobuf_digicap_x1** register and the capacitance of the internal tuning capacitor for XOUT can be controlled via the **TOP.XO.XO_CNFG.xobuf_digicap_x2** register. Note, the values of **TOP.XO.XO_CNFG.xobuf_digicap_x1** and **TOP.XO.XO_CNFG.xobuf_digicap_x2** are each a combination of the fixed capacitance and the internal tuning capacitance for each leg on the crystal.

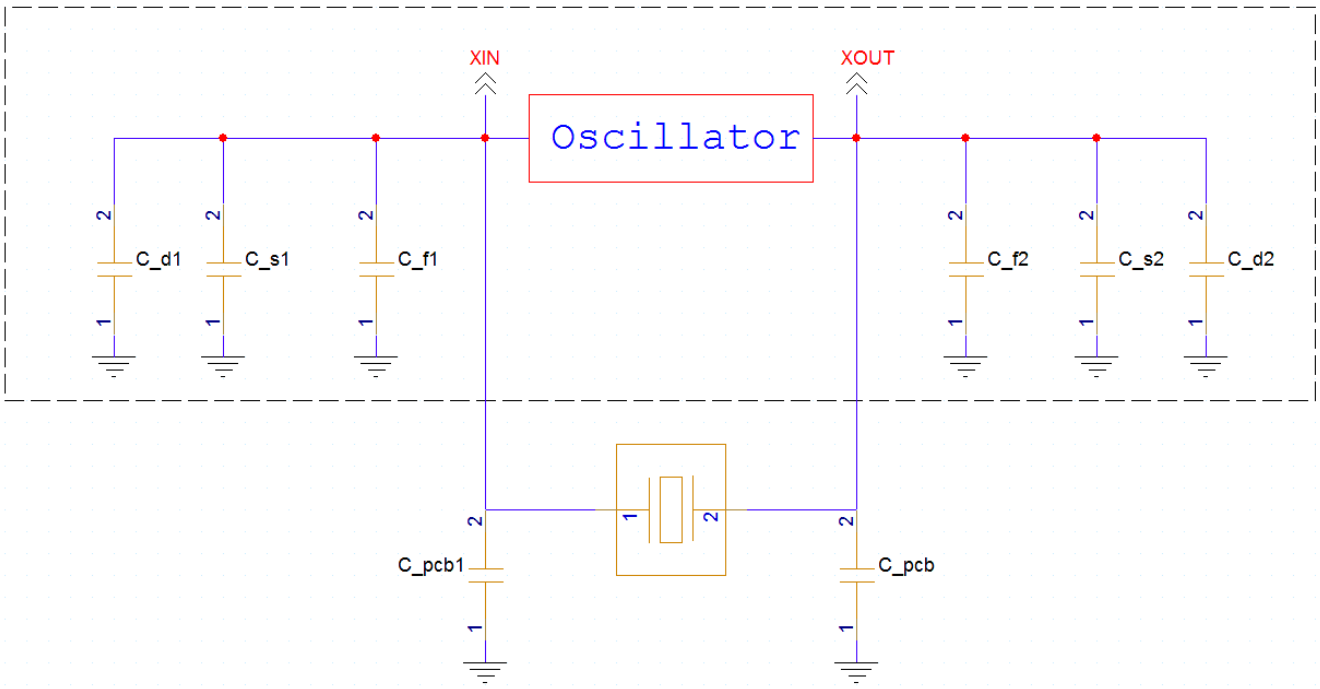

Figure 2: Crystal Capacitance

4. Equivalent Series Resistance

Equivalent series resistance (ESR) is the effective resistance component in series with the LC model of the crystal itself. ESR is determined by the crystal size, cut, frequency, and mode of vibration. An AT-cut crystal with a fundamental mode 50MHz resonance frequency in a 3225 package will have an ESR of around 50Ω, due to the size of crystal that easily fits into this package size. ESR subtracts from the negative resistance in the oscillator. A small package with a very small crystal may have too high an ESR for the driver, making it harder to start and sustain oscillation. A large package can fit a larger crystal (at the same cut, mode, and frequency) and will have a lower ESR.

ESR is proportional to the motional resistance (R_M) of the crystal and the shunt capacitance (C_O). It is also inversely proportional to the load capacitance (C_L). The ESR can be calculated as follows:

$$ESR = R_M \left(1 + \frac{C_O}{C_L}\right)^2$$

ESR is commonly expressed as a maximum value in ohms and is significant for two reasons.

1. The loop gain needed for an oscillator to start up and maintain oscillation is proportional to the ESR.
2. The drive level of an oscillator is proportional to the ESR. Therefore, if the ESR is too large, the crystal can have trouble oscillating or it can lead to a drive level which exceeds the rating that accelerates aging.

For FC3 and FC3W devices, the maximum ESR value that is recommended is 50Ω.

5. Drive Level

Confirm that the crystal maximum specified drive level will accommodate the drive level of the FC3 product. For FC3 and FC3W products, the typical drive strength is 160µW for a load capacitance of 8pF and 225µW for a load capacitance of 10pF. To prevent exceeding the drive level of the crystal, a series-damping resistor (R_S) can be added, but this series resistor will decrease the negative resistance and loop gain will increase phase noise. It is preferred to select a crystal that can tolerate the required drive strength. Adding an R_S, populated with a 0-ohm shunt allows the use of a series resistance if a suitable crystal cannot be sourced.

Exceeding the drive level on the crystal accelerates aging. Renesas recommends measuring the power dissipated in the crystal to ensure it is below the crystal maximum specification. For more information, see the Quartz Crystal Drive Level Application Note.

R_S should be a small surface mounted part (example 0201 or 0402) to minimize stray capacitance.

6. Using a Crystal Oscillator (XO) with FC3

A crystal oscillator (XO) can be used in place of a crystal with FC3 or FC3W. To use a XO with FC3 or FC3W, the crystal interface must be overdriven. When overdriving the crystal interface, the XOUT pin should be floated with no trace attached and the XIN input overdriven by an AC coupled LVCMOS driver, or, by one side of an AC coupled differential driver. The XIN pin is internally biased to 0.6V. The voltage swing on XIN should be between 0.6V peak-to-peak and 1.2V peak-to-peak; the slew rate should not be less than 0.6V/ns. The slew rate is calculated by measuring at the midpoint of the rising waveform using a window of ±50mV.

Note: The maximum allowable voltage on the XIN pin is 1.32V. Exceeding this voltage may damage the pin.

Figure 3 shows a 1.8V or 2.5V LVCMOS driver overdriving the XIN pin. For V_{DD} = 1.8V, considering the output impedance of the driver (R_O), the values of the series resistance (R_S) and R_1 should be chosen so that the voltage swing on XIN will be below 1.2V peak-to-peak. For V_{DD} = 2.5V, the sum of the output impedance of the driver (R_O) and the series resistance (R_S) can be made higher than R_1 so that the voltage swing on XIN will be below 1.2V peak-to-peak. Figure 4 shows one side of an LVPECL driver overdriving the XIN pin.

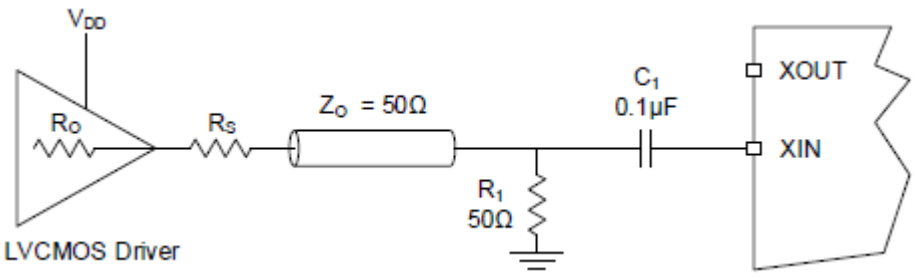

Figure 3. LVCMOS Driver to Crystal Input Interface

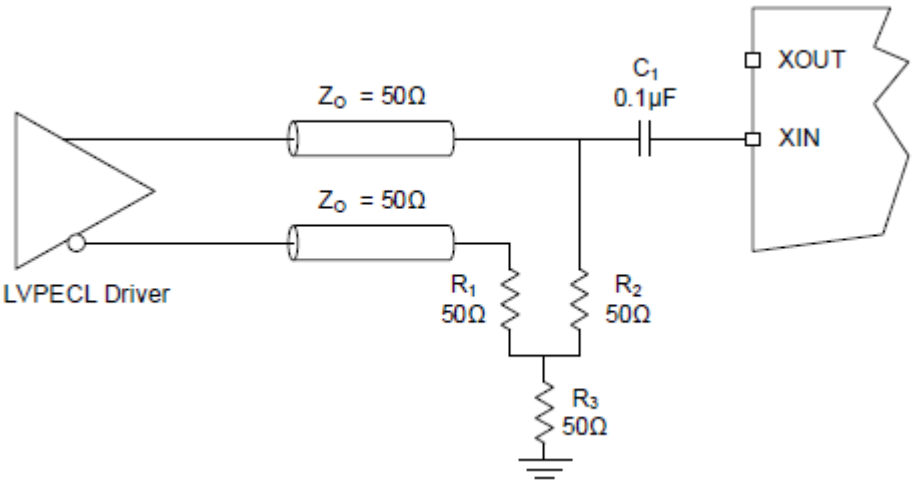

Figure 4. LVPECL Driver to Crystal Input Interface

It is recommended to AC couple the XIN pin of the FC3 or FC3W device by using a 0.1µF capacitor close to the device. The maximum XIN voltage is 1.3V peak-to-peak, and the recommended XIN voltage is 1.2V peak-to-peak. The XIN voltage can be controlled by using a 50ohm to ground voltage divider close to the device, but before the AC coupling capacitor. If the 50ohm to ground resistor does not provide enough resistance to meet the voltage limit, a series resistance can be place along the XIN trace between the XO and the 50ohm resistor. The value of the series resistance required will vary between XOs due to internal resistance from the XO. The series resistance can be calculated using voltage division. Figure 5 shows a generalized diagram of the path from the XO to the XIN pin on FC3 and FC3W.

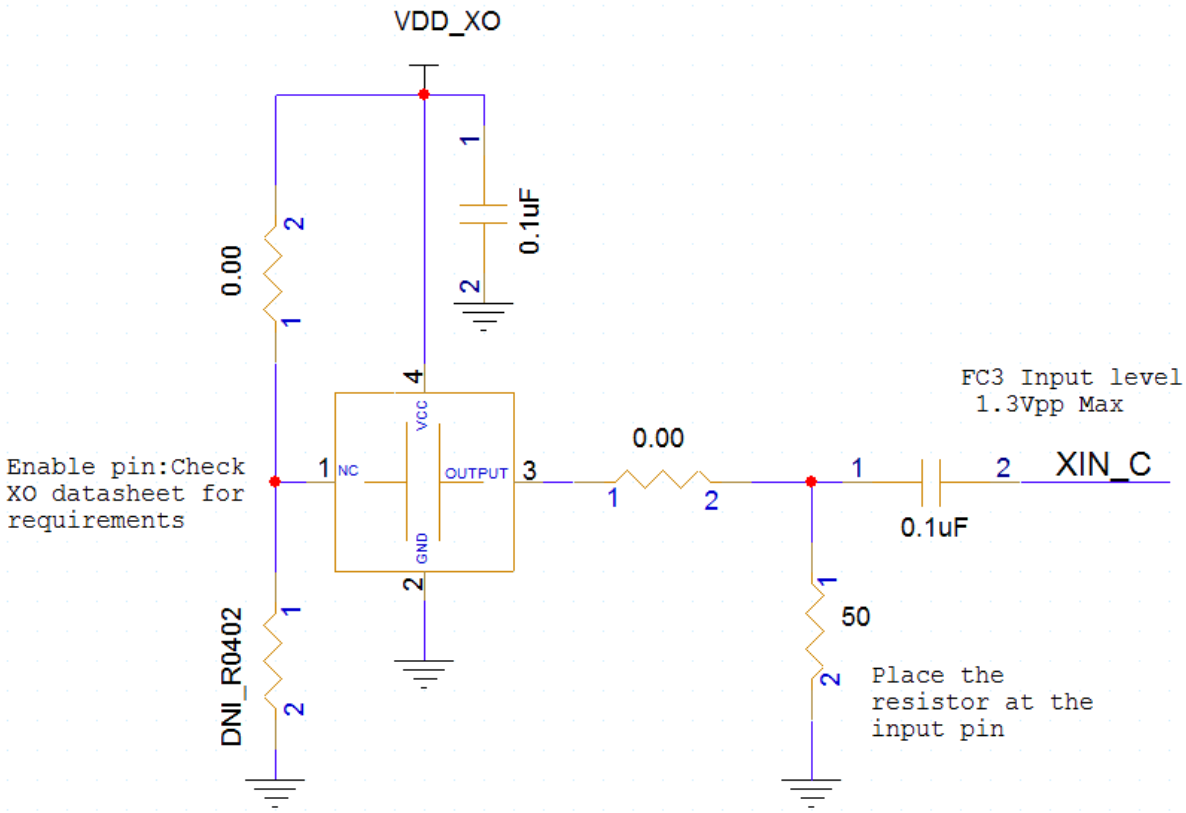

Figure 5. Generalization of Path from XO to the XIN Pin on FC3 and FC3W

7. Operating Temperature

Operating a crystal outside of its specified operating temperature range may prematurely age the crystal (increased ppm frequency change over time) or may damage the housing. A crystal operating outside of its temperature range can result in higher jitter frequency offset caused by the temperature. Crystal performance is typically not guaranteed beyond its specified temperature range. The recommended operating temperature range for FC3 and FC3W devices is -40°C to 85°C.

8. Frequency Tolerance

Select a manufacturing tolerance (maximum deviation from the specified resonant frequency at room temperature) and frequency shift over the operating temperature range (often called frequency stability) that is acceptable for the application. When tight frequency tolerances (< 10ppm) over the operating temperature range are a requirement, it may be necessary to use a TCXO (temperature compensated crystal oscillator) or OCXO (oven-controlled crystal oscillator) instead. For FC3 and FC3W devices, the crystal input frequency tolerance range is ±450ppm.

Note: For FC3 and FC3W products, the crystal or crystal oscillator at XIN is the jitter reference. The preference is to use a crystal for low jitter instead of a generated clock signal.

9. Aging

Confirm that the crystal aging tolerance (ppm per year) meets the application requirement. Exceeding the drive level on the crystal, as well as shock, vibration and operating the crystal outside of its specified temperature range, accelerates aging. If the crystal will experience shock or vibration in its application, consider an oven-controlled SC-cut crystal that is more tolerant of vibration.

10. Recommended Crystals (XTAL) and Crystal Oscillators (XO)

Table 7 provides a list of acceptable crystals for applications using a FC3 device. Table 8 provides a list of acceptable crystal oscillators for applications using a FC3 device.

Table 7. Recommended Crystals for FC3 and FC3W Applications

Manufacturer	Type	Part Number	Product Size (mm)	Frequency (MHz)	ESR (Ω)	CL (pF)	Typical Drive Level (µW)	Max. Drive Level (uW)	Freq. Tolerance (ppm)	Freq. Stability (ppm)	Aging (ppm/ year at 25°C)	Temp. Range (ºC)
NDK	XTAL	EXS00A-CS15517	2.0 × 1.6	49.152	50	9	10	200	±27			-40 to 85
NDK	XTAL	EXS00A-CS16476	2.0 × 1.6	50	30	9	10	200	±25			-40 to 85
NDK	XTAL	EXS00A-CS15524	2.0 × 1.6	54	30	9	10	200	±40			-40 to 85
NDK	XTAL	EXS00A-CS15287	2.0 × 1.6	60	30	9	10	200	±25			-40 to 85
NDK	XTAL	EXS00A-CS15295	2.0 × 1.6	62.5	35	9	10	200	±30			-40 to 85
NDK	XTAL	EXS00A-CS15306	2.0 × 1.6	68	50	9	10	200	±30			-40 to 85
NDK	XTAL	EXS00A-CS15308	2.0 × 1.6	73	50	9	10	200	±30			-40 to 85

Manufacturer	Type	Part Number	Product Size (mm)	Frequency (MHz)	ESR (Ω)	CL (pF)	Typical Drive Level (µW)	Max. Drive Level (uW)	Freq. Tolerance (ppm)	Freq. Stability (ppm)	Aging (ppm/ year at 25°C)	Temp. Range (ºC)
NDK	XTAL	EXS00A-CS15310	2.0 × 1.6	78.125	50	9	10	200	±30			-40 to 85
TXC	XTAL	7M49172003	3.2 × 2.5	49.152	20	8	100	300	±10	±15	±1	-40 to 85
TXC	XTAL	8Y49172005	2.0 x 1.6	49.152	30	12	100	300	±10	±15	±1	-40 to 85
TXC	XTAL	8Y49172006	2.0 x 1.6	49.152	30	8	100	300	±10	±15	±1	-40 to 85
TXC	XTAL	7M50072003	3.2 × 2.5	50	22	8	100	200	±10	±15	±1	-40 to 85
TXC	XTAL	8Y50072010	2.0 x 1.6	50	30	8	100	200	±10	±15	±1	-40 to 85
TXC	XTAL	8Y49172005	2.0 × 1.6	49.152	30	12	100	300	±10	±15	±1	-40 to 85
TXC	XTAL	7M54072002	3.2 × 2.5	54	50	8	100	200	±10	±15	±1	-40 to 85
TXC	XTAL	8Y54072007	2.0 x 1.6	54	40	8	100	300	±25			-40 to 85
TXC	XTAL	7M60072004	3.2 x 2.5	60	25	8	100	300	±10	±20	±1	-40 to 95
TXC	XTAL	8Y60072004	2.0 x 1.6	60	40	8	100	300	±20	±30	±1	-40 to 105
TXC	XTAL	8Y60072005	2.0 × 1.6	60	40	8	100	300	±25			-40 to 85
TXC	XTAL	7M62572001	3.2 x 2.5	62.5	50	8	100	300	±10	±20	±1	-40 to 85
TXC	XTAL	8Y62572001	2.0 x 1.6	62.5	40	8	100	300	±20	±30	±1	-40 to 105
TXC	XTAL	8Y62572002	2.0 × 1.6	62.5	40	8	100	300	±25			-40 to 85
TXC	XTAL	8Z62572001	2.5 × 2.0	62.5	40	8	100	300	±25			-40 to 85
TXC	XTAL	8Y68072001	2.0 × 1.6	68	40	8	100	300	±25			-40 to 85
TXC	XTAL	8Y73072002	2.0 × 1.6	73	40	8	100	300	±25			-40 to 85
TXC	XTAL	8Y73072001	2.0 x 1.6	73	40	8	100	300	±20	±30	±1	-40 to 105
TXC	XTAL	8Y78172001	2.0 × 1.6	78.125	40	8	100	300	±20	±30	±1	-40 to 105
TXC	XTAL	8Y78172002	2.0 × 1.6	78.125	40	8	100	300	±25			-40 to 85
KYOCERA	XTAL	CX2016SA50000	3.2 × 2.5	50	50	8	10	200	±15	±50	±1	-40 to 125

Table 8. Recommended Crystal Oscillators for FC3 and FC3W Applications

Manufacturer	Type	Part Number	Product Size (mm)	Frequency (MHz)	Voltage (V)	Total Frequency Stability (ppm)	Temperature Range (°C)
TXC	XO	8W48070009	2.5 x 2.0	48	3.3	±25	-40 to 85
TXC	XO	8W48070007	2.5 x 2.0	48	3.3	±50	-40 to 105
TXC	XO	8W49170004	2.5 × 2.0	49.152	3.3	±25	-40 to 85
TXC	XO	8W50070009	2.5 x 2.0	50	3.3	±25	-40 to 85
TXC	XO	8W50070006	2.5 x 2.0	50	3.3	±50	-40 to 105
TXC	XO	8W62570006	2.5 × 2.0	62.5	3.3	±50	-40 to 105
TXC	XO	8W62570007	2.5 x 2.0	62.5	3.3	±25	-40 to 85
TXC	XO	8W68070001	2.5 × 2.0	68	3.3	±50	-40 to 105
TXC	XO	8W73070001	2.5 × 2.0	73	3.3	±50	-40 to 105
NDK	XO	RNA5029A	2.5 × 2.0	49.152	3.3	±50	-40 to 105
NDK	XO	RNA5027A	2.5 × 2.0	50	3.3	±50	-40 to 105
NDK	XO	RNA5025A	2.5 × 2.0	48	3.3	±50	-40 to 105
NDK	XO	RNA5024A	2.5 × 2.0	54	3.3	±50	-40 to 105
NDK	XO	RNA5024F	2.5 × 2.0	68	3.3	±50	-40 to 105

11. Revision History

Revision	Date	Description
1.07	June 25, 2025	▪ Added several TXC XTALs to Table 7 ▪ Added several TXC XOs to Table 8
1.06	May 26, 2025	▪ Added EXS00A-CS15517 to Table 7 ▪ Added EXS00A-CS15524 to Table 7 ▪ Added RNA5024F to Table 8 ▪ Modified Freq. Tolerance, Freq. Stability, and Aging for all NDK XTALs in Table 7
1.05	Sep 13, 2024	Updated “Load Capacitance”.
1.04	Sep 4, 2024	Updated parameters for NDK XTAL EXS00A-CS16476 in Table 7.
1.03	Aug 30, 2024	▪ Updated typical and maximum load capacitance values in Table 1. ▪ Updated Load Capacitance section. ▪ Added Max Drive Level column to Table 7. ▪ Updated multiple parameters in Table 7 and Table 8.
1.02	Jun 14, 2024	▪ Added two rows for 49.152MHz XTAL specifications (part numbers 7M49172003 and 8Y49172005) to Table 7. ▪ Added 49.152MHz XO specifications (part number 8W49170004) to Table 8.
1.01	Jun 6, 2024	Completed numerous changes in support of adding FC3W recommendations.
1.00	Nov 17, 2023	Initial release.

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