ClockMatrix –Advanced Holdover Usage

This application note explains the types of holdover available in ClockMatrix™ devices, as well as the recommended usage of the advanced holdover feature for typical applications.

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1. Introduction

A DPLL goes into the holdover state when it has had a reference then the reference is lost (this is different from free-run where the DPLL never had a reference.) The DPLL then tries to maintain the frequency of the locked reference. Holdover frequency accuracy is dependent on the free-run frequency accuracy and the holdover implementation in the DPLL while the free-run frequency accuracy is only dependent on the master clock (TCXO/OCXO/XO/crystal).

2. Different Types of Holdover in ClockMatrix

The ClockMatrix devices support three different types of holdover: simple holdover, advanced holdover and manual offset.

In the *simple holdover* case, the last instantaneous fractional frequency offset (FFO) is held by the DCO (digitally controlled oscillator) when the reference is disqualified. This is not optimal for some wider digital loop filter bandwidths since a noise spike from a bad pulse as the signal is disabled at PHY input (for a telecom or Ethernet signal) may contaminate the last FFO. For very narrow bandwidths (20mHz and below), the main low pass filter will avoid any sudden changes to the filter output so simple holdover can be used.

Advanced holdover mode is recommended for designs when holdover performance is important and the oscillator can support a lower bandwidth than the main loop bandwidth. Advanced holdover mode has an additional holdover filter that processes the frequency offsets from the main loop filter. The holdover filter would be set to a smaller bandwidth. There is also a holdover history register, which is set in units of seconds. In ClockMatrix, the holdover history function has two storage locations where the output from the holdover filter is stored. The holdover history (time) value tells the firmware how often to switch to the other location. This mechanism allows the holdover calculation to disregard a corrupted holdover value by switching to a value calculated earlier.

For instance, if the history value is set to 5 seconds, the value from the holdover filter is stored every 5 seconds to alternating locations when the DPLL is in lock. When entering holdover, the DPLL sends an FFO value from between 5 seconds (the history setting) and 10 seconds (2 times the history setting) to the DCO.

If the holdover value is completely corrupted, then there is a holdover history clear bit. This would set the holdover frequency to be the same as the free-run frequency, however, this function is rarely used.

Like the main low pass filter, the holdover filter also has a settling time. The first-order approximations for the settling time for the recommended holdover bandwidth settings are:

Holdover Bandwidth (mHz)	Settling Time (s)
100	15
10	150
1.5	1300
0.18	10000

The user needs to wait for the settling time to guarantee a stable holdover value, but the value will be available after waiting for the holdover history time.

In the *manual offset* case, the holdover offset is set in a register.

3. Use of Advanced Holdover

For the settings of the advanced holdover feature for typical applications, see Timing Commander Configurations for Common Use Cases on Renesas.com. The advanced holdover mode is used in the G.8262 option 1, G.8262 option 2, G.8262.1 and G.8273.2 (write phase) use cases. Since the bandwidth for the GNSS Up-Convert Lock to 1Hz and GNSS (GPS) Measurement (APTS) modes is 20mHz, the simple holdover method is used. For the G.8273.4 (PTS) Write Frequency Mode, the mode is left as default (simple).

4. Related Documents

For more information, visit the ClockMatrix™ Timing Solutions page on our website.

5. Revision History

Revision	Date	Description
1.01	Mar 3, 2023	Changed scope of document.
-	Dec 10, 2020	Initial release.

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