Stepper Motor Driver
SLG47105

This application note describes how to create a bipolar stepper motor driver with current control using one HVPAK SLG47105. It is possible to switch between full step and microstep modes. It is shown how to configure the design to get 1/2, 1/4, 1/8, or 1/16 microstep. The driver also allows for direction change. The design features slow decay for full mode and mixed decay for microstep mode.

The application note comes complete with design files which can be found in the Reference section.

Contents

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1. Terms and Definitions

DFF	D Flip-Flop
HV	High Voltage
LUT	Look-up Table
OSC	Oscillator

2. References

For related documents and software, please visit: HVPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .hvp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] Go Configure Software Hub, Software Download, and User Guide
[2] AN-CM-295 Stepper Motor Driver.hvp, GreenPAK Design File
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG47105 Datasheet, Renesas Electronics

3. Introduction

A stepper motor is a brushless DC electric motor that divides every revolution into a number of equal steps. The motor's position can then be commanded to move and hold at one of these steps without any position sensor for feedback (an open-loop controller), as long as the motor is carefully sized for the application in terms of torque and speed.

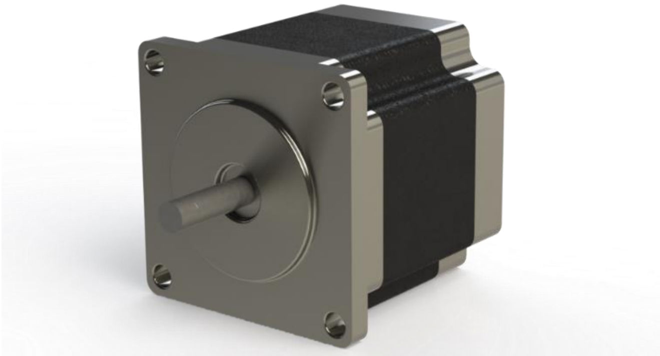

Figure 1. Stepper Motor

A typical stepper motor can be used in two modes: full step and microstep. The microstep mode allows the rotor to rotate on a smaller angle than in full step mode, making the rotation smoother. The SLG47105 provides full step mode and microstep modes of 1/2, 1/4, 1/8, and 1/16 steps. Besides, it is possible to choose between full and microstep modes in one design.

Stepper motors can be divided into two classes according to the type of winding: bipolar and unipolar steppers.

Unipolar stepper motors have one winding with the center tap per phase. Each section of windings is switched on for each direction of the magnetic field. Because in this arrangement a magnetic pole can be reversed without switching the direction of current, the commutation circuit can be made very simple for each winding. Usually, given a phase, the center tap of each winding is made common, giving three leads per phase and six leads for a typical two-phase motor. These two-phase commons are often connected internally, so the motor has only five external leads.

Bipolar stepper motors have a single winding per phase. To reverse a magnetic pole, the current in a winding needs to be reversed. Therefore, the control circuit must be more complicated. There are two leads per phase, and none is common. This application note describes how to create a bipolar stepper motor driver.

4. Operating Principle

In this application note, it is shown how to configure the SLG47105 to get microstep modes of 1/2, 1/4, 1/8, and 1/16 steps.

The internal design structure can be divided into several parts:

- Step/Microstep block that controls full step and microstep modes. In full step mode, one pulse on the STEP input corresponds to one step for the stepper motor. In microstep mode, one step is divided into the corresponding number of microsteps, which increases rotation accuracy.
- Winding Control block that ensures the correct winding energizing sequence depending on the selected mode and direction.
- CCMPs, PWMs with RegFile, and PWM choppers control the current in two windings with the help of external resistors and set the sine current waveform. RegFile holds the CCMP Vref values required to create a 1/4 sine wave. The PWM block selects the value from the RegFile and sets this value as the Current CMP reference. When the current exceeds the required value, the PWM chopper will chop the output voltage to decrease the output current.
- Internal logic and HV GPOs toggle the current sine polarity and rotation direction (depending on the Direction input pin state).

- Decay logic. In full step mode, slow decay is used. In microstep mode, the slow decay is used when the sine goes up, and the mixed decay when the sine goes down.
- True zero. It is impossible to set the 0 mV Vref in the RegFile, so the true zero step is added using internal logic.

The stepper motor driver's typical circuit is shown in Figure 2. It requires only two external resistors for current sensing.

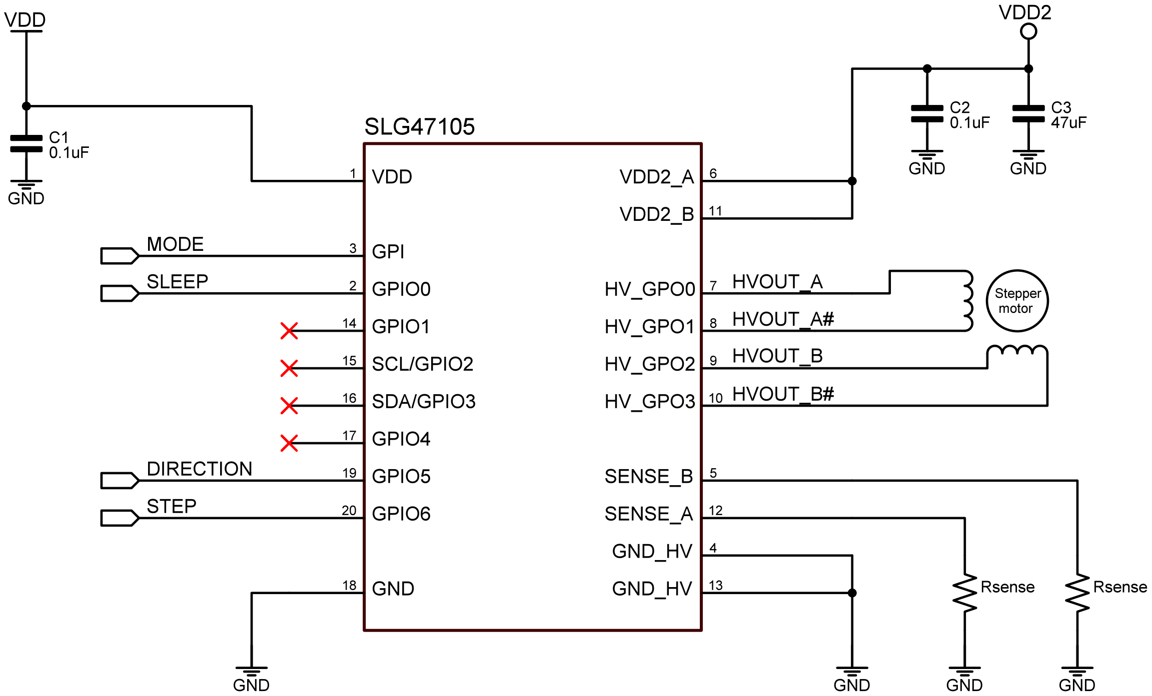

Figure 2. Stepper Motor Driver Typical Circuit

The design has four inputs for motor control:

1. PIN3 MODE – to select the stepper motor operation mode. HIGH signal level = full step operation, LOW signal level = microstep operation.

2. PIN2 SLEEP – to disable the driver. HIGH signal level = sleep mode, LOW signal level = active mode.

3. PIN19 DIRECTION – to change the direction of motor rotation. HIGH = forward, LOW = reverse.

4. PIN20 STEP – motor rotates by one step or microstep every rising edge using this input.

4.1 Microstep 1/2 GreenPAK Design

4.1.1. Description

The GreenPAK design for the 1/2 microstep is shown in Figure 3.

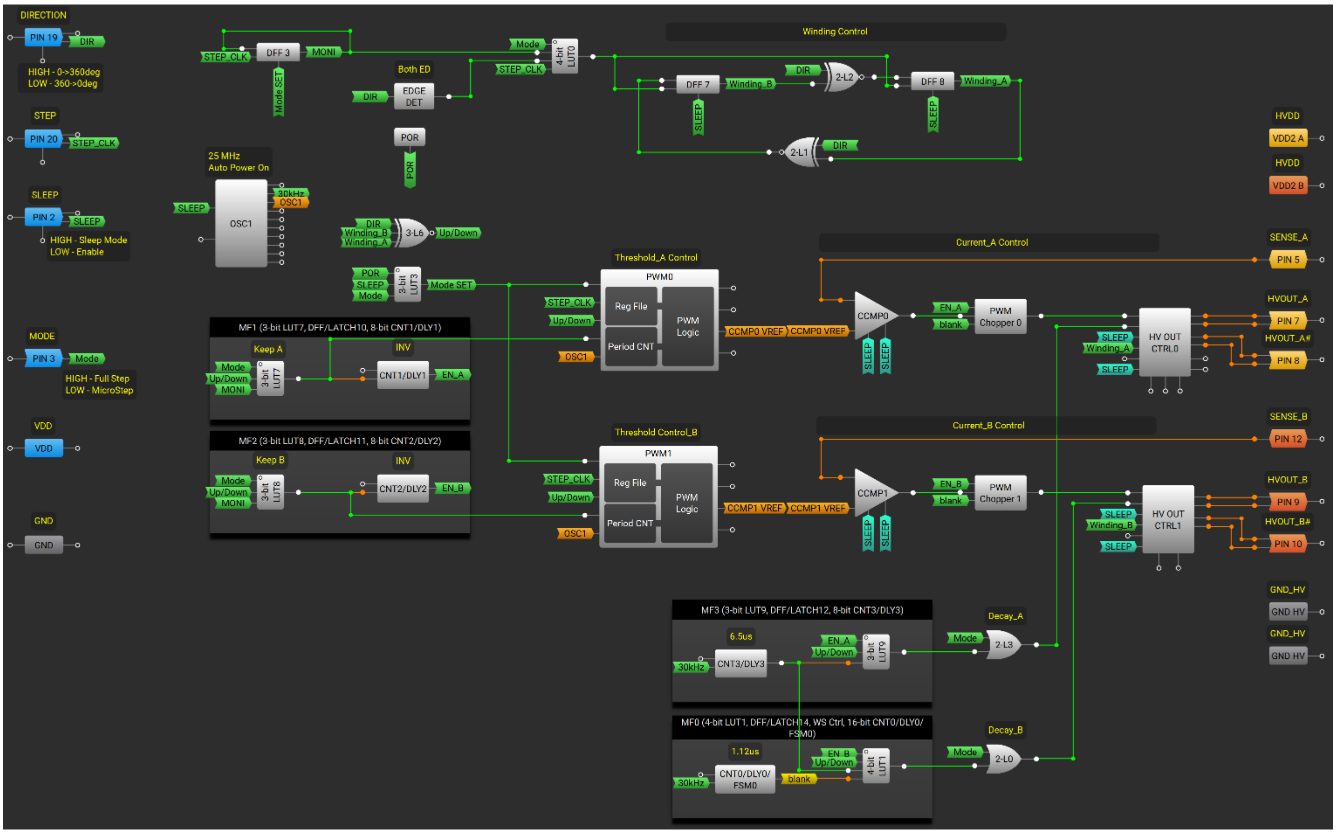

Figure 3. Stepper Motor Driver (Microstep – 1/2) GreenPAK Design

Figure 4 shows the timing diagram of the stepper motor driver operation in the full step mode.

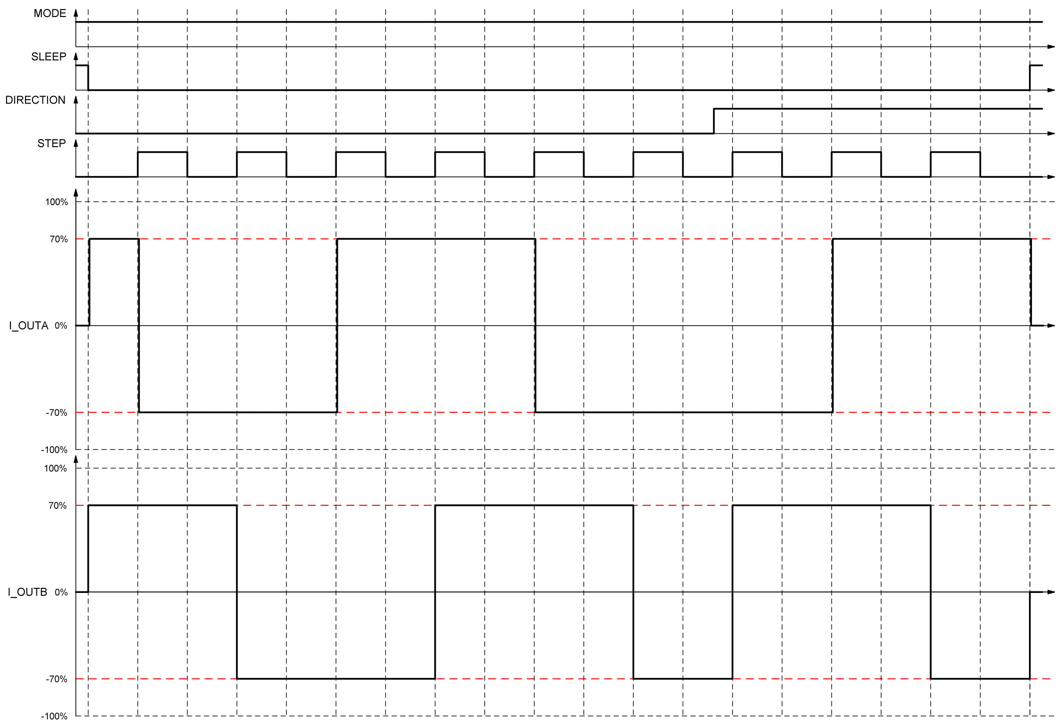

Figure 4. Full Step Timing Diagram

Figure 5 shows the timing diagram of the stepper motor driver operation in the 1/2 microstep mode.

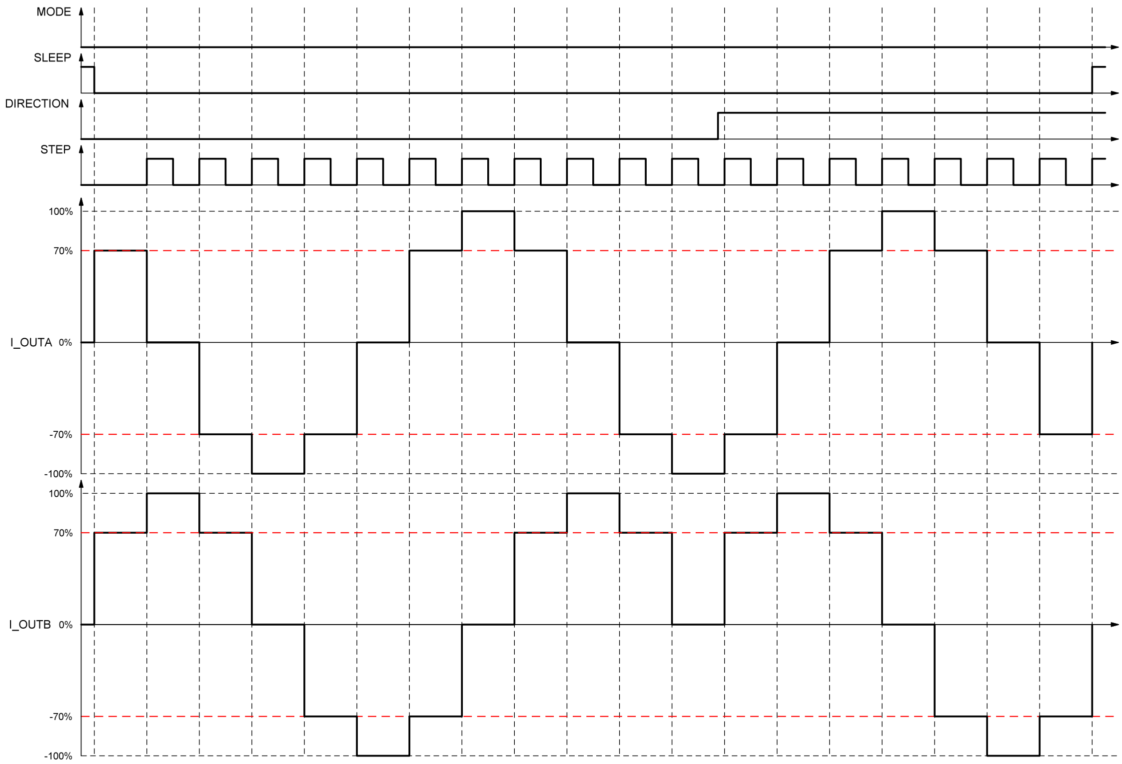

Figure 5. Microstep of 1/2 Timing Diagram

The DFF7, DFF8, 2-bit LUT1, and 2-bit LUT2 form the winding control block. Winding_A and Winding_B outputs are used for the phase selection in the HV OUT CTRL blocks and Up/Down generation by the 3-bit LUT6. The Up/Down signal also depends on the direction, which is set by PIN19. The Up/Down signal determines in which direction the sine should move and switches the CCMP Vref thresholds in the RegFile accordingly. The Winding Control block also sets the winding home position.

The DFF3 divides the STEP_CLK frequency by 2, creating a switching signal MONI for the Winding Control block. Thus, in the full step mode, the sequence will change each rising edge on the STEP input (PIN 20). In the microstep mode, it will change every two clocks. The logic selection is provided by 4-bit LUT0.

PWM0 controls the winding A (Winding_A signal, HV OUT CRL0). PWM1 controls the winding B (Winding_B signal, HV OUT CRL1). The RegFile is filled with CCMP Vref values for 1/2 microstep mode. The initial byte for PWM0 is 0, and for PWM1 is 15, and it corresponds to 71% current – home position. The 3-bit LUT3 forms the Mode SET signal, which is connected to the PWR DWN inputs of the PWM macrocells. It powers down the PWMs if there is no POR, the SLEEP signal is HIGH, or Mode = 1 (full step mode). It means that in full step mode, the PWMs are in sleep mode and the CCMP Vrefs are equal to the value stored in the initial byte of the RegFile – 71% current.

The PWM0 uses LSB, and the PWM1 uses MSB. LSB and MSB parts are filled with the same values, but in a different order: LSB in ascending order, while MSB in descending order. This allows the same Up/Down signal to be used for both PWMs, because if the current in one winding increases, then in the other it decreases, and vice versa.

The Duty Cycle CLK inputs of the PWMs are connected to the STEP input (PIN 20) STEP_CLK signal. Every rising edge of the step clock, the PWM blocks move to the next CCMP threshold. The 3-bit LUT7 and 3-bit LUT8 are used to create keep signals for PWM blocks. When the CCMP Vref reaches the lowest value, the HIGH signal for one step clock is generated, thus keeping this threshold for one more clock. Meanwhile, the CNT1/DLY1 and CNT2/DLY2 are configured as inverters and invert the keep signals, creating enable signals for A and B windings. These signals are HIGH during all microsteps except “zeros”.

The enable signals EN_A and EN_B go to the PWM inputs of PWM Chopper 0 and PWM Chopper 1, respectively. CCMP0 and CCMP1 outputs are connected to the CHOP inputs of PWM Chopper 0 and PWM Chopper 1, respectively. CCMPs outputs are HIGH when the current exceeds the Iref threshold value.

$$Iref = Vref\ (100\%)\ /\ GAIN\ /\ R_{sense}$$

The Vref values are set dynamically from the PWMs.

The CNT0/DLY0/FSM0 is configured as a falling-edge delay and forms a 1.12 us, 30 kHz blank signal for PWM Choppers. The PWM Choppers outputs are connected to the EN inputs of the HV OUT CTRL0 and HV OUT CTRL1 accordingly.

The CNT3/DLY3 is configured as a 6.56 us one-shot and used to create a mixed decay when the sine goes down in microstep mode. Note that the duration can be changed depending on the motor used. When the sine goes up, the slow decay is used. This logic is ensured by the 3-bit LUT9 and 4-bit LUT1. In full step mode, only slow decay is used. This logic is ensured by the 2-bit LUT3 and 2-bit LUT0.

4.1.2. Test Results

Figure 6 shows the test results of the full mode operation.

D3 (red/top line) – MODE (PIN 3)

D2 (green/2nd line) – SLEEP (PIN 2)

D1 (yellow/3rd line) – DIRECTION (PIN 19)

D0 (blue/4th line) – STEP (PIN 20)

Ch1 (green/5th line) – current through HV GPO0 (PIN 7), in Amperes

Ch2 (yellow/6th line) – current through HV GPO2 (PIN 9), in Amperes

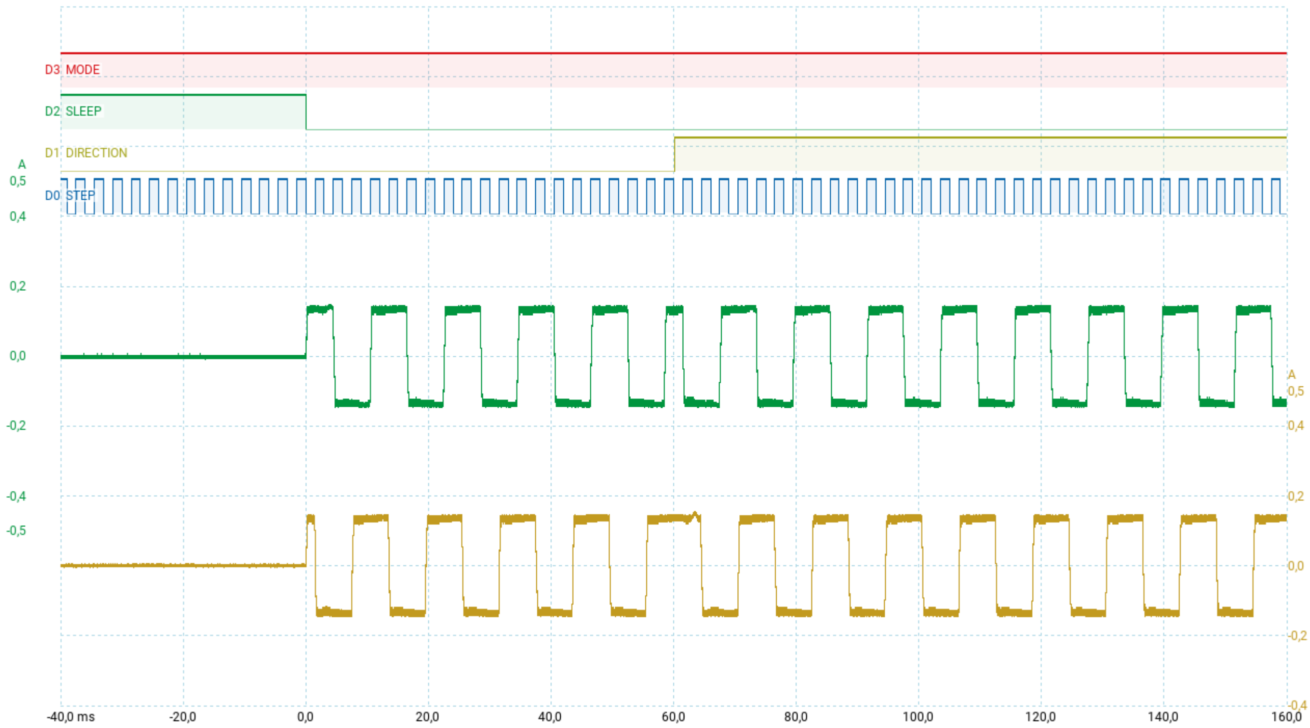

Figure 6. Full Step Start and Direction Change

Figure 7-Figure 9 show the ½ microstep operation.

D3 (red/top line) – MODE (PIN 3)

D2 (green/2nd line) – SLEEP (PIN 2)

D1 (yellow/3rd line) – DIRECTION (PIN 19)

D0 (blue/4th line) – STEP (PIN 20)

Ch1 (green/5th line) – current through HV GPO0 (PIN 7), in Amperes

Ch2 (yellow/6th line) – current through HV GPO2 (PIN 9), in Amperes

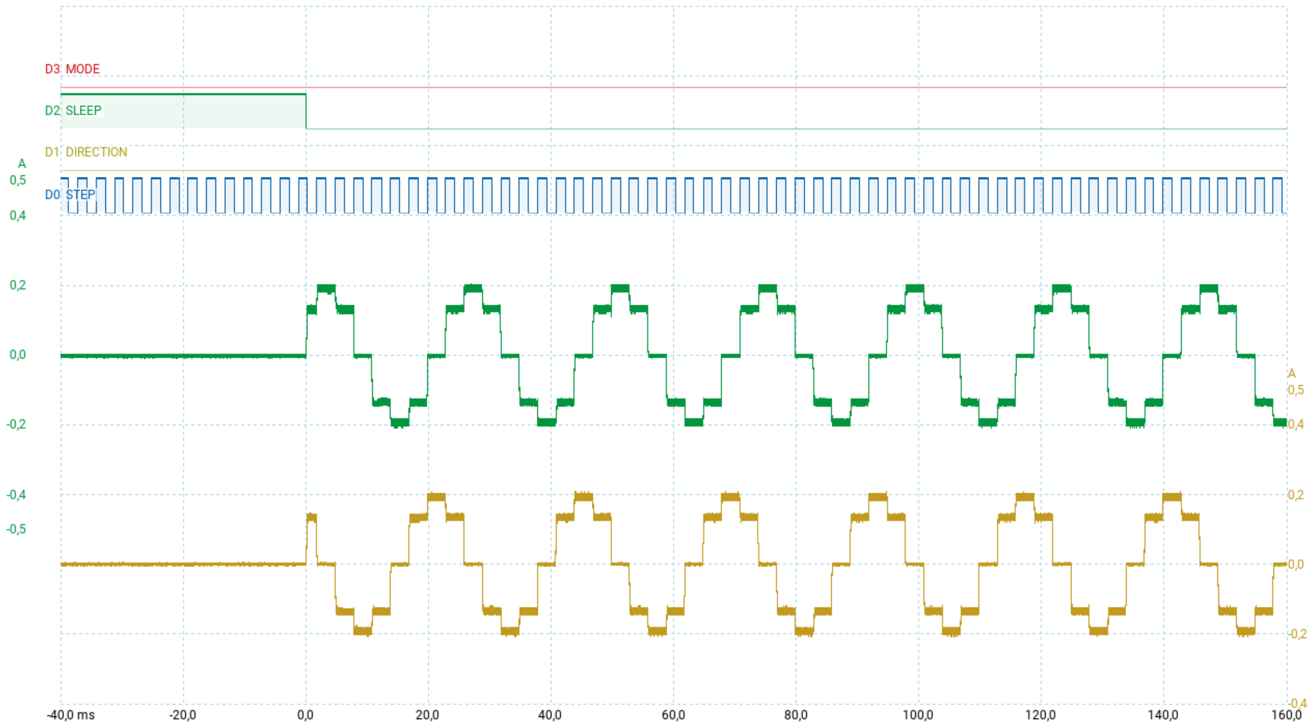

Figure 7. Microstep (1/2) Start, DIRECTION = 0

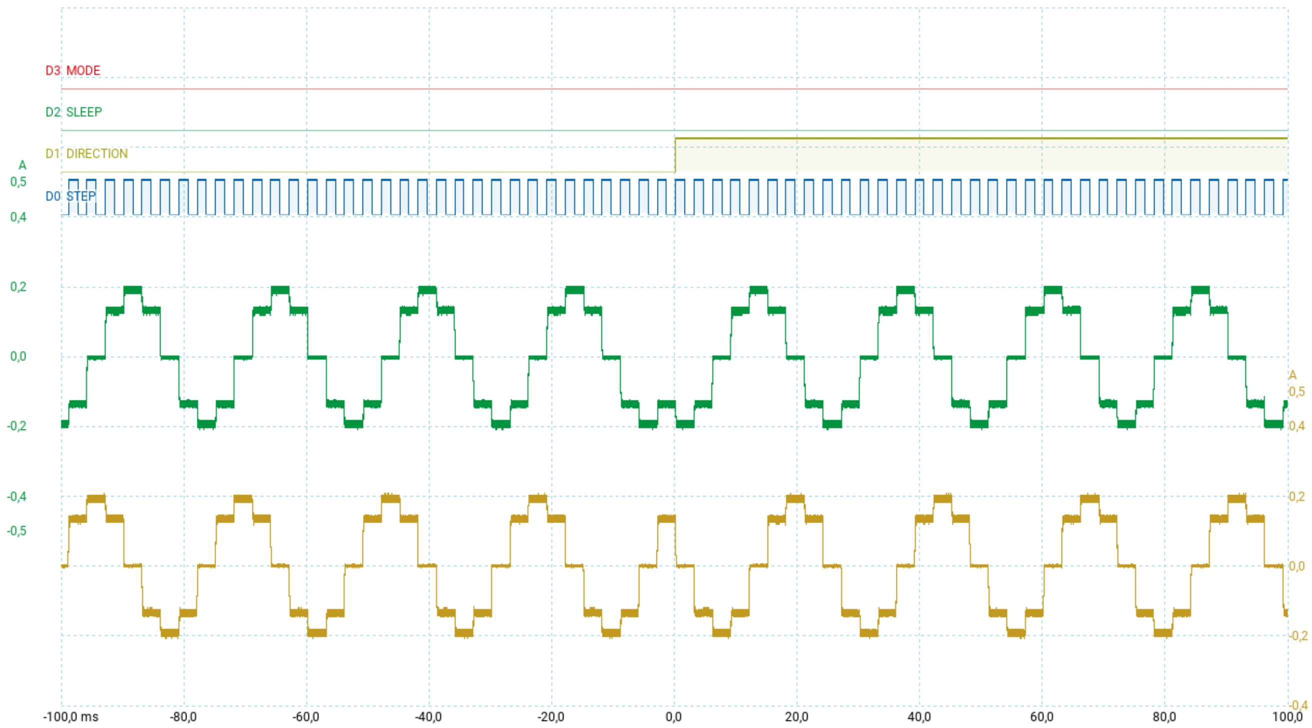

Figure 8. Microstep (1/2) Direction Change

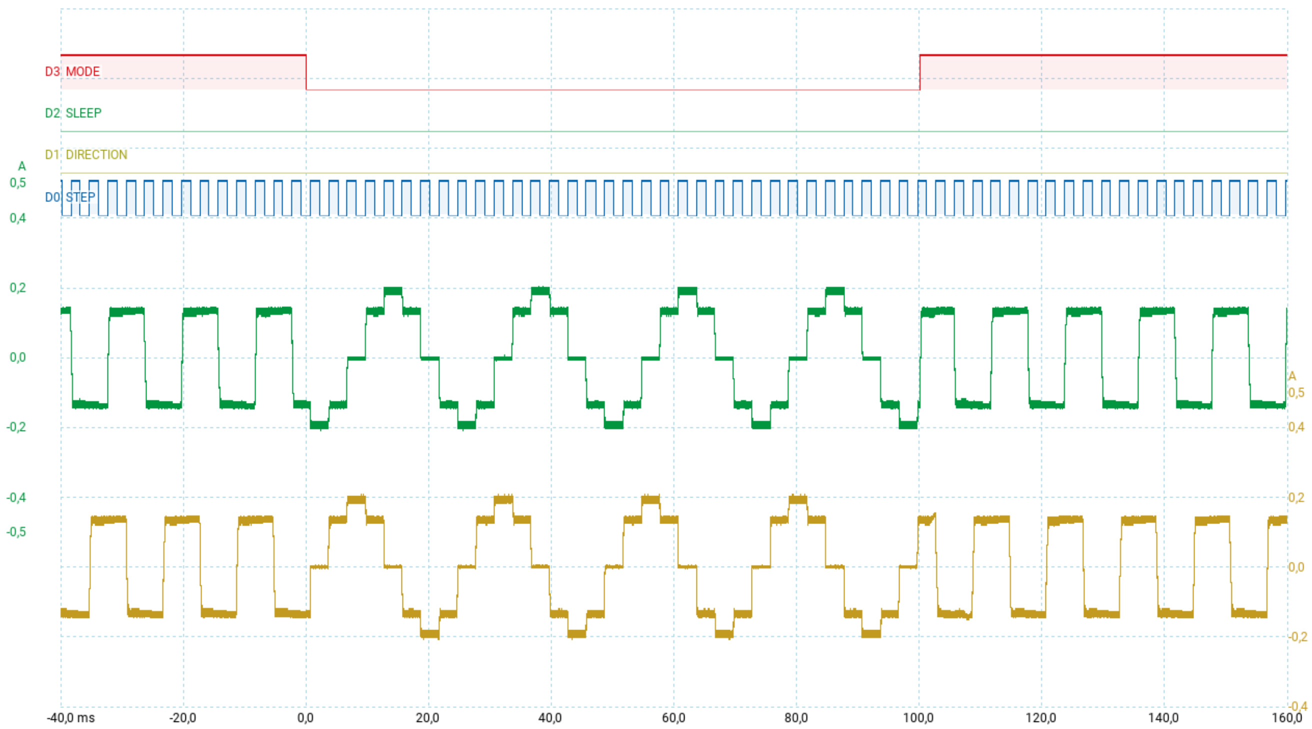

Figure 9. Microstep (1/2) and Full Step Switch

4.2 Microstep 1/4 GreenPAK Design

4.2.1. Description

To create a 1/4 microstep mode, only the microstep clock, PWM macrocells, and RegFile configuration must be changed. All other logic stays the same. The GreenPAK design for the 1/4 microstep is shown in Figure 10.

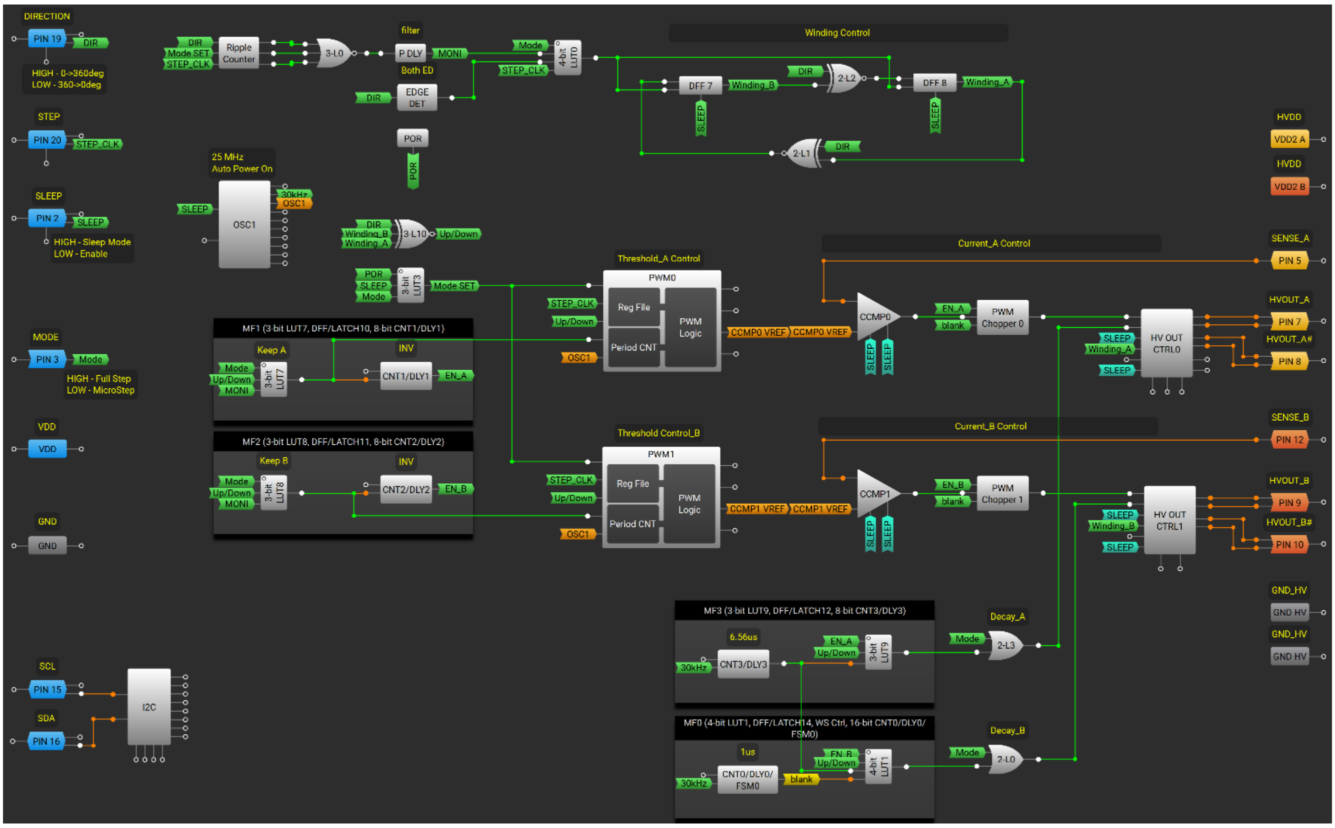

Figure 10. Stepper Motor Driver (Microstep – 1/4) GreenPAK Design

Figure 11 shows the timing diagram of the stepper motor driver operation in the 1/4 microstep mode.

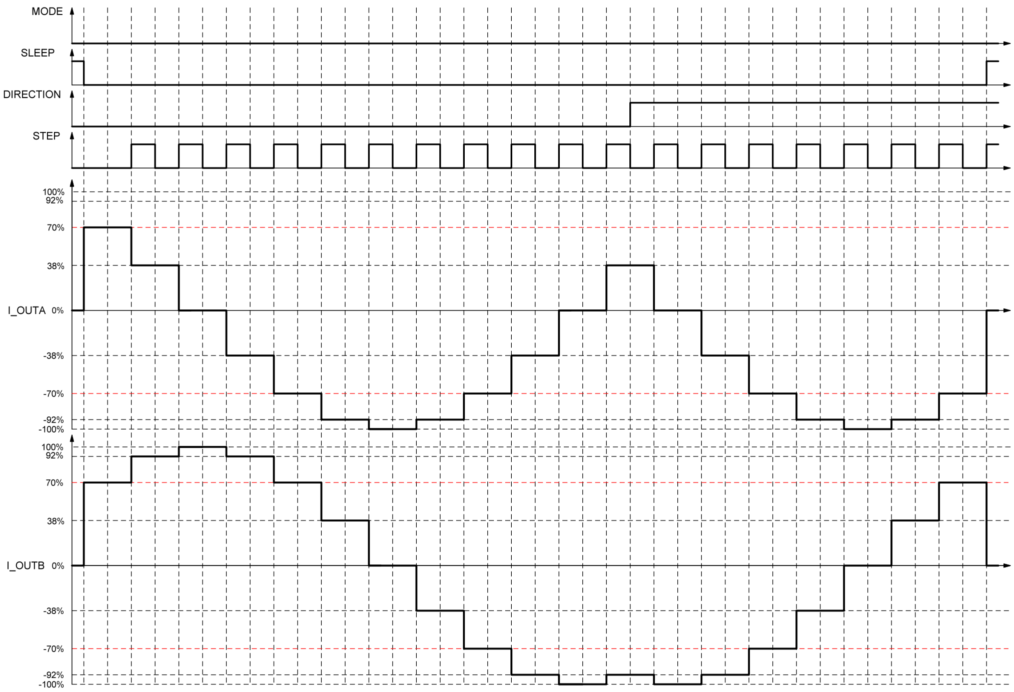

Figure 11. Microstep of 1/4 Timing Diagram

The DFF3, which divides the STEP_CLK frequency by 2 in the 1/2 microstep, is changed to the Ripple Counter with 3-bit LUT0 and a filter on the P DLY to create a divider by 4 with a possibility to change direction. This block is a new switching signal MONI for the Winding Control block. Thus, in the full step mode, the sequence will change each rising edge on the STEP input (PIN 20). In the microstep mode, it will change every four clocks. The logic selection is provided by 4-bit LUT0.

The RegFile is now filled with CCMP Vref values for 1/4 microstep mode. The initial byte for PWM0 is 1, and for PWM1 is 14, and it corresponds to 71% current – home position.

4.2.2. Test Results

Figure 12-Figure 14 show the 1/4 microstep operation.

D3 (red/top line) – MODE (PIN 3)

D2 (green/2nd line) – SLEEP (PIN 2)

D1 (yellow/3rd line) – DIRECTION (PIN 19)

D0 (blue/4th line) – STEP (PIN 20)

Ch1 (green/5th line) – current through HV GPO0 (PIN 7), in Amperes

Ch2 (yellow/6th line) – current through HV GPO2 (PIN 9), in Amperes

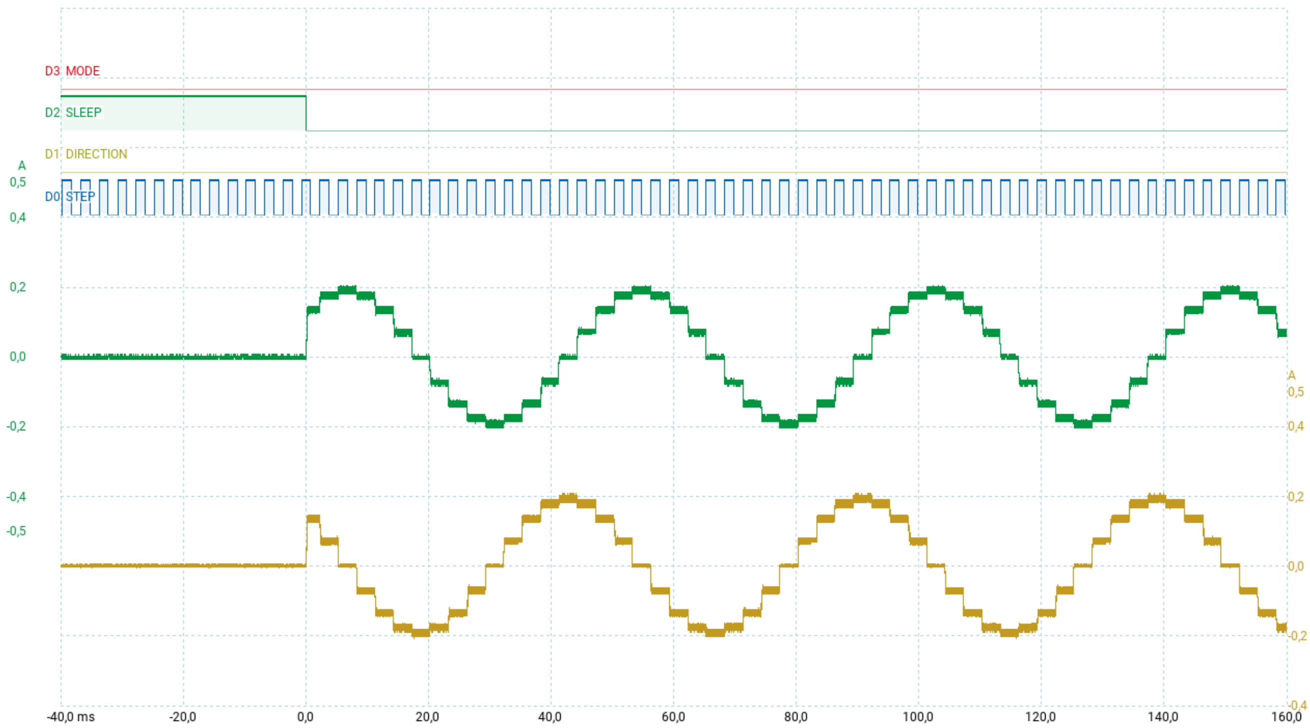

Figure 12. Microstep (1/4) Start, DIRECTION = 0

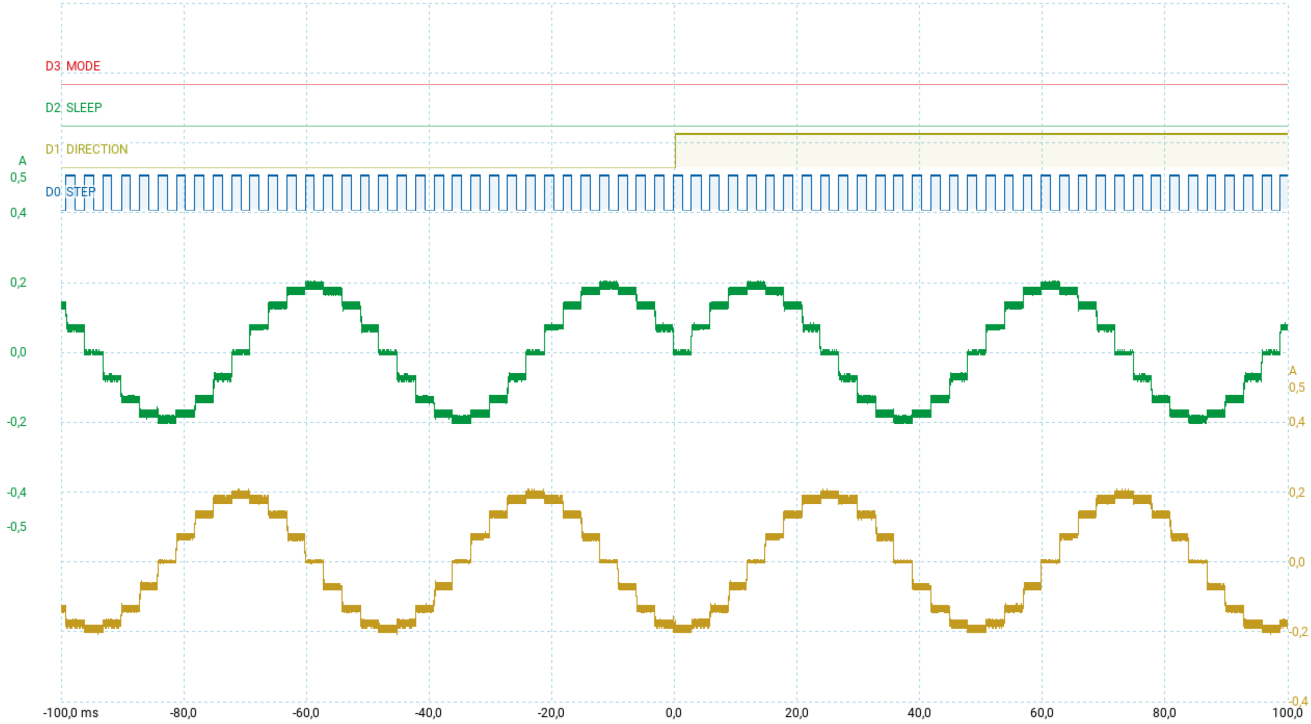

Figure 13. Microstep (1/4) Direction Change

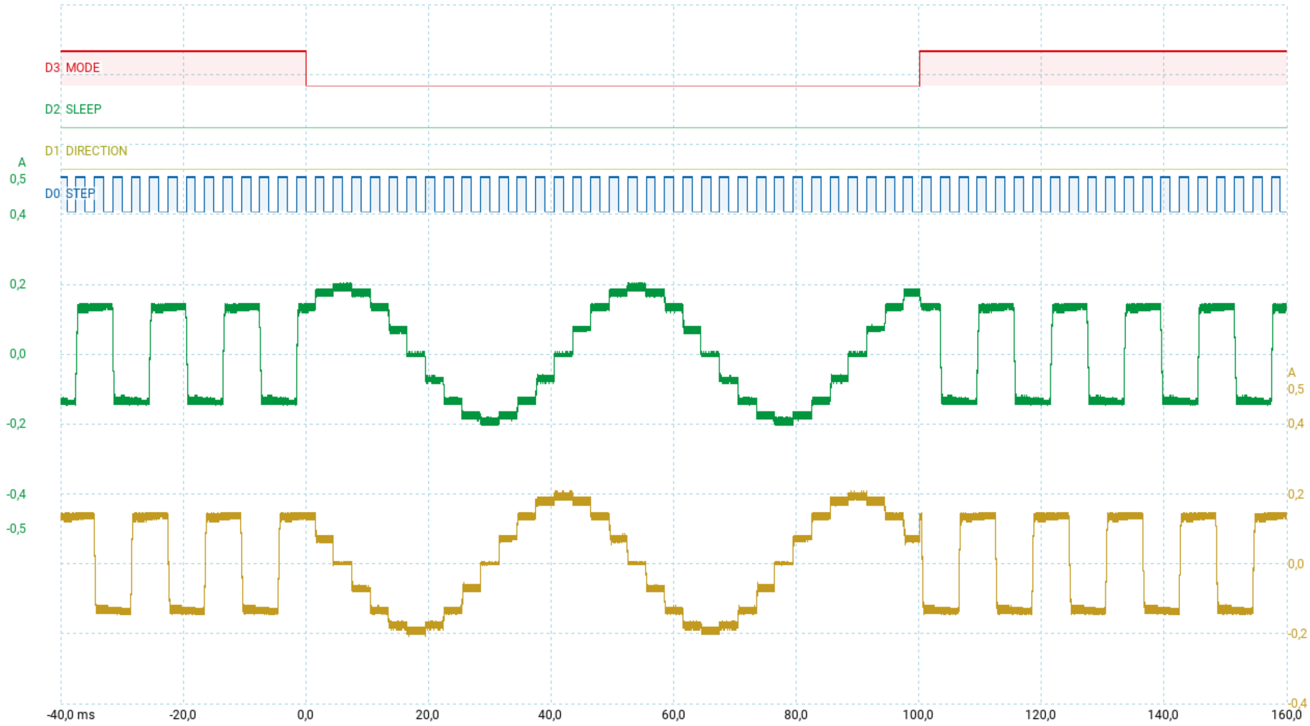

Figure 14. Microstep (1/4) and Full Step Switch

4.3 Microstep 1/8 GreenPAK Design

4.3.1. Description

To create a 1/8 microstep mode, only the microstep clock, PWM macrocells, and RegFile configuration must be changed. All other logic stays the same. The GreenPAK design for the 1/8 microstep is shown in Figure 15.

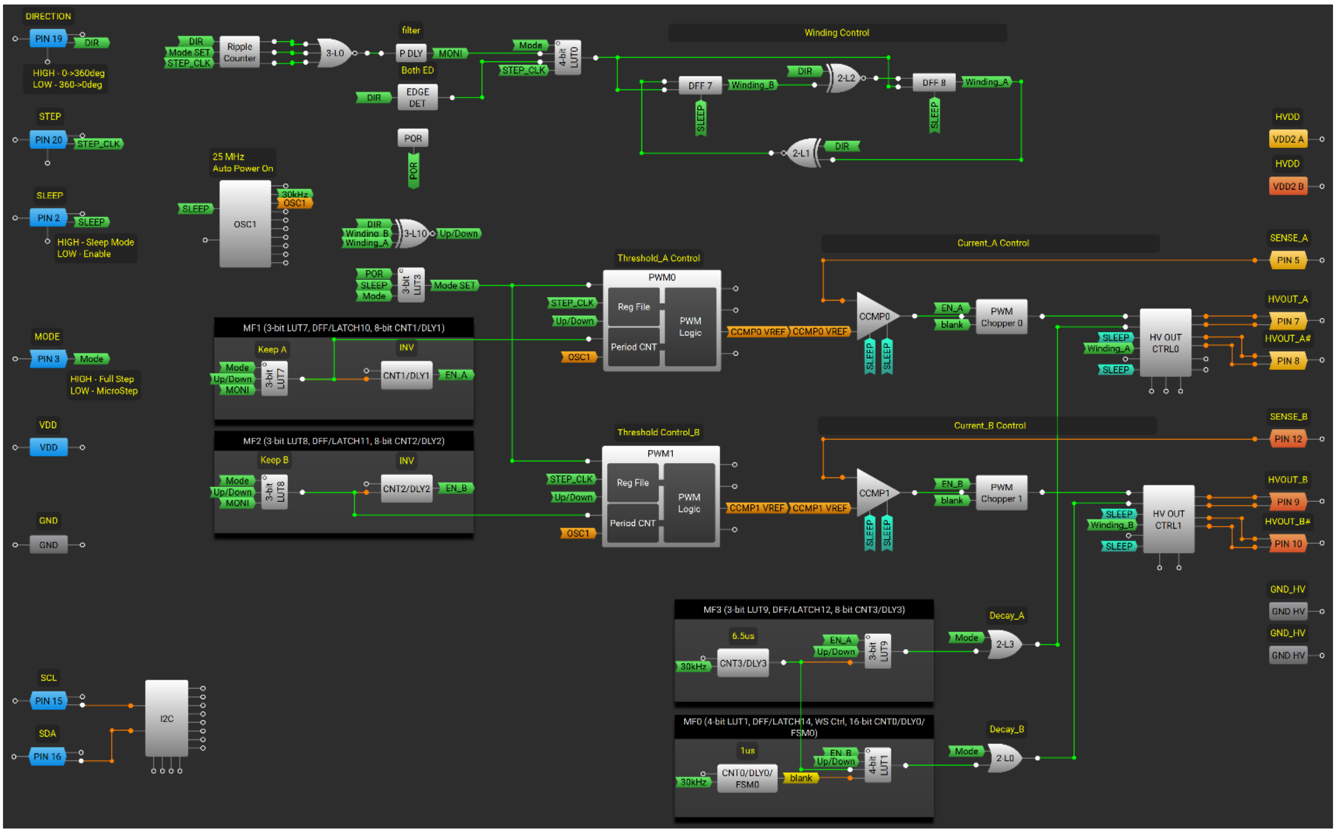

Figure 15. Stepper Motor Driver (Microstep – 1/8) GreenPAK Design

Figure 16 shows the timing diagram of the stepper motor driver operation in the 1/8 microstep mode.

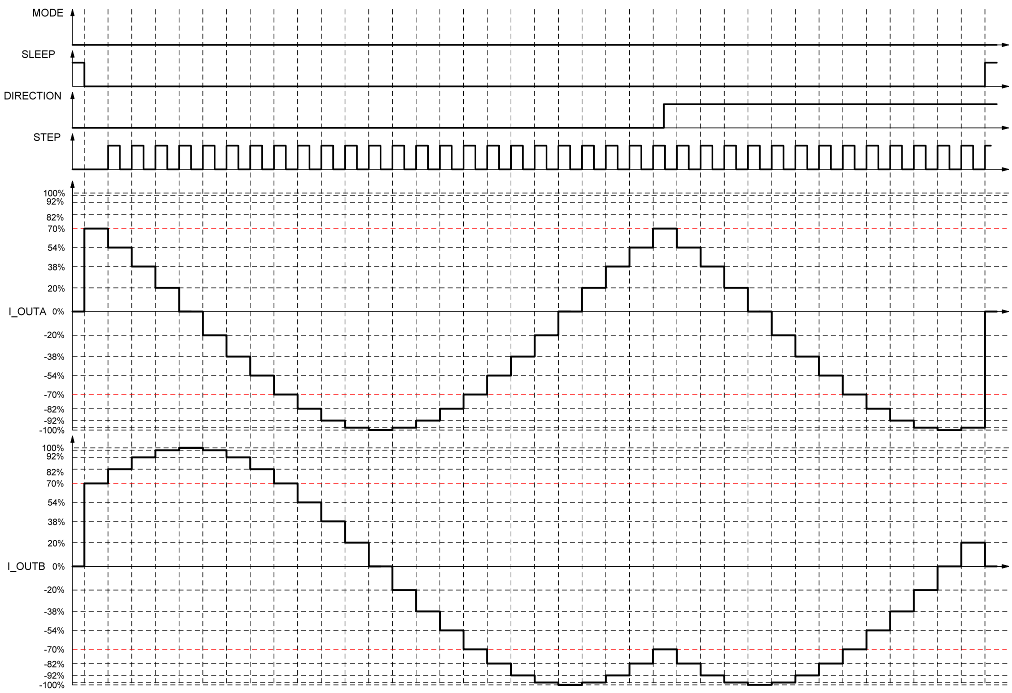

Figure 16. Microstep of 1/8 Timing Diagram

The Ripple Counter, which divides the STEP_CLK frequency by 4 in the 1/4 microstep, is reconfigured to create a divider by 8 with a possibility to change direction. This block with the 3-bit LUT0 and filter on the P DLY is a switching signal MONI for the Winding Control block. Thus, in the full step mode, the sequence will change each rising edge on the STEP input (PIN 20). In the microstep mode, it will change every eight clocks. The logic selection is provided by 4-bit LUT0.

The RegFile is now filled with CCMP Vref values for 1/8 microstep mode. The initial byte for PWM0 is 3, and for PWM1 is 12, and it corresponds to 71% current – home position.

4.3.2. Test Results

Figure 17-Figure 19 show the 1/8 microstep operation.

D3 (red/top line) – MODE (PIN 3)

D2 (green/2nd line) – SLEEP (PIN 2)

D1 (yellow/3rd line) – DIRECTION (PIN 19)

D0 (blue/4th line) – STEP (PIN 20)

Ch1 (green/5th line) – current through HV GPO0 (PIN 7), in Amperes

Ch2 (yellow/6th line) – current through HV GPO2 (PIN 9), in Amperes

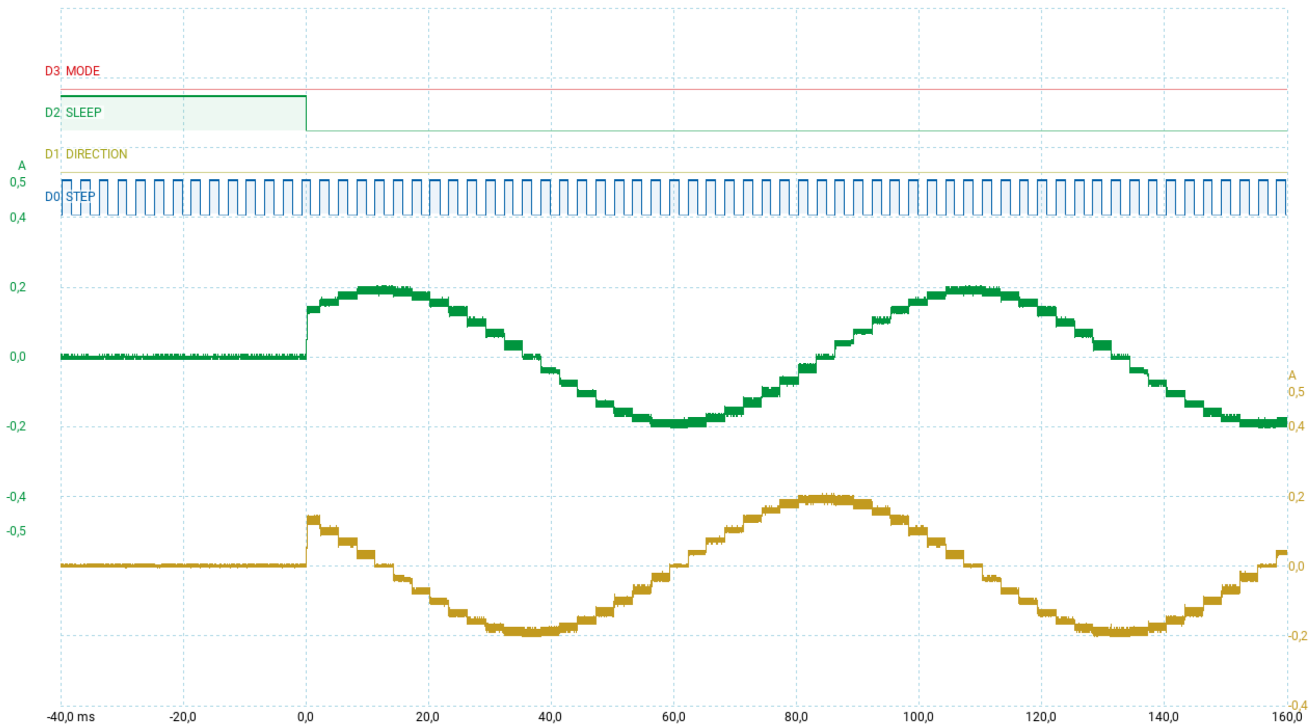

Figure 17. Microstep (1/8) Start, DIRECTION = 0

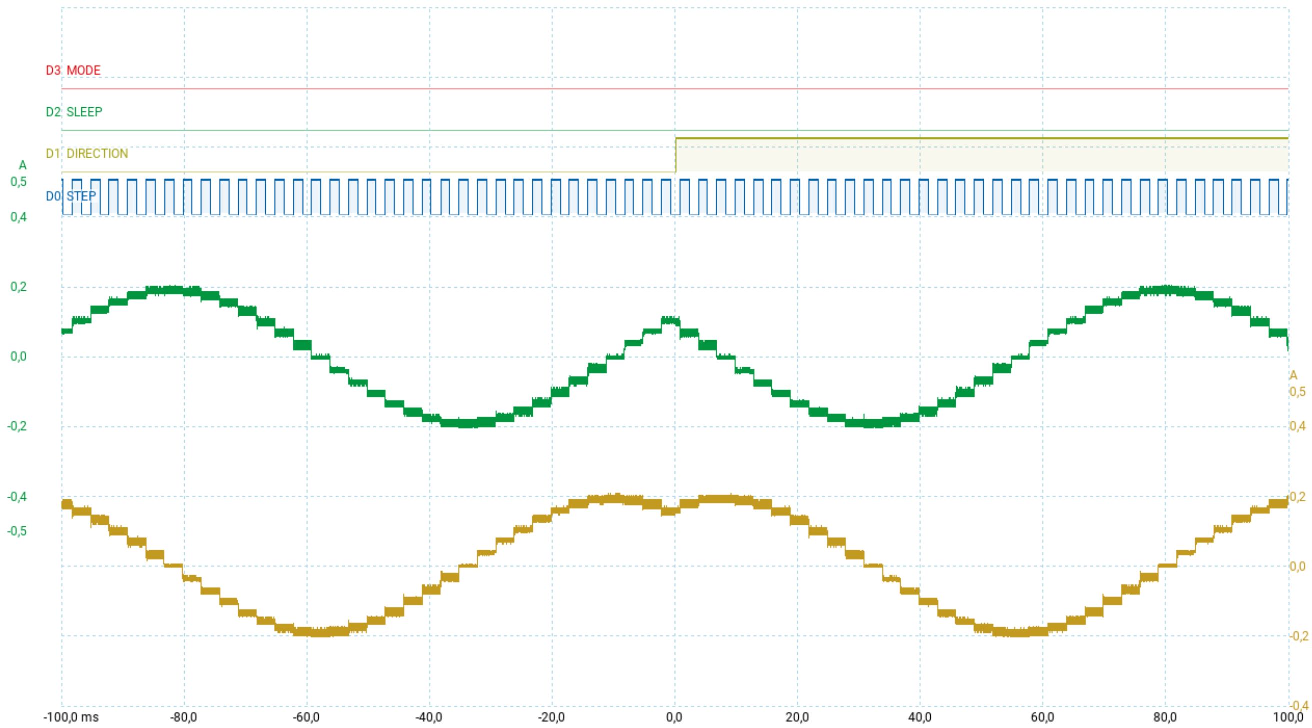

Figure 18. Microstep (1/8) Direction Change

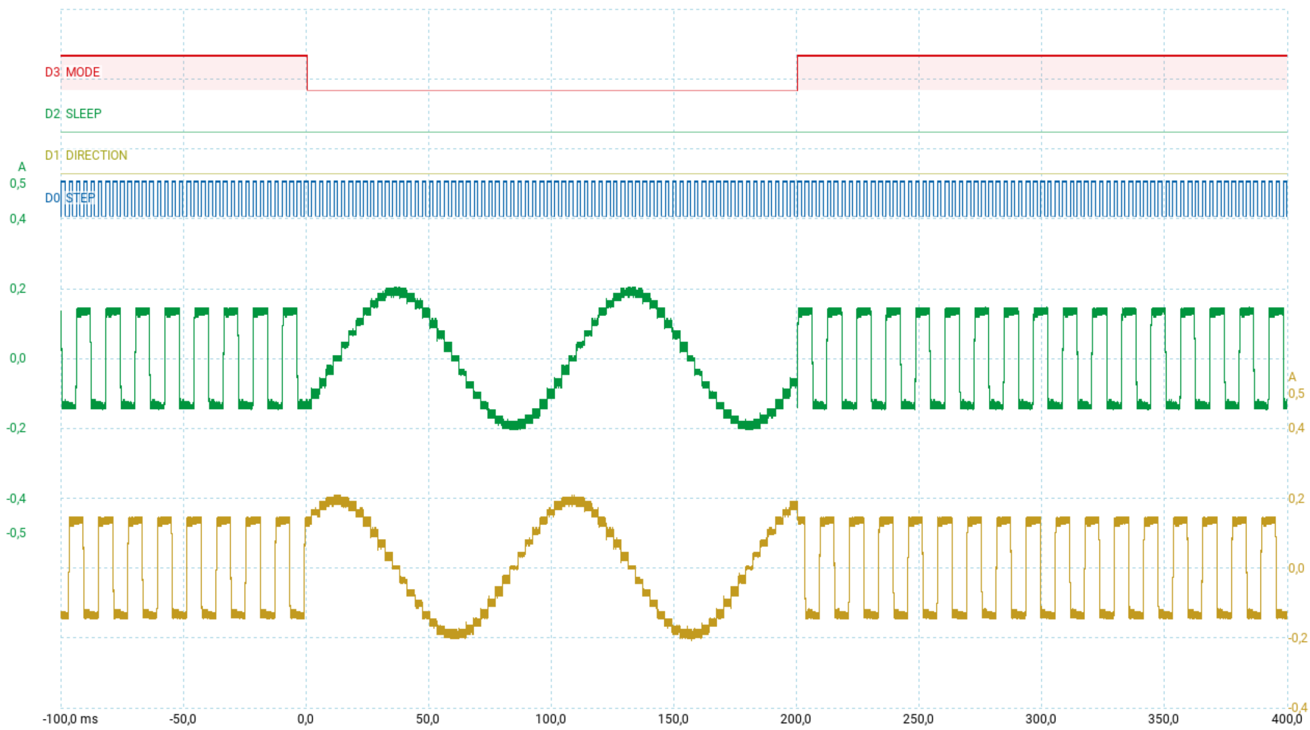

Figure 19. Microstep (1/8) and Full Step Switch

4.4 Microstep 1/16 GreenPAK Design

4.4.1. Description

To create a 1/16 microstep mode, the configuration of the microstep clock, PWM macrocells with keep logic, RegFile, and decay logic must be changed. The GreenPAK design for the 1/16 microstep is shown in Figure 20.

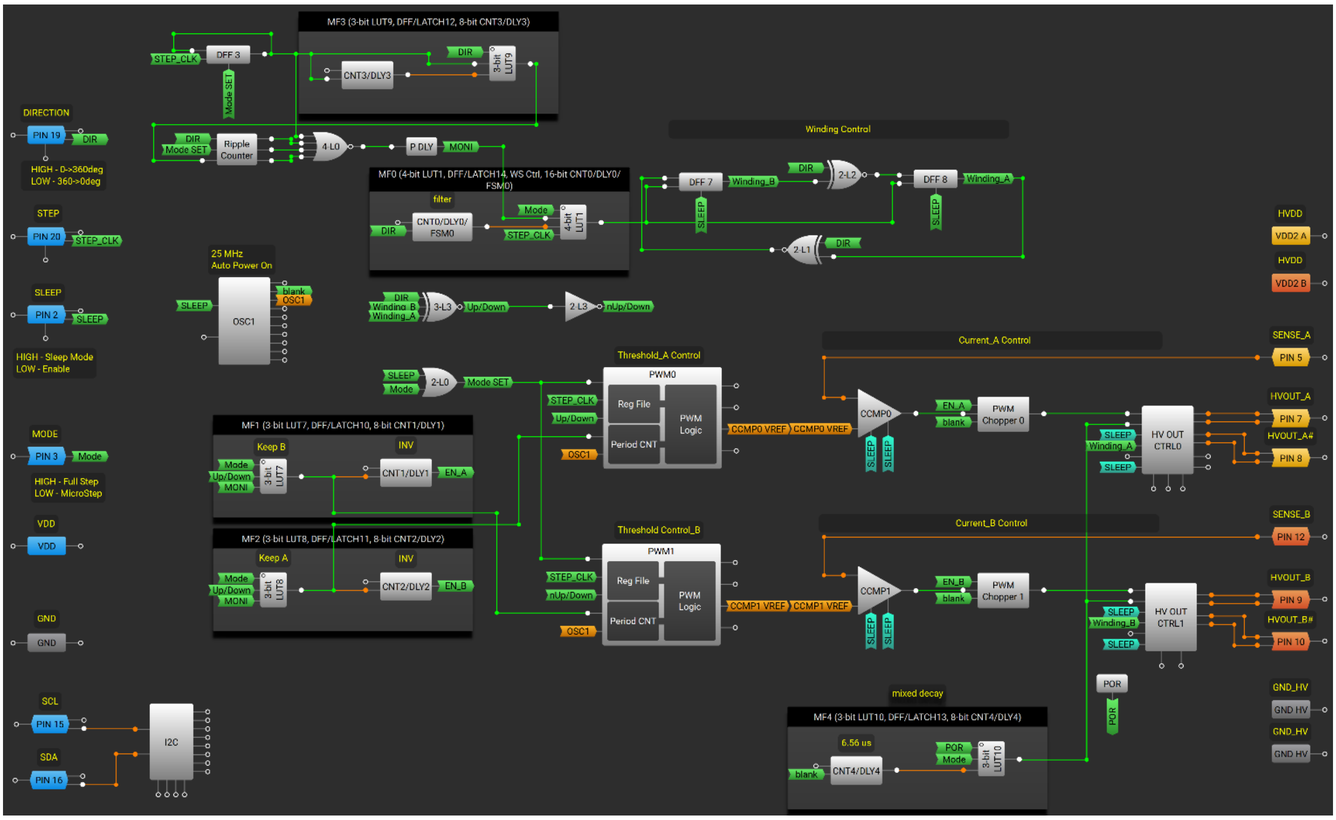

Figure 20. Stepper Motor Driver (Microstep – 1/16) GreenPAK Design

Figure 21 shows the timing diagram of the stepper motor driver operation in the 1/16 microstep mode.

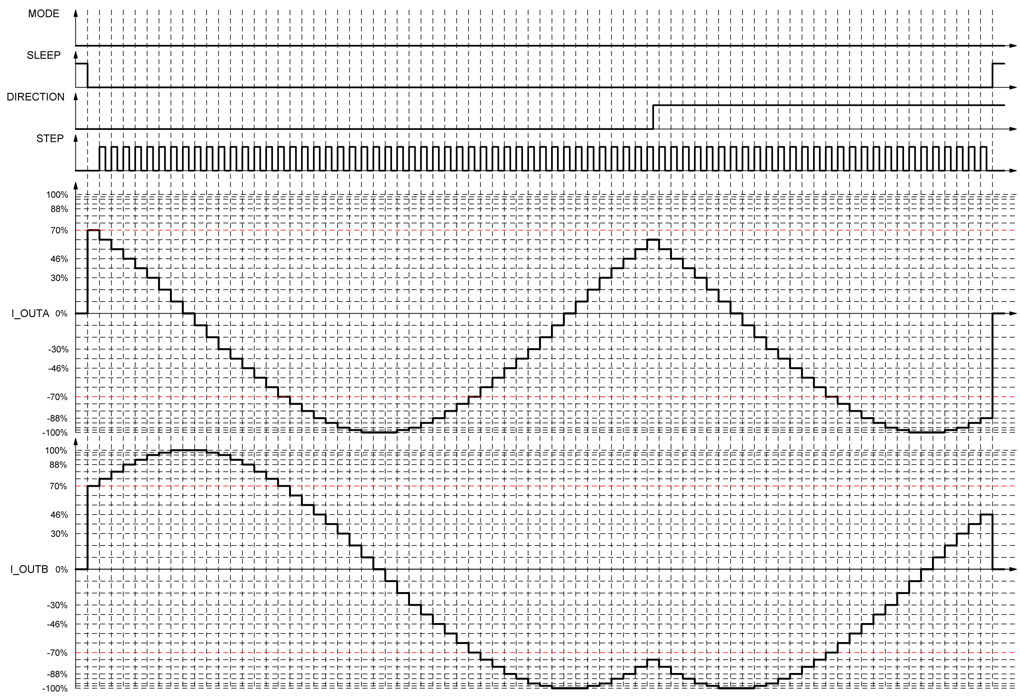

Figure 21. Microstep of 1/16 Timing Diagram

To the Ripple Counter, which divides the STEP_CLK frequency by 8 in the 1/8 microstep, the MF3 and DFF3 construction is added to create a divider by 16 with a possibility to change direction. This block with the 4-bit LUT0 and filter on the P DLY is a switching signal MONI for the Winding Control block. Thus, in the full step mode, the sequence will change each rising edge on the STEP input (PIN 20). In the microstep mode, it will change every sixteen clocks. The logic selection is provided by 4-bit LUT1.

The RegFile is now filled with CCMP Vref values for 1/16 microstep mode. It requires all 16 bits. Thus, both PWM0 and PWM1 use all 16 bytes. The initial byte for both PWMs is 8, and it corresponds to 71% current – home position. The same Up/Down signal cannot be used for both PWMs anymore, because if the current in one winding increases, then in the other it decreases, and vice versa. The 2-bit LUT3 is configured as an inverter and outputs the nUp/Down signal for the PWM1. The KEEP input for the PWM0 is now taken from the 3-bit LUT7, and for the PWM1 from the 3-bit LUT8.

Blank signal for the PWM Choppers is taken from the flexible divider of the OSC1. It is also used for the mixed decay creation on the CNT4/DLY4. Due to a lack of internal resources, the mixed decay is used for the whole microstep mode – sine up and down. In the full step mode, the slow decay is used.

4.4.2. Test Results

Figure 22-Figure 24 show the 1/16 microstep operation.

D3 (red/top line) – MODE (PIN 3)

D2 (green/2nd line) – SLEEP (PIN 2)

D1 (yellow/3rd line) – DIRECTION (PIN 19)

D0 (blue/4th line) – STEP (PIN 20)

Ch1 (green/5th line) – current through HV GPO0 (PIN 7), in Amperes

Ch2 (yellow/6th line) – current through HV GPO2 (PIN 9), in Amperes

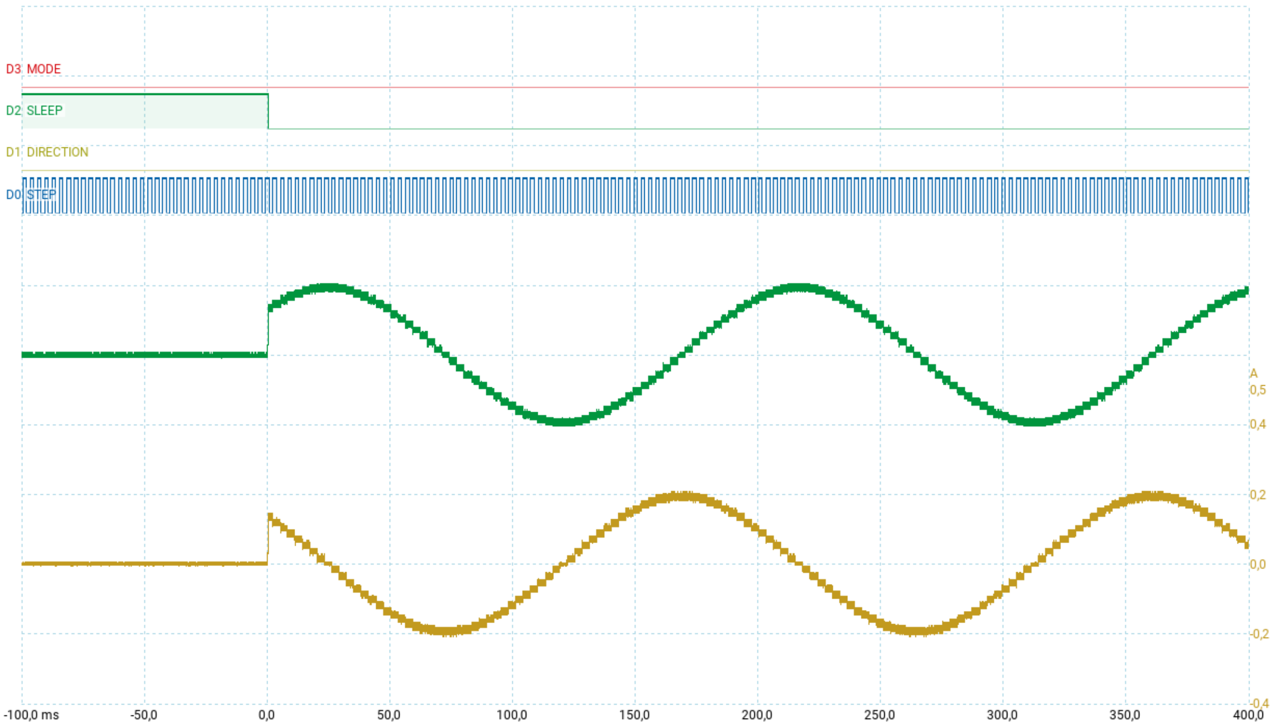

Figure 22. Microstep (1/16) Start, DIRECTION = 0

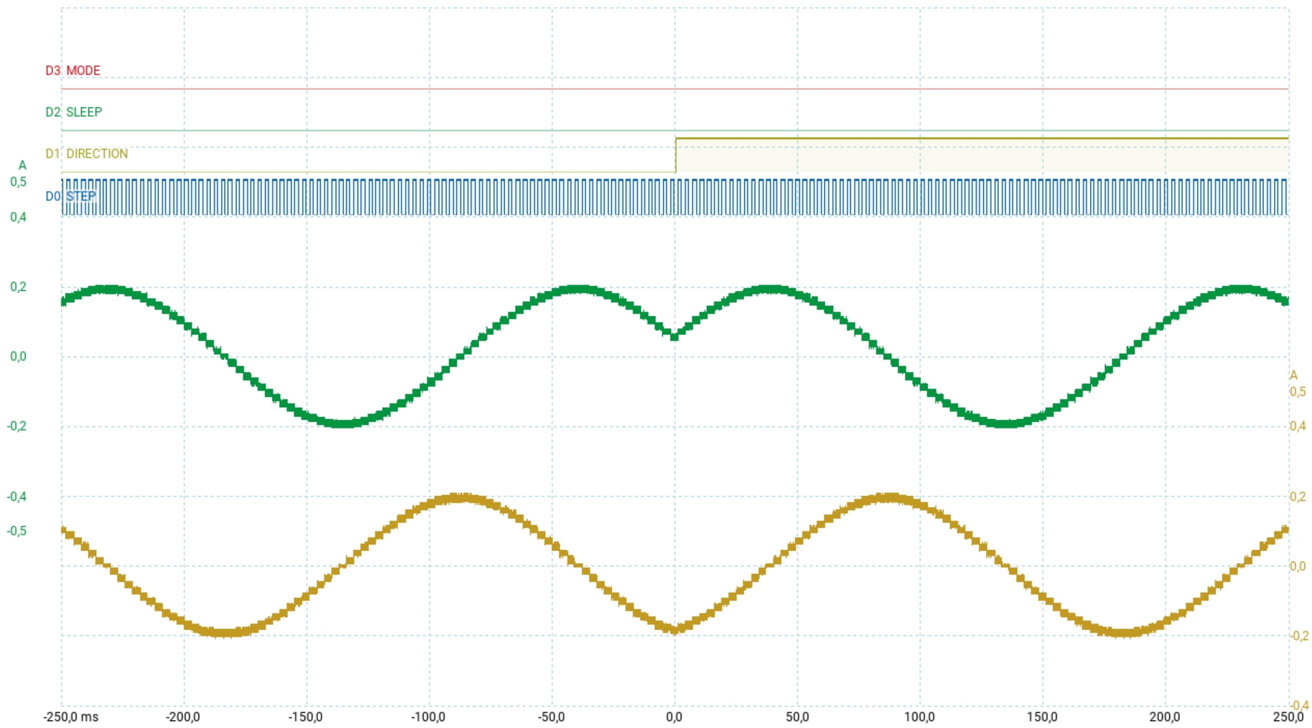

Figure 23. Microstep (1/16) Direction Change

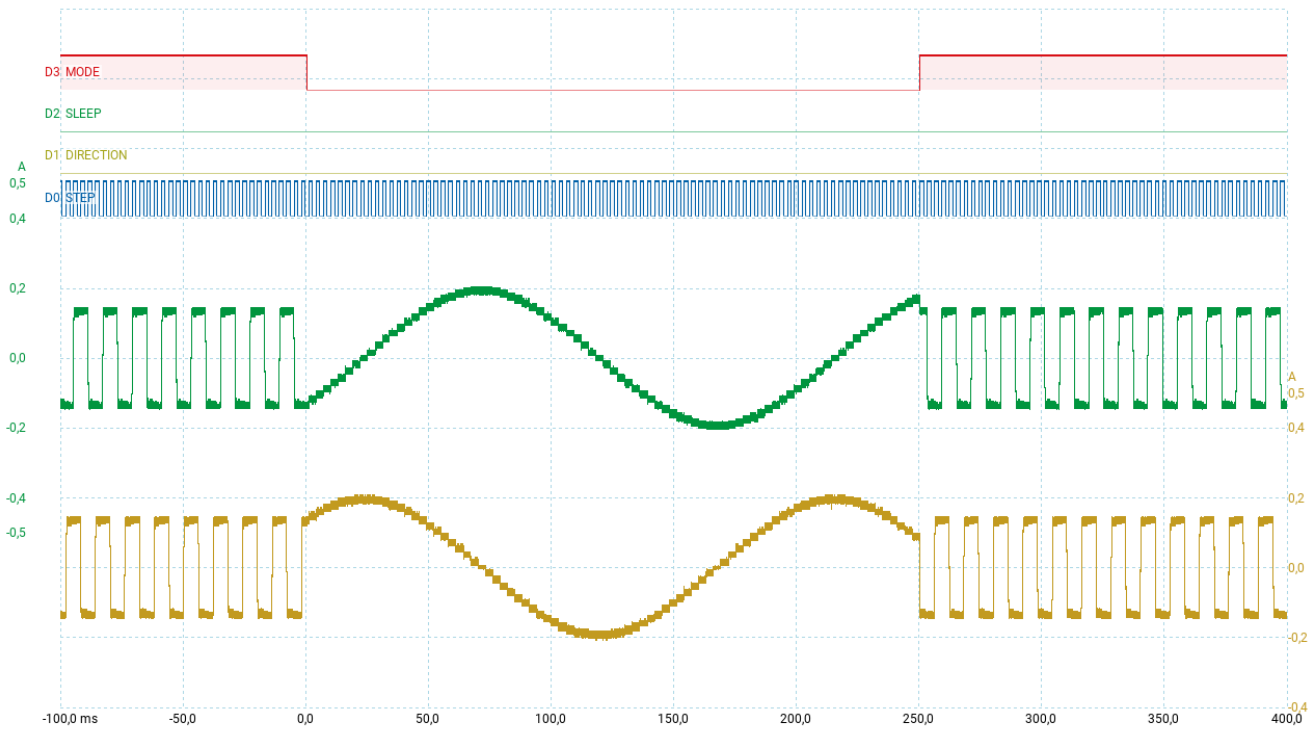

Figure 24. Microstep (1/16) and Full Step Switch

5. Conclusion

This application note presents a design of a bipolar stepper motor driver with current control implemented on a single HVPAK. The driver supports both full step and microstep operation, offering selectable resolutions of 1/2, 1/4, 1/8, and 1/16 steps, along with direction control capability. The design applies a slow decay mode for full step operation and a mixed decay mode for microstep, ensuring efficient performance and stable motor operation across different modes.

The flexibility of the internal resources allows adapting it to the needs of the customer without effort.

6. Revision History

Revision	Date	Description
1.11	Oct 20, 2025	Design updated Added microsteps of 1/2, 1/4, and 1/8 Renesas rebranding
1.10	Aug 14, 2020	Changed PWM frequency from 164kHz to 125kHz Changed blanking time from 1.2us to 0.8us Added slow decay mode for sine rising and slow decay for sine falling Fixed number of steps in microstep mode from 15 to 16
1.00	Mar 24, 2020	Initial release