

AnalogPAK Adjustable Analog Filter

SLG47001

This application note illustrates how to use the SLG47001/03 and SLG47004 to implement an adjustable analog filter and describes different ways to adjust the filter's cutoff frequency. The two on-chip Digital Rheostats tune the cutoff frequency, and one of the on-chip operational amplifiers is used as the active element.

The application note comes complete with design files which can be found in the Reference section.

Contents

1. Terms and Definitions	2
2. References	2
3. Introduction.....	3
4. System Overview	3
5. Functional Block Architecture	5
5.1 Setting Rheostat Data.....	6
5.2 Changing Rheostat Data	6
5.2.1 Changing Rheostat Value via I ² C.....	6
5.2.2 Changing Rheostat Value via Internal Logic	7
5.3 Software Simulation.....	9
5.4 Hardware Testing	10
6. Conclusion	11
7. Revision History	12

Figures

Figure 1. Analog Interface with One Tunable Filter	3
Figure 2. Sallen-Key Filter Based on the SLG47001/03	3
Figure 3. Sallen-Key Filter Based on the SLG47004	4
Figure 4. GreenPAK Designer Project.....	5
Figure 5. Digital Rheostat Properties.....	6
Figure 6. I ² C Connection to Change Rheostats Resistance	6
Figure 7. Internal Logic Block Diagram to Change Rheostats Resistance	7
Figure 8. Internal Logic for Changing Rheostat Resistance	7
Figure 9. Rheostat Reloading Unit.....	8
Figure 10. Software Simulation of Internal Logic	8
Figure 11. Hardware Testing Waveforms for Internal Logic	9
Figure 12. Simulated Frequency Response of a Filter Built on SLG47001/03 for Two Cutoff Frequencies.....	9
Figure 13. Simulated Frequency Response of a Filter Built on SLG47004 for Two Cutoff Frequencies.....	10
Figure 14. Frequency Response of Prototype Filter Built on SLG47001 for Two Cutoff Frequencies	10
Figure 15. Frequency Response of Prototype Filter Built on SLG47004 for Two Cutoff Frequencies	11

Tables

Table 1. Butterworth Filter Component Values - Resistance Set by Digital Rheostat, Capacitance Fixed for each Device	5
--	---

1. Terms and Definitions

ADC	Analog-to-digital converter
CNT	Counter
DFF	D flip-flop
LUT	Look-up table
OpAmp	Operational amplifier

2. References

For related documents and software, please visit:

[AnalogPAK | Renesas](#)

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the AnalogPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC. We also recommend that you familiarize yourself with the full capabilities of the AnalogPak SLG47001/03 [5] and SLG47004 [6].

[1] [GreenPAK Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics

[2] [AN-CM-310 GreenPAK™ Adjustable Analog Filter.aap](#), AnalogPAK Design File, Renesas Electronics

[3] [AnalogPAK Development Tools](#), AnalogPAK Development Tools Webpage, Renesas Electronics

[4] [GreenPAK Application Notes](#), GreenPAK Application Notes Webpage, Renesas Electronics

[5] [SLG47001/03 Datasheet](#), Renesas Electronics

[6] [SLG47004 Datasheet](#), Renesas Electronics

3. Introduction

This application note describes an adjustable analog filter implemented using the SLG47001/03 and SLG47004 AnalogPAK devices. The design developed for the SLG47001 is fully compatible with the SLG47003. Separate implementations are provided for the SLG47001/03 and SLG47004 to account for differences in their internal architectures. In both implementations, the filter cutoff frequency is adjusted using the configurable analog resources available in the corresponding device, while an integrated operational amplifier is used as the active filter element. This application note also discusses several methods for adjusting the cutoff frequency. Complete design files for both device implementations are provided in the Reference section.

In many applications, signals from multiple sources, such as sensors, are acquired using a single analog-to-digital converter (ADC). Such systems typically require an analog multiplexer and a separate analog filter for each channel because each signal source may have different filtering requirements, including a different cutoff frequency. A more space- and cost-efficient alternative is to share a single tunable analog filter among all channels, as illustrated in Figure 1. The configurable analog resources of the SLG47001/03 and SLG47004 enable this architecture to be implemented as a compact, flexible, and power-efficient solution.

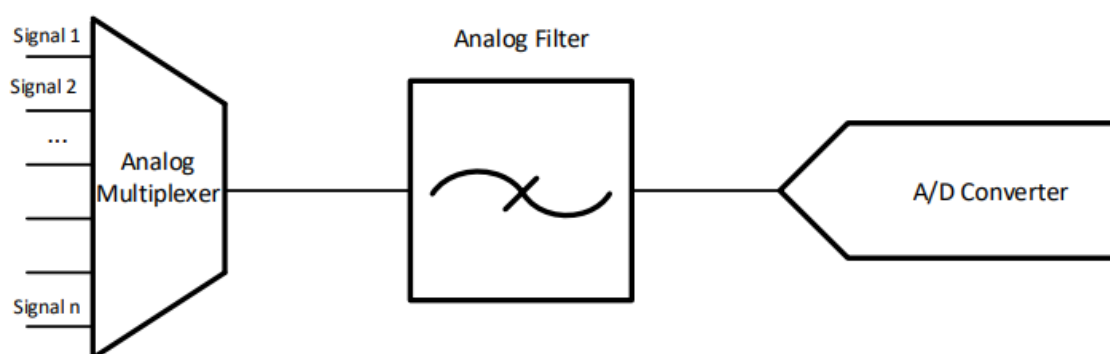


Figure 1. Analog Interface with One Tunable Filter

4. System Overview

This application note demonstrates the implementation of an adjustable analog filter using, as an example, a second-order, programmable, active low-pass Sallen-Key filter (Figure 2, Figure 3).

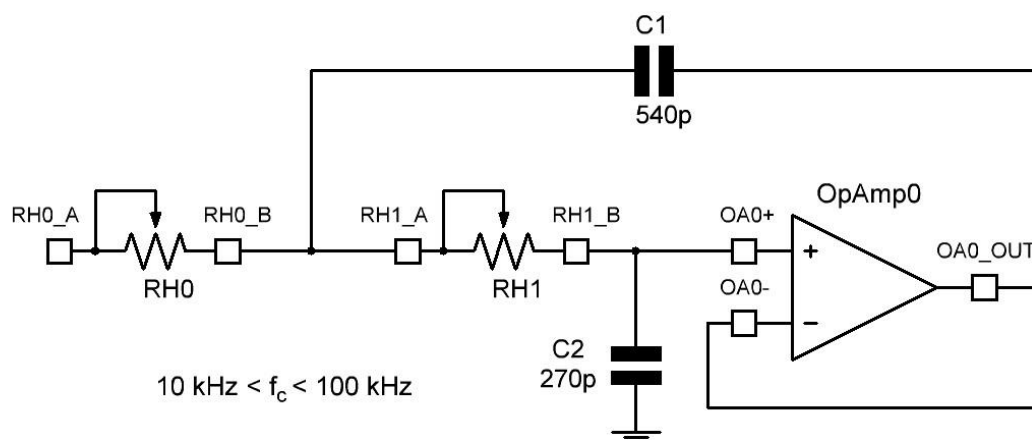


Figure 2. Sallen-Key Filter Based on the SLG47001/03

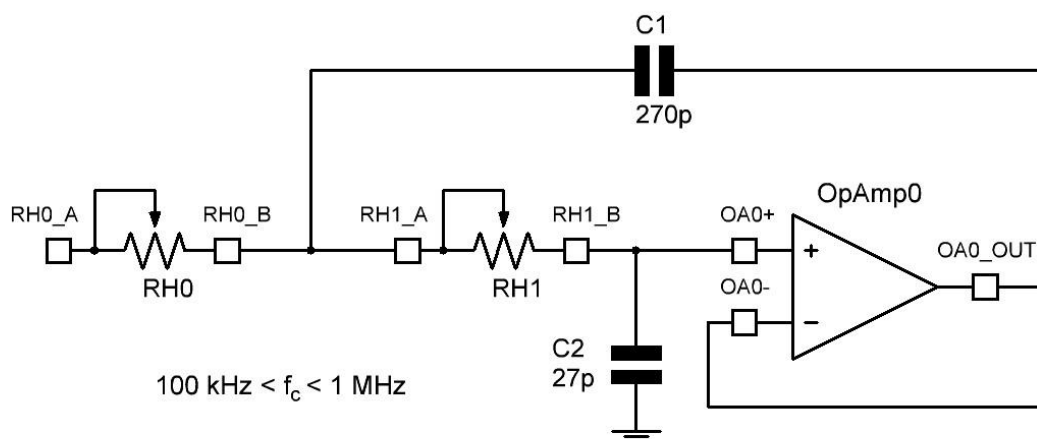


Figure 3. Sallen-Key Filter Based on the SLG47004

The filter is built from two resistors, two capacitors, and an operational amplifier. The two resistors are replaced with the SLG47001/03/04 Digital Rheostats, and one of the SLG47001/03/04 operational amplifiers is used as the active element.

By adjusting the two Digital Rheostats, both the cutoff frequency and the approximation method of this active filter can be changed. The Butterworth approximation is used in this application note. The frequency behavior of a Butterworth filter is maximally flat in the magnitude response across the passband. Its attenuation rate in the transition band is better than that of a Bessel filter, although not as steep as a Chebyshev filter. There is no ringing in the stopband, and although the step response shows some overshoot and ringing in the time domain, both are smaller than for a comparable Chebyshev filter.

The transfer function of the low-pass configuration in Figure 2 is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{K/(RH_0 RH_1 C_1 C_2)}{s^2 + s(1/RH_0 C_1 + 1/RH_1 C_1 + 1/RH_1 C_2 - K/RH_1 C_2) + 1/(RH_0 RH_1 C_1 C_2)}$$

where $K = 1$;

For this topology the cutoff frequency is:

$$f_c = \frac{1}{2\pi\sqrt{RH_0 RH_1 C_1 C_2}}$$

These expressions can be used to calculate the appropriate resistance and capacitance values.

The capacitor values are kept constant while the resistive elements are adjusted. Since the operational amplifiers in the SLG47004 and the SLG47001/03 are different, different cutoff frequencies were selected for each device: 100 kHz and 1 MHz for the SLG47004, and 10 kHz and 100 kHz for the SLG47001/03. This choice is driven by the difference in amplifier bandwidth, i.e., Gain Bandwidth Product (GBP). The resistor and capacitor values for both filters are given in Table 1.

It should also be noted that, due to the difference in slew rate between the two devices, the frequency response measurements were taken using different input sine-wave amplitudes from the signal generator: 100 mV for the SLG47001/03 and 500 mV for the SLG47004.

The SLG47001/03 and SLG47004 contain two 10-bit digital rheostats. The full-scale resistance of each rheostat is 100 kΩ, and the digital code that sets the resistance ranges from 0 to 1023 (1024 taps). Code 0 corresponds to the minimum resistance between the RHx_A and RHx_B terminals; as the code increases, the resistance

increases monotonically, and as the code decreases, the resistance decreases. The voltage on any rheostat pin may lie between AGND and VDDA and can be changed dynamically during operation.

The values calculated for this filter design are summarized in Table 1, together with the closest achievable Digital Rheostat values for RH0 and RH1 and their corresponding digital codes.

Table 1. Butterworth Filter Component Values - Resistance Set by Digital Rheostat, Capacitance Fixed for each Device

P/N	Cutoff Frequency, kHz	Calculated RH0 Value, Ω	Closest Digital Rheostat RH0 Value, Ω	Digital Rheostat RH0 Code	Calculated RH1 Value, Ω	Closest Digital Rheostat RH1 Value, Ω	Digital Rheostat RH1 Code	C ₁ , pF	C ₂ , pF
SLG47001/03	10	41680	41679	420	41680	41679	420	540	270
	100	4170	4167	42	4170	4167	42		
SLG47004	100	4400	4395	44	78900	78906	807	270	27
	1000	440	490	4	7890	7910	80		

5. Functional Block Architecture

Figure 4 shows the internal design of the project in GreenPAK Designer software.

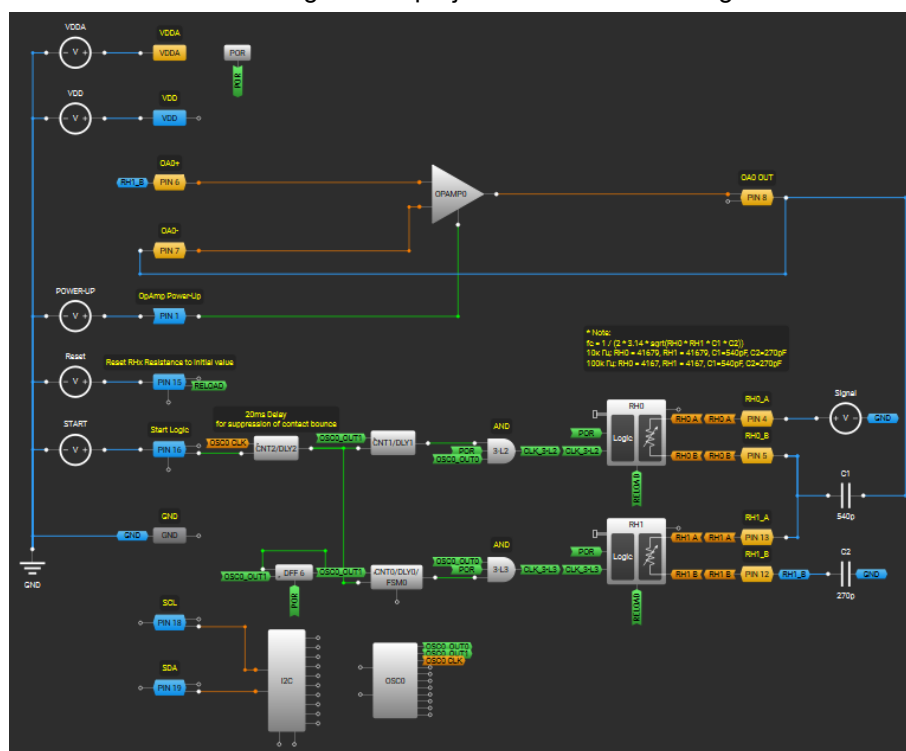


Figure 4. GreenPAK Designer Project

5.1 Setting Rheostat Data

Both rheostats allow the “Resistance (Initial data)” field to be set in their properties, which directly sets the desired cutoff frequency of the filter (Figure 5).

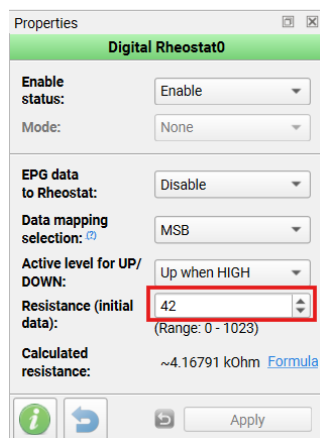


Figure 5. Digital Rheostat Properties

5.2 Changing Rheostat Data

There are two ways to change the Digital Rheostat values: over I²C, and through internal logic.

5.2.1 Changing Rheostat Value via I²C

Both the SLG47001/03 and the SLG47004 contain an I²C macrocell that can read and write the Digital Rheostat data (Figure 6). However, since the two devices have different register maps, the corresponding I²C addresses differ between them.

For the SLG47004, the rheostat resistance is set through registers [0xC0, 0xC1] for RH0 and [0xD0, 0xD1] for RH1. The current rheostat values can be read back from registers [0xC2, 0xC3] for RH0 and [0xD2, 0xD3] for RH1.

For the SLG47001/03, the rheostat resistance is set through registers [0x91, 0x92] for RH0 and [0x93, 0x94] for RH1. The current rheostat values can be read back from registers [0x9A, 0x9B] for RH0 and [0x9C, 0x9D] for RH1.

In both devices, the I²C master can write to the corresponding set registers to adjust the cutoff frequency of the filter according to the digital codes given in Table 1.

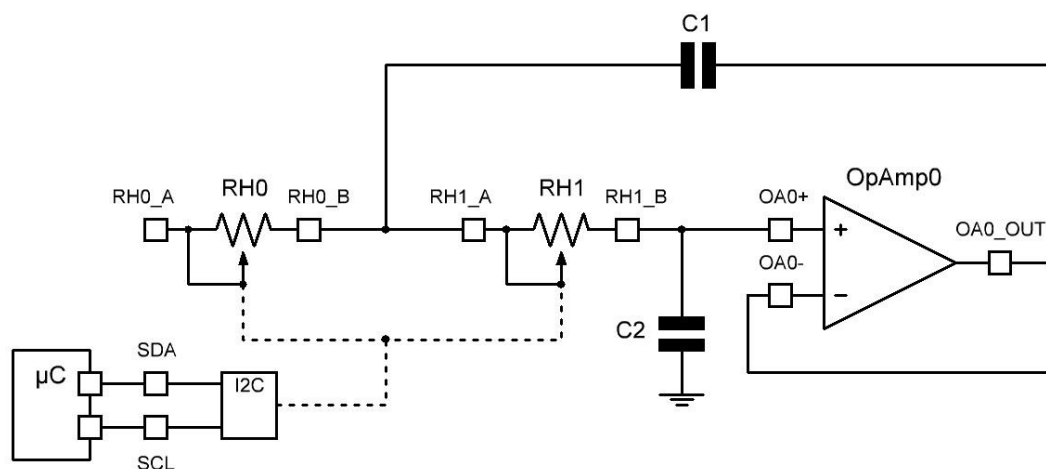


Figure 6. I²C Connection to Change Rheostats Resistance

5.2.2 Changing Rheostat Value via Internal Logic

Adjusting the cutoff frequency over I²C is simple and convenient, but it requires an I²C master. An alternative method uses two pins and internal logic (Figure 7).

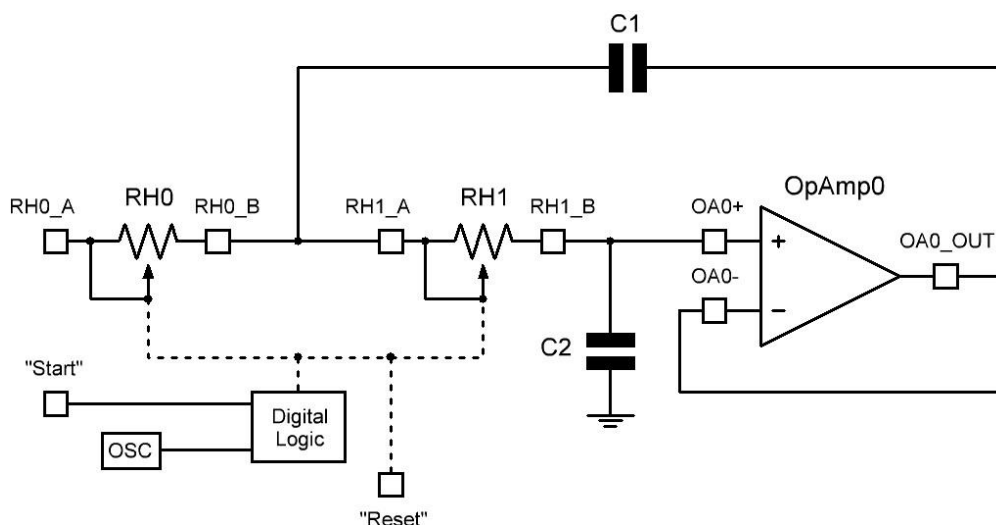


Figure 7. Internal Logic Block Diagram to Change Rheostats Resistance

A High level on the Start (Pin 16) and Reset (Pin 15) pins switches the filter between two different cutoff frequencies. With the rheostat initial values set for a 100 kHz cutoff, a High level on Pin 16 changes the cutoff to 10 kHz (Figure 8). A High level on Pin 15 resets the cutoff back to 100 kHz (Figure 9).

To detail this behavior: for the 100 kHz cutoff, RH0 = 4.167 k Ω (code 42) and RH1 = 4.167 k Ω (code 42). To change the cutoff to 10 kHz, RH0 = 41679 Ω (code 420) and RH1 = 41679 Ω (code 420). Therefore, the digital code RH0 and RH1 must be increased by 378. To increase the resistance, the rheostat setting “Active level for UP/DOWN” must be set to “Up when High”.

The 8-bit counters can be configured to provide the required number of clock pulses from the oscillator to the rheostats. The 8-bit CNT1/DLY1 data must be set to 187, and the 8-bit CNT0/DLY0 data to 187.

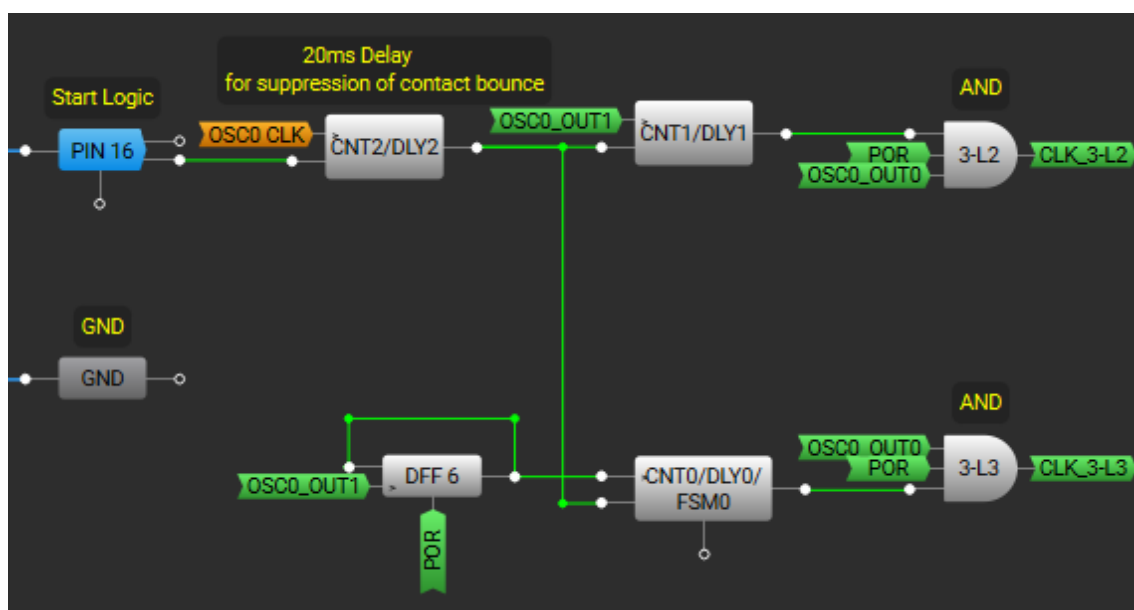


Figure 8. Internal Logic for Changing Rheostat Resistance

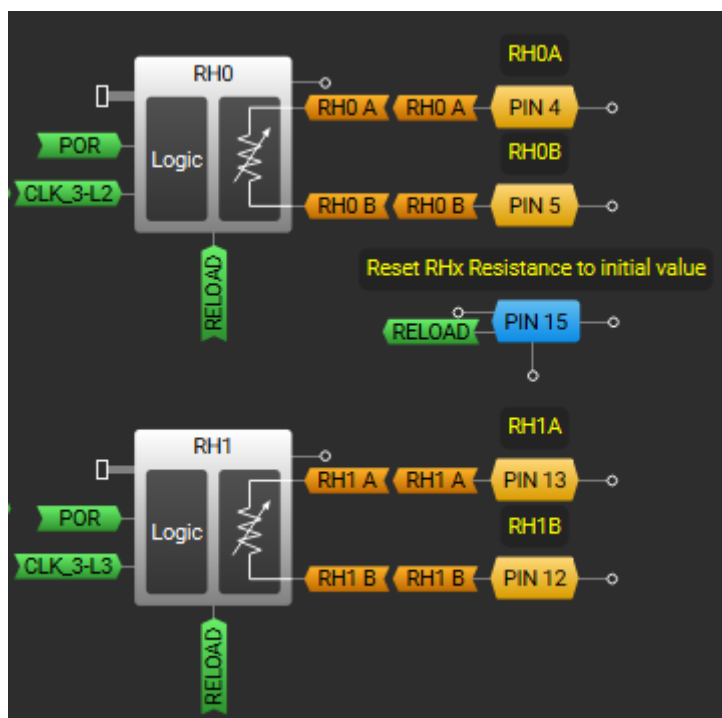


Figure 9. Rheostat Reloading Unit

The counters are stopped by the internal logic (Figure 8). Both CNT1/DLY1 and CNT0/DLY0 are configured as One-Shot blocks. When the "Start Logic" signal goes High, each counter triggers on the rising edge and drives its output High — CNT1/DLY1 to input IN2 of 3-bit LUT2, and CNT0/DLY0 to input IN0 of 3-bit LUT3. The remaining inputs of 3-bit LUT2 and 3-bit LUT3 receive the POR signal and the 2.048 kHz output of Oscillator 0. Both LUTs are configured as a logical AND, so each one passes the 2.048 kHz clock to its rheostat only while the corresponding one-shot output and POR are High. The output of 3-bit LUT2 drives the CLK input of Digital Rheostat RH0, and the output of 3-bit LUT3 drives the CLK input of Digital Rheostat RH1.

Software simulation results for this internal logic are shown in Figure 10, and hardware testing results in **Error! Reference source not found.**

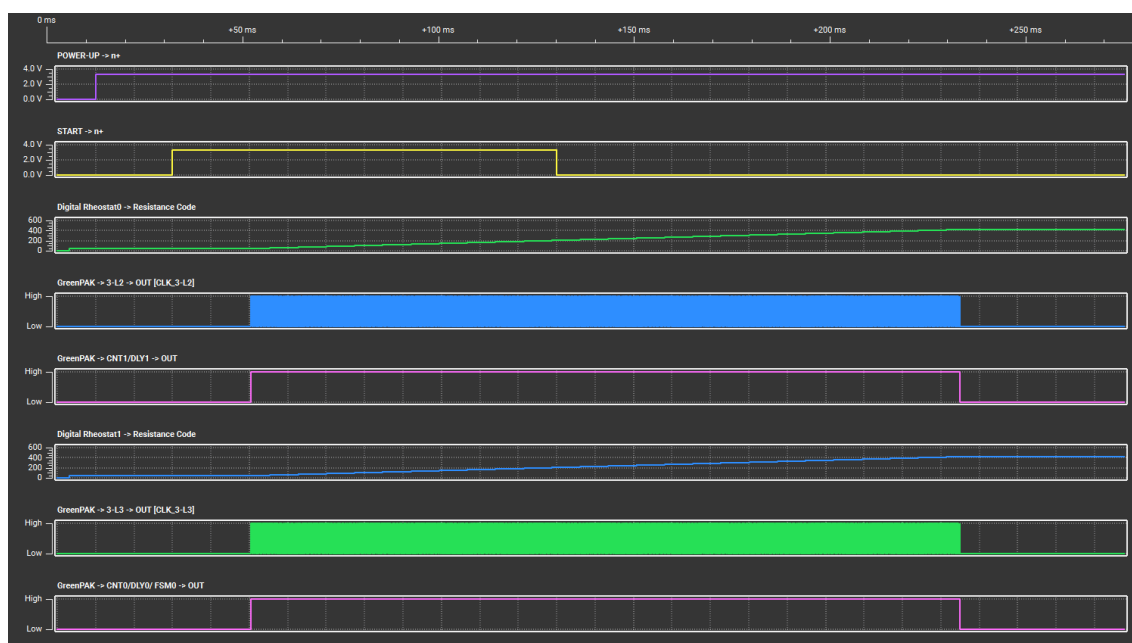


Figure 10. Software Simulation of Internal Logic



Figure 11. Hardware Testing Waveforms for Internal Logic

For resetting the cutoff frequency, Pin 15 works as a Digital Input connected to the “Reload” input of the rheostats. When the Reload signal goes High, the rheostat value is reset to the initially set Resistance (initial data).

5.3 Software Simulation

Figure 12 shows the frequency response of the second-order active Sallen–Key low-pass filter for cutoff frequencies of 10 kHz and 100 kHz, whereas Figure 13 shows the response for cutoff frequencies of 100 kHz and 1 MHz.



Figure 12. Simulated Frequency Response of a Filter Built on SLG47001/03 for Two Cutoff Frequencies

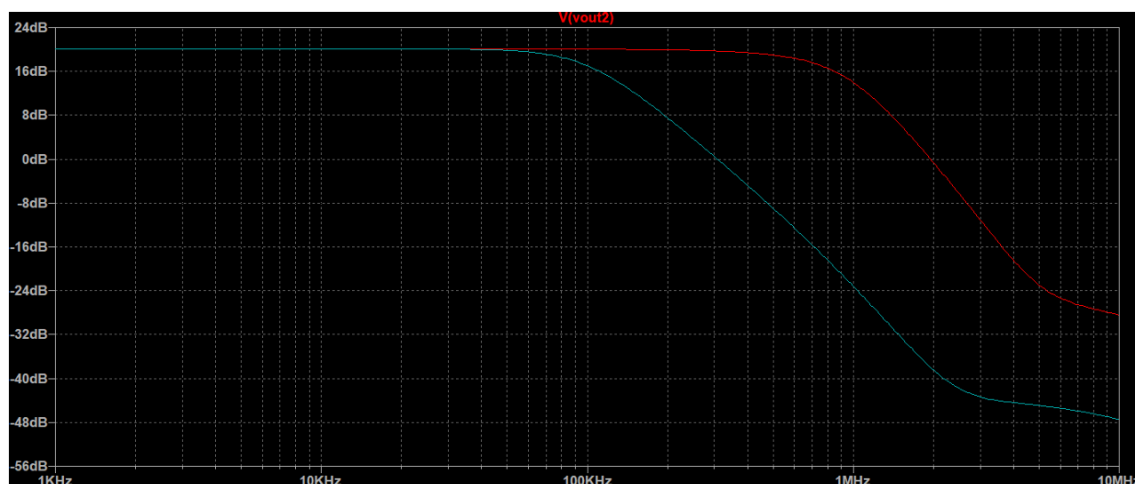


Figure 13. Simulated Frequency Response of a Filter Built on SLG47004 for Two Cutoff Frequencies

5.4 Hardware Testing

The test results of the prototypes implemented using the SLG47001 and SLG47004 ICs for both cutoff frequencies are shown in Figure 14 and Figure 15, respectively.

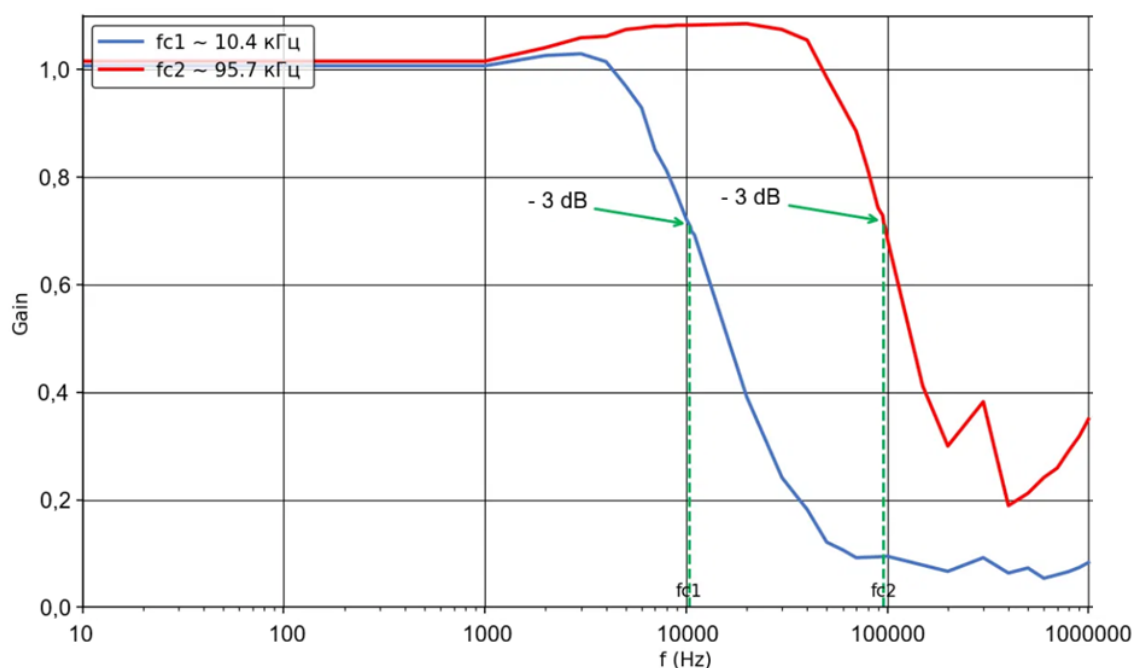


Figure 14. Frequency Response of Prototype Filter Built on SLG47001 for Two Cutoff Frequencies

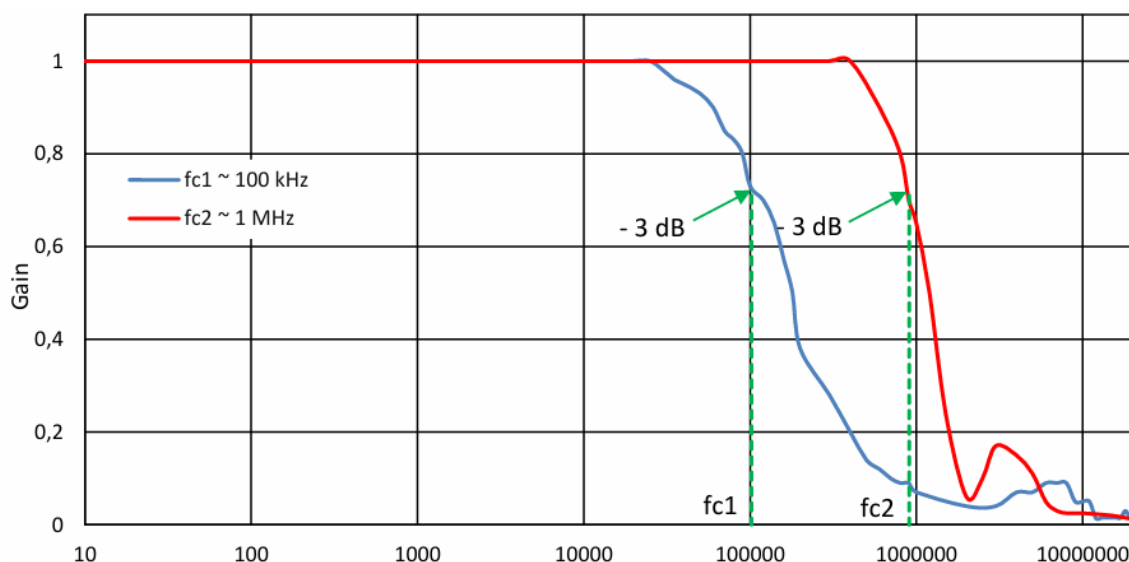


Figure 15. Frequency Response of Prototype Filter Built on SLG47004 for Two Cutoff Frequencies

6. Conclusion

The SLG47001/03 and SLG47004 provide the internal resources required to implement advanced analog functions. This application note demonstrates how these configurable mixed-signal ICs can be used to implement an adjustable analog filter as a functional replacement for several standard products. Using a single tunable analog filter to support different cutoff frequencies provides a more flexible and cost-effective solution while reducing PCB footprint and power consumption. The configurable architecture of these devices also allows this approach to be readily extended to adjust other filter characteristics, such as the filter approximation.

7. Revision History

Revision	Date	Description
2.00	Jun 22, 2026	Changed the base part number
1.00	Nov 18, 2020	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.