Application Note

DC Power Line Communication

AN-CM-318

Abstract

This application note presents a low cost, low power, capacitor-coupled, DC power-line communication system based on the GreenPAK SLG46108 device.

This application note comes complete with design files which can be found in the references section.

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Figures

1 Terms and Definitions

PLC	Power Line Communication
LUT	Look Up Table

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/configurable-mixed-signal.

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to modify the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-318 Power Line Communication.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG46108, Datasheet

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This article was originally published on Power Electronics News.

3 Introduction

This application note presents a method to use a DC power line for data communication while simultaneously providing power without interruption. This is accomplished via RLC coupling circuits together with GreenPAK IC's providing modulation (TX) and demodulation (RX).

4 TX/RX Operation

The communication signal on this power line is On-Off Key (OOK) modulated. GreenPAK IC's perform the OOK modulation / demodulation of UART digital signals using of 62kHz carriers generated from within the GreenPAK IC's. Figure 1 shows UART communication between side A and B. TXD_ and RXD_ are the digital UART signals as seen by the system MCU's at each end; PL_TX/RX are the signals coupled to/from the power line.

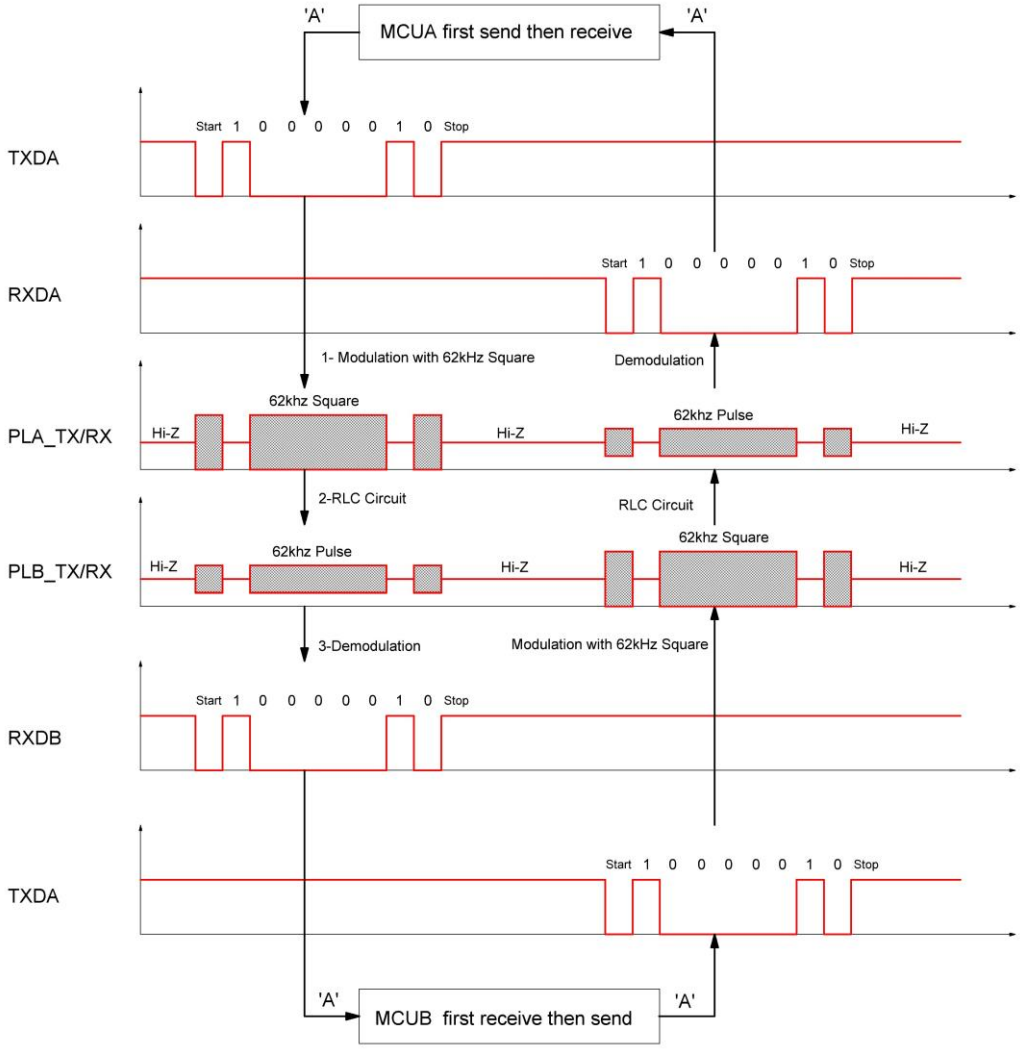

Figure 1: Operation Timing Diagram

5 Circuit Analysis

The RLC coupling circuit is shown in Figure 7. The analysis is of the circuit under non-ideal (rising edge equals 10ns) step signal. The s-domain model of the non-ideal step signal can be obtained by Laplace transform of the time domain expression.

$$v(t) = \frac{5}{t_r} * t * [u(t) - u(t - t_r)] + 5 * u(t - t_r) \xrightarrow{Laplace} V(s) = \frac{5}{t_r} * \frac{1}{s^2} * (1 - e^{-t_r s})$$

The s-domain model of the circuit obtained by replacing the circuit components with its s-domain model and simplify(a>b>c>d). This process is shown in Figure 2. R1 represents the output impedance of GPIO.

$$G(s) = \frac{\frac{2.2 * 10^{-6}s^2 + 10^7}{2s}}{\frac{4.7 * 10^3 s + 10^{12}}{47s} + \frac{2.2 * 10^{-6}s^2 + 10^7}{2s}} \approx \frac{s^2 + 4.7 * 10^{12}}{s^2 + 9.4 * 10^7 s + 2 * 10^{16}}$$

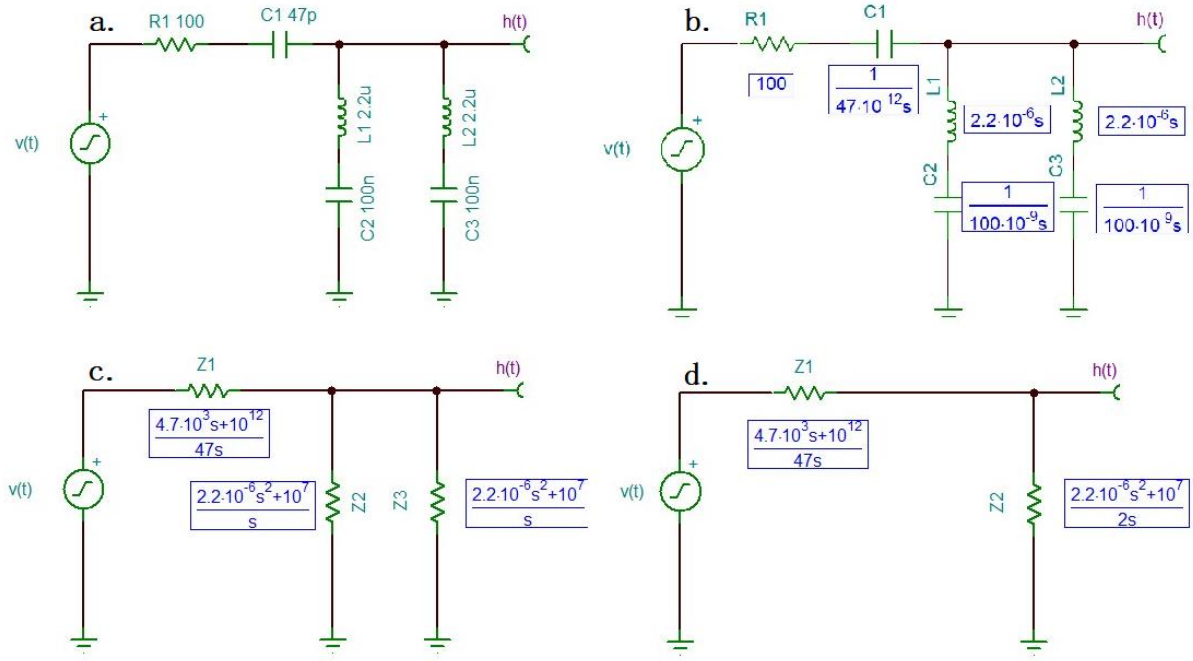

Figure 2: RLC Circuit Simplification in s-Domain

Multiply the mode of the circuit with the input signal to get the response function in s-domain:

$$H(s) = V(s) * G(s) = \frac{5}{10 * 10^{-9}} * \frac{1}{s^2} * \left(1 - e^{-10*10^{-9}s}\right) * \frac{s^2 + 4.7 * 10^{12}}{s^2 + 9.4 * 10^7 s + 2 * 10^{16}}$$

The response in time domain can be obtained by performing the inverse Laplace transform of the function:

$$h(t) = \begin{cases} 3.76 * e^{-4.7*10^7 t} \sin\left(1.33 * 10^8 t\right), & 0 \le t \le 10 * 10^{-9} \\ 6.3 * e^{-4.7*10^7 t} \sin\left(1.33 * 10^8 t + 68.3°\right), & t > 10 * 10^{-9} \end{cases}$$

The response curve is shown in Figure 3. The rising and falling edges of PL_TX are converted into pulses. Figure 4 summarizes the impact of the circuit. In order to prevent the PL_RX PIN from receiving a negative voltage, the pulse is DC biased to VDD/2 by the RC-R circuit.

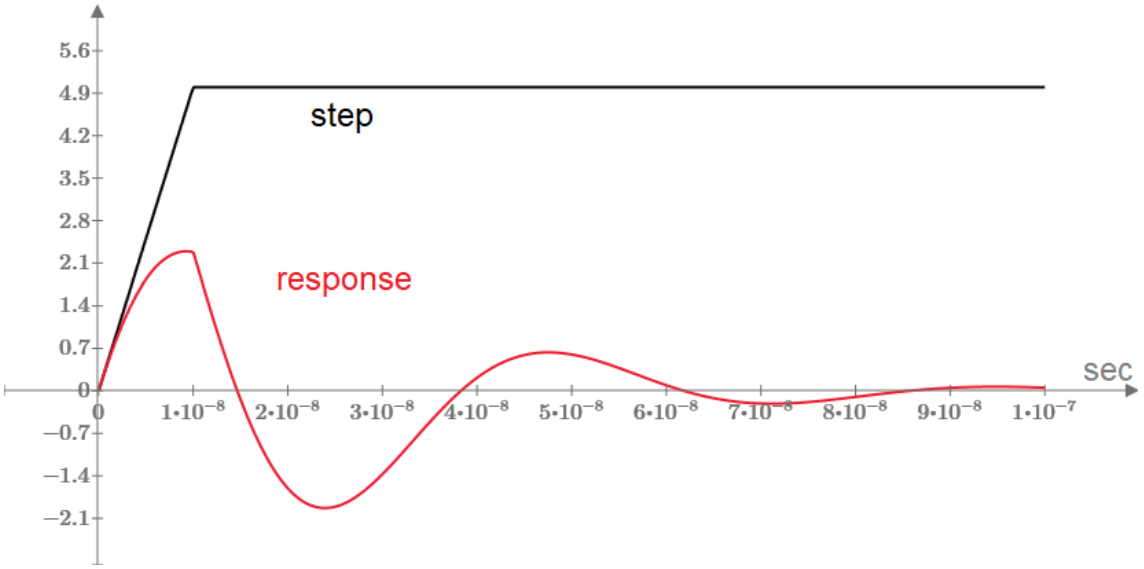

Figure 3: RLC Circuit Response

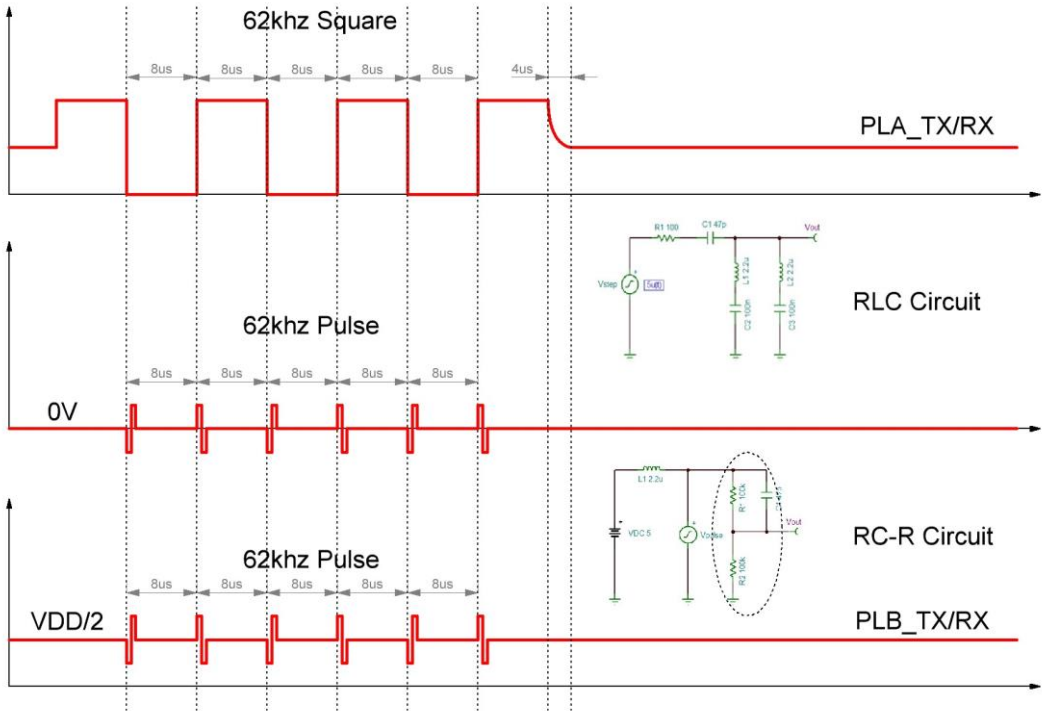

Figure 4: Circuit Timing Diagram

6 GreenPAK Design

The GreenPAK-SLG46108V developed in GreenPAK Designer is shown in Figure 5.

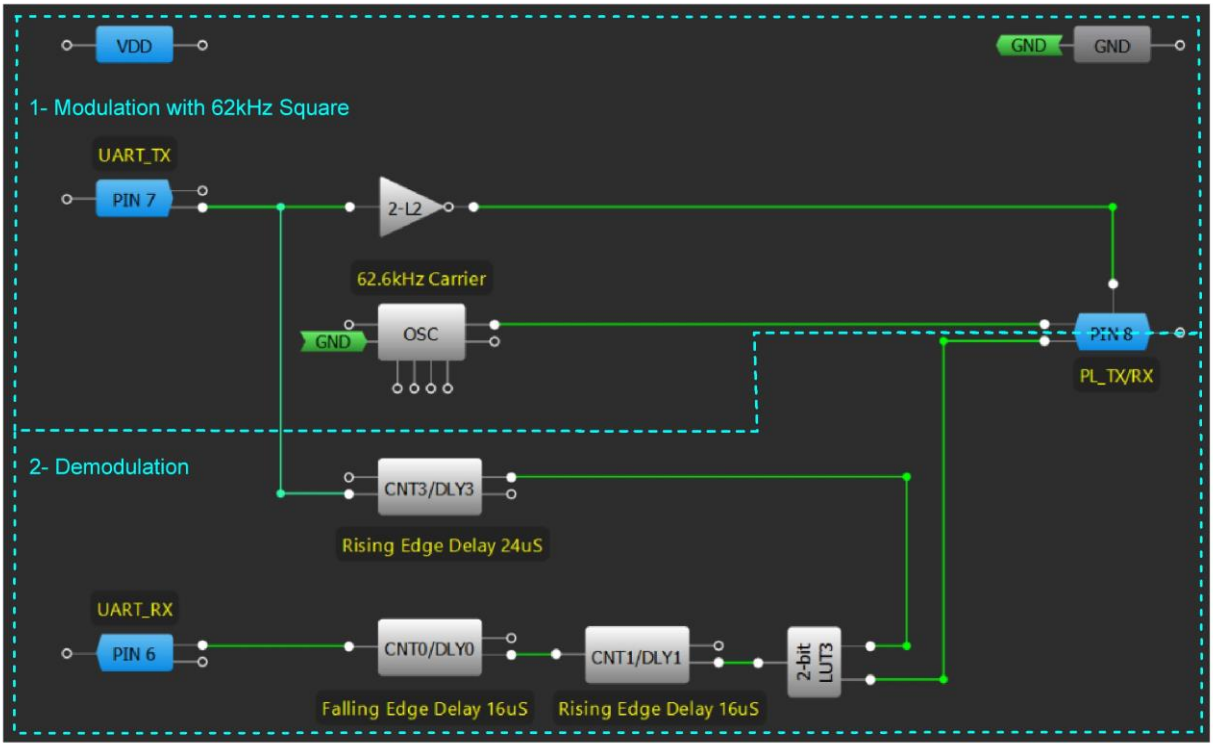

Figure 5: SLG46108 GreenPAK Design

6.1 Pin Configuration

The PIN7(UART_TX) is used to receive the serial port signal. After being modulated, it is sent to the power line through the PIN8 (PL_TX/RX). PIN7(UART_TX) is set as digital input without Schmitt trigger with pull up resistor.

The signal received from PL_TX/RX is demodulated and output to PIN6(UART_RX), PIN6 is set as digital output push-pull.

PIN8(PL_TX/RX) is configured as a digital input/output. When PIN7(UART_TX) is a low level, PL_TX/RX is in output mode, otherwise its input mode.

6.2 Modulation

This design is for a 9600bps baud-rate, so the carrier frequency needs to be greater than 48kHz. We configure OSC power mode to force power on, OSC frequency to 2Mhz/8, output0 second divider by 4 to get a 62.6kHz carrier.

As shown in Figure 1, when UART_TX is a low level, PL_TX/RX outputs the carrier. When UART_TX is a high level, PL_TX/RX is in a high-impedance input state.

6.3 Demodulation

After PL_TX/RX stops outputting the carrier and re-biased to VDD/2 by the RC-R circuit, we start to demodulate the signal input by PL_TX/RX. The time required to re-bias to VDD/2 can be measured by an Oscilloscope. We set DLY3 to rising edge delay 24us which is greater than the measured time, 2-bit LUT3 sets to high when DLY3 inputs low.

As shown in Figure 6, PL_TX/RX receives the signal from the power line and converts it into a digital pulse, then is demodulated by DLY1(rising edge delay 16us). In order to ensure that the low-level time after demodulation is equal to before modulation, delay the demodulated signal by DLY0(falling edge delay 16us).

Since the bias voltage of PL_TX/RX is VDD/2, when PL_TX/RX is in digital input mode, the device will consume approximately 70uA of extra current.

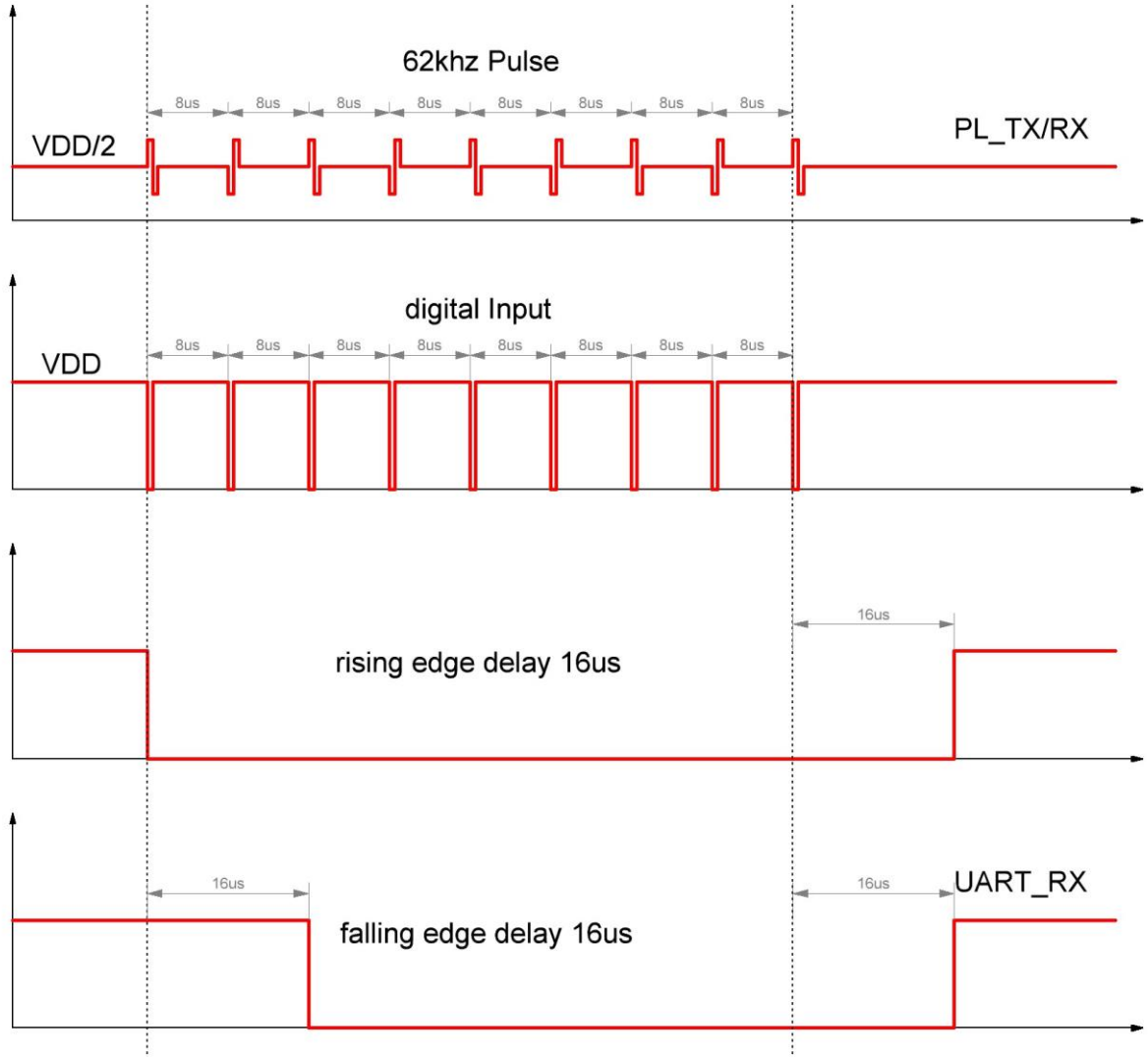

Figure 6: Demodulation

7 Application Schematic

Figure 7 depicts the schematic of the power line interface on a PCB with SLG46108 sockets. Figure 8 shows the picture of the PCB with its prototype. Two IC sockets will plug directly into the 2x10 female socket like Figure 9.

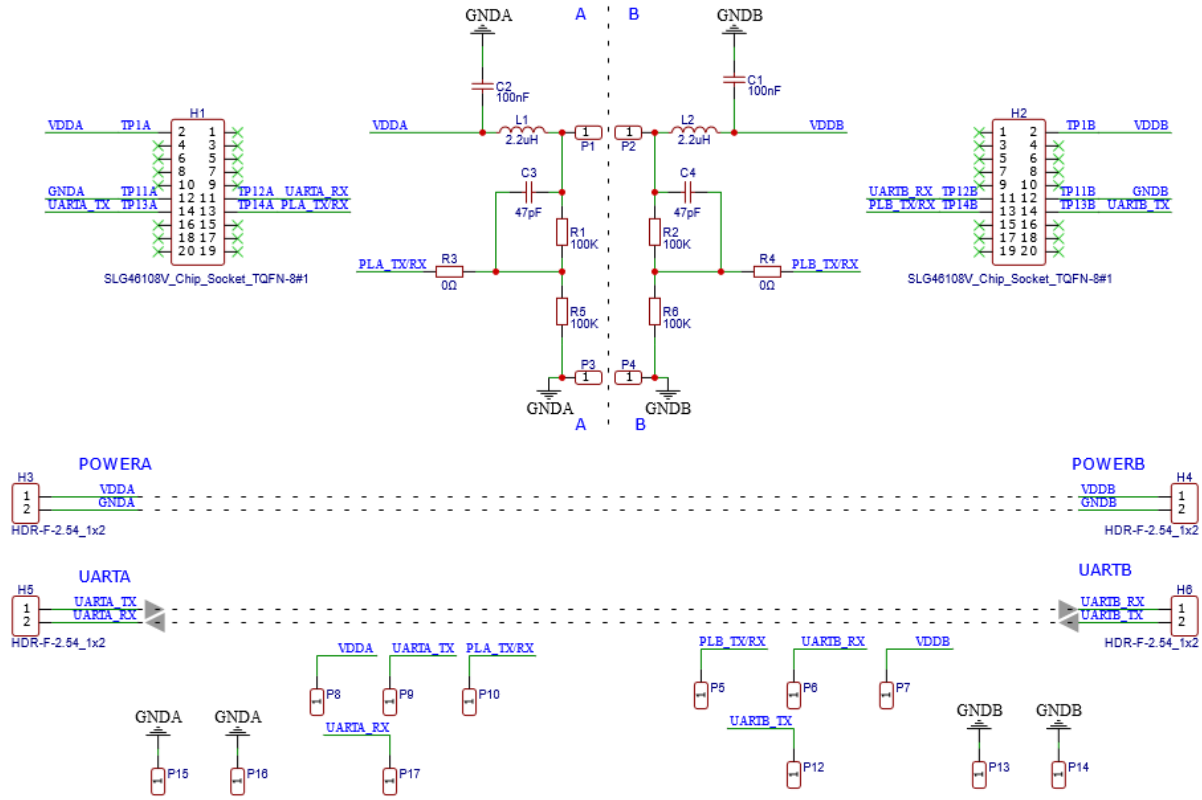

Figure 7: PCB Schematic

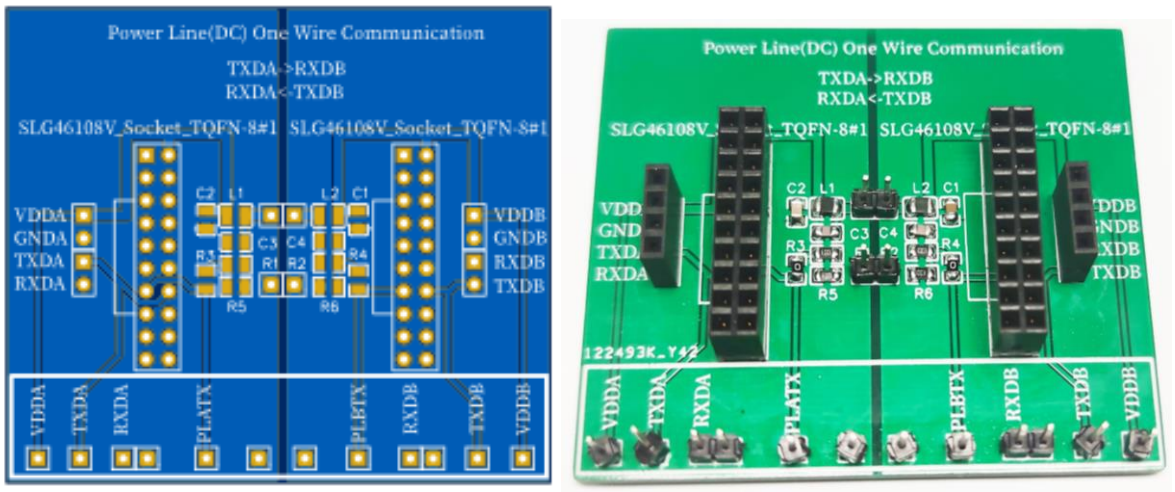

Figure 8: PCB with Prototype

8 Measurements

The board was tested with two Arduino boards as shown in Figure 9, Arduino A power by USB, Arduino B power by the power line. Figure 10 shows the Arduino programming used in the test. Arduino A sends a character 'A' every 10ms, Arduino B returns the received character. Figure 11 shows the waveform obtained in the test. Figure 12 shows the detail of the signal sent by PLA_TX/RX. Figure 13 shows the detail of the pulse received by PLB_TX/RX.

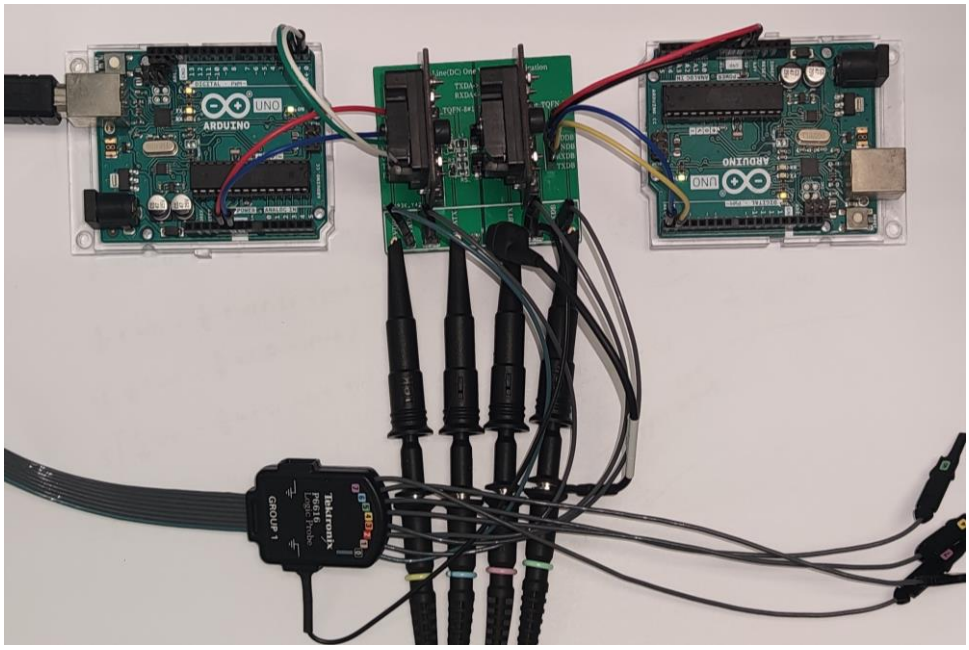

Figure 9: Testing with Arduino

```
//Arduino A Program.
void setup()
{
  // start serial port at 9600 bps:
  Serial.begin(9600);
  while (!Serial) {}
}

void loop()
{
  //send 'A' every 10mS
  Serial.write('A');
  delay(10);
}
```

```
//Arduino B Program
int inByte = 0;
void setup()
{
  Serial.begin(9600);
  while (!Serial) {}
}
void loop()
{
  if (Serial.available() > 0)
  {
    //send the received byte
    inByte = Serial.read();
    Serial.write(inByte);
  }
}
```

Figure 10: Arduino Programming

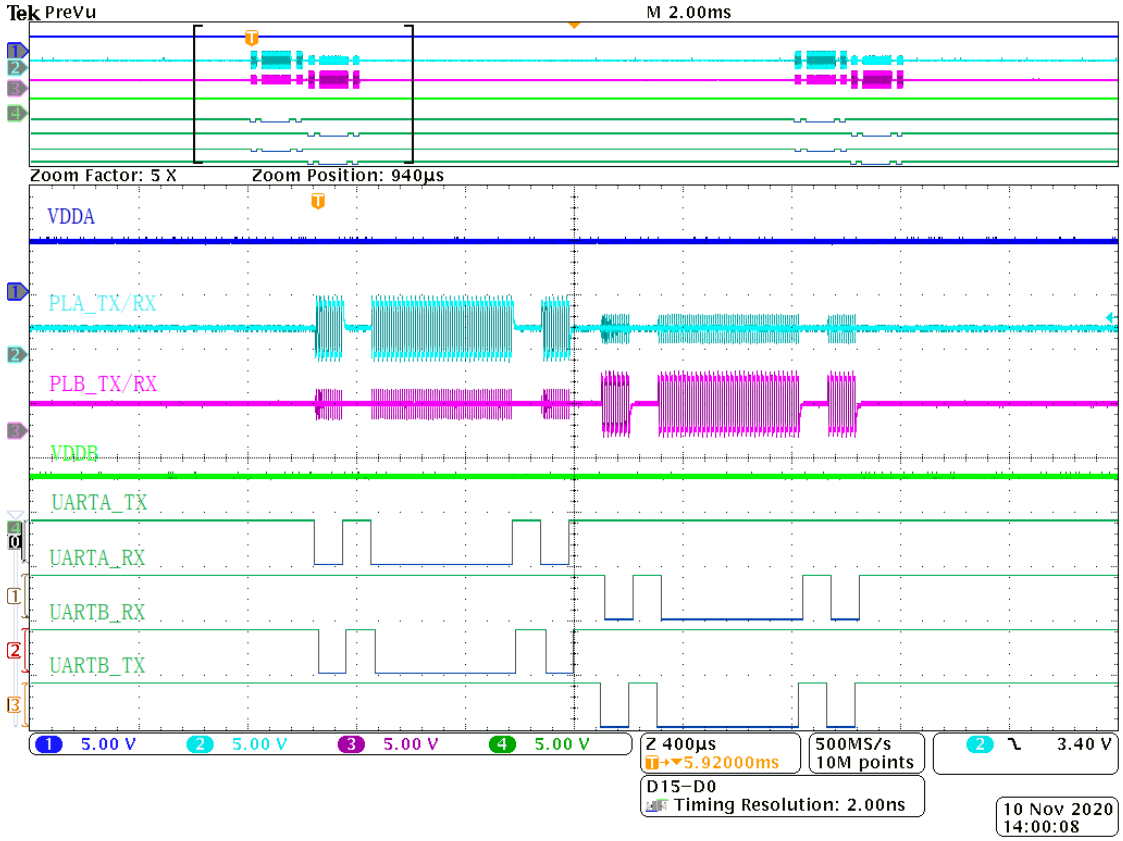

Figure 11: Waveforms of Power Line Communication

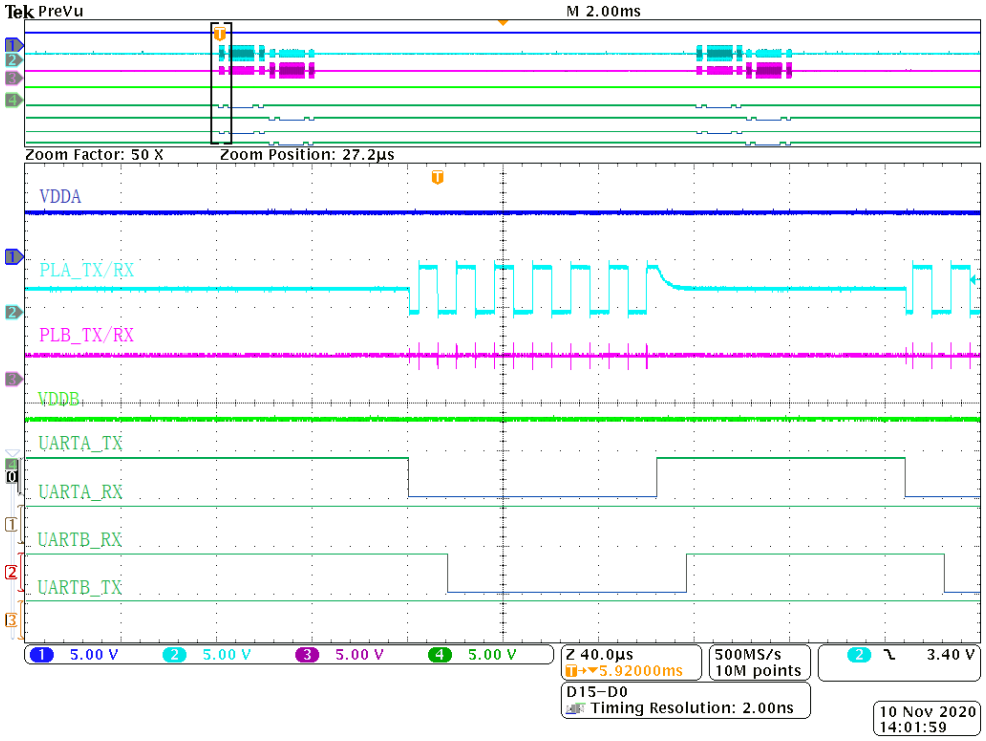

Figure 12: The detail of the signal sent by PLA_TX/RX

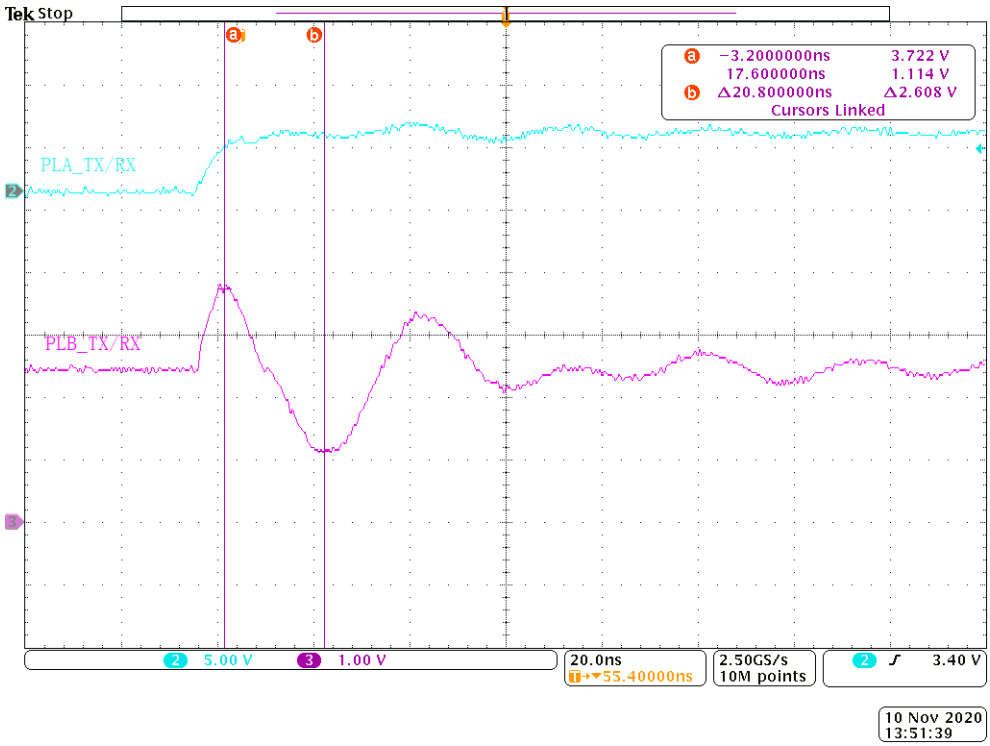

Figure 13: The detail of the signal received by PLB_TX/RX

9 Conclusion

This application note presents how to implement a low cost, low power, DC power line communication based on GreenPAK and capacitive coupling. Compared with other solutions, the main advantage of GreenPAK is that the communication method or content can be modified as needed. For example, you can easily modify the carrier frequency to suit the required communication baud rate. In addition, you can use the DFF inside the GreenPAK IC to form parallel-to-serial components, directly serialize the IO state and transmit it to the power line without the involvement of the MCU. The GreenPAK which includes ACMPs can easily transmit the battery level information into the power line.

Revision History

Revision	Date	Description
1.0	6-Sept-2021	Initial version.

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