

AnalogPAK™ Potentiometer Controlled by an Encoder SLG47001

This application note was developed using the SLG47001 and illustrates how to use it to control a potentiometer with an encoder and to implement an adjustable voltage divider based on it. The same design is fully compatible with the SLG47003 and SLG47004.

The application note comes complete with design files which can be found in the Reference section.

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1. Terms and Definitions

CLK	Clock
CNT	Counter
DFF	D flip-flop
LUT	Look-up table
OSC	Oscillator

2. References

For related documents and software, please visit:

[AnalogPAK | Renesas](#)

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the AnalogPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC. We also recommend that you familiarize yourself with the full capabilities of the AnalogPak SLG47001 [5].

[1] [GreenPAK Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics

[2] [AN-CM-320 AnalogPAK™ Potentiometer Controlled by an Encoder.aap](#), AnalogPAK Design File, Renesas Electronics

[3] [AnalogPAK Development Tools](#), AnalogPAK Development Tools Webpage, Renesas Electronics

[4] [GreenPAK Application Notes](#), GreenPAK Application Notes Webpage, Renesas Electronics

[5] [SLG47001 Datasheet](#), Renesas Electronics

3. Introduction

There are many applications in which a mechanical potentiometer forms part of a user-control interface. Such mechanical potentiometers can be replaced with more modern and reliable encoder-controlled elements together with digital rheostats, which adjust the electrical parameters of a signal.

The SLG47001 is an excellent solution that combines two digital rheostats with configurable logic for processing the encoder information. This combination enables a wide range of designs — a regulated power supply, an amplifier with adjustable gain, and others. In addition, the on-chip digital logic makes it possible to determine the speed of encoder rotation. This approach is shown in **Error! Not a valid bookmark self-reference..**

The design described in this application note targets the SLG47001 and is also fully compatible with the SLG47003 and SLG47004.

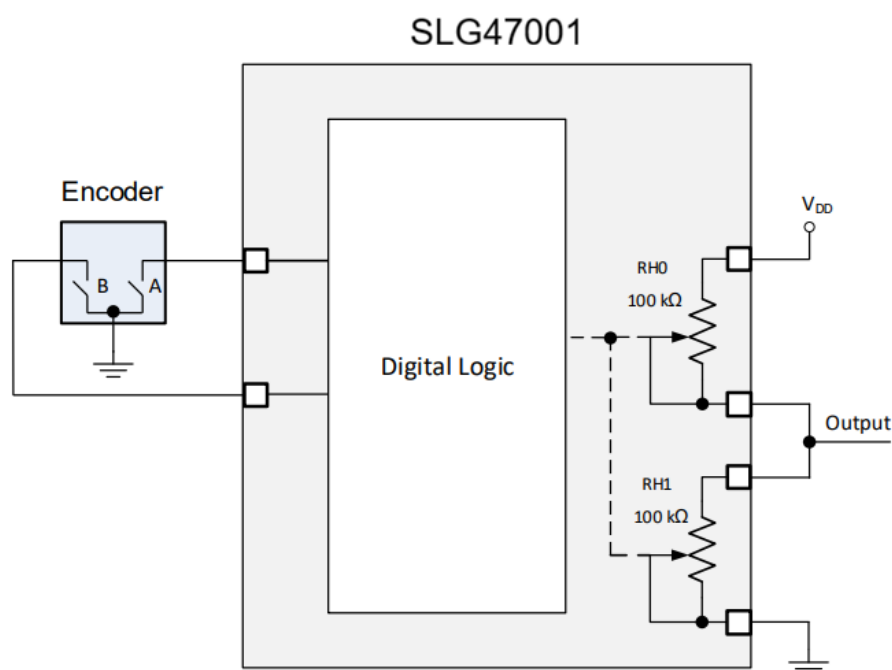


Figure 1. General Schematic of a Voltage Divider Controlled by the Encoder

4. System Overview

Figure 2 shows the internal design based on the SLG47001.

An incremental encoder generates the A and B output signals that are used to change the digital-rheostat resistance. The rheostats form the potentiometer and implement the adjustable voltage divider that regulates the output voltage.

At any given moment, the phase difference between the A and B signals is positive or negative depending on the direction of encoder movement.

The speed-determination function is built from Frequency Detectors, One Shots, and Multiplexers.

This application note uses the EC11 encoder. The encoder produces noisy output transitions caused by switch bounce; to suppress this noise, 2 ms delays are used. Note that this delay is tuned for the EC11 encoder (according to its datasheet). For other encoders the delay value should be evaluated accordingly.

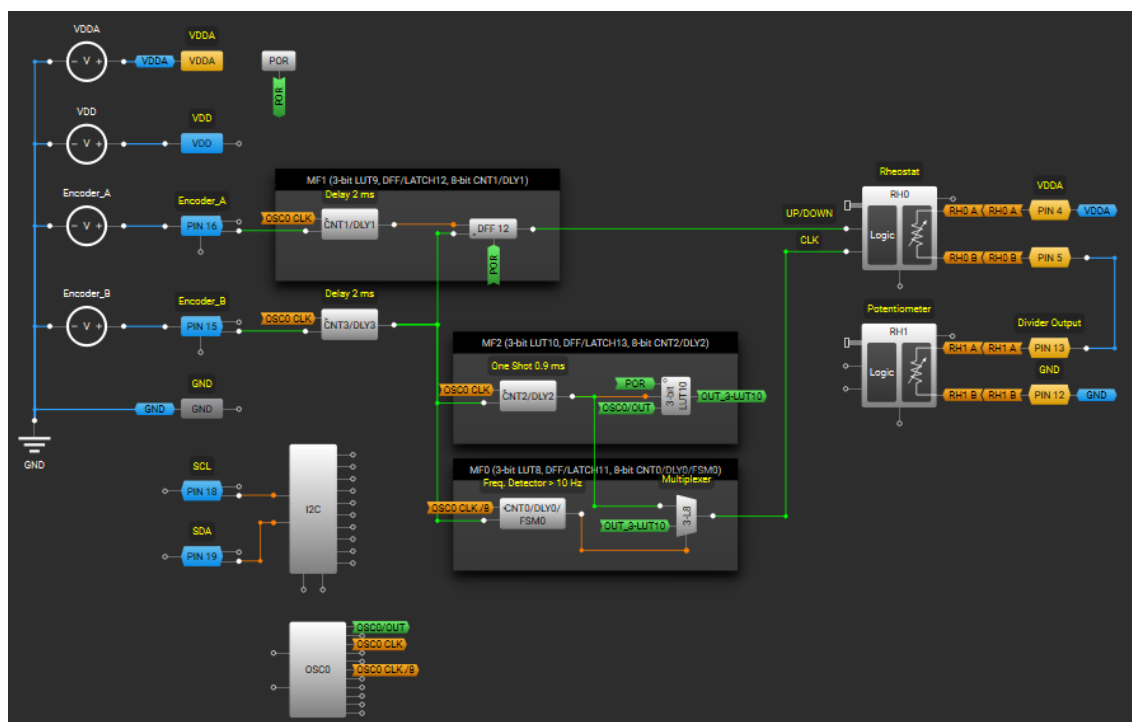


Figure 2. GreenPAK Designer Project

5. Functional Block Architecture

5.1 Digital Logic Description

5.1.1 Determining the Encoder Direction

First, the Delay macrocells delay both edges of the encoder output signals by 2 ms. The Delay macrocells act as a deglitch filter that removes switch bounce. The delayed B signal is applied to the DLY inputs of the One Shot and Frequency Detectors and to the CLK input of the DFF, while the delayed A signal is applied to the D input of the DFF. When the encoder disk rotates clockwise, signal A leads signal B and the DFF output is High; when it rotates counterclockwise, signal B leads signal A and the DFF output is Low. The DFF therefore determines the direction of rotation. The High or Low level on the rheostat Up/Down input determines whether the internal counter increments or decrements on each pulse at the CLK input.

A timing diagram for clockwise rotation is shown in , and for counterclockwise rotation in

Figure 4. Timing Diagrams for Counterclockwise Encoder Rotation

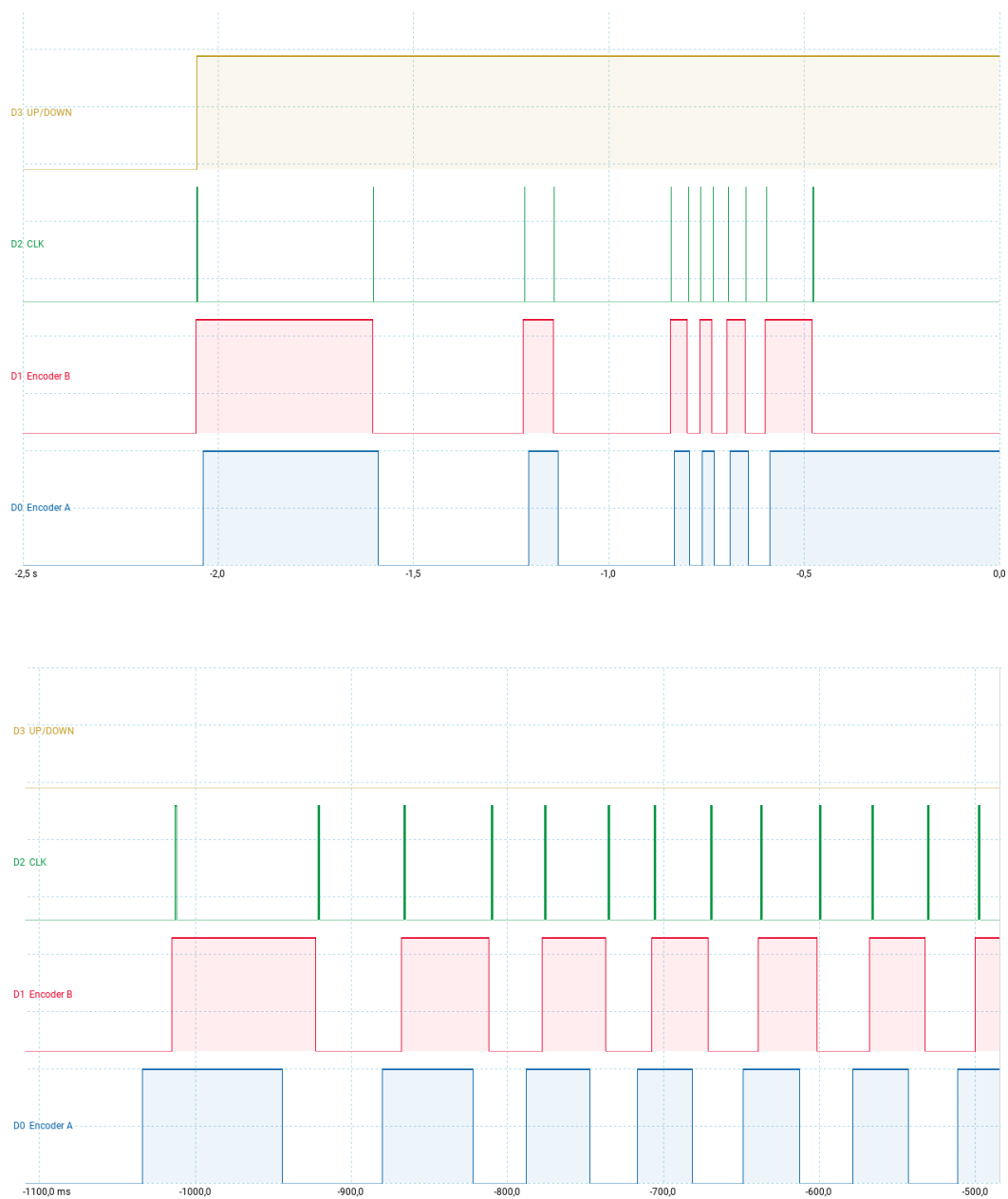
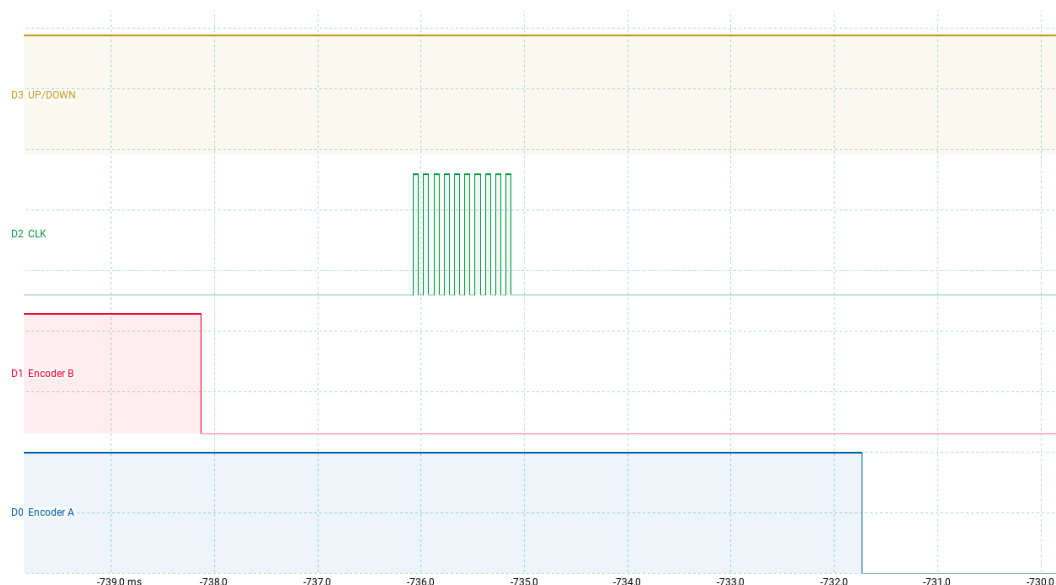


Figure 4. Timing Diagrams for Counterclockwise Encoder Rotation

Figure 3. Timing Diagrams for Clockwise Encoder Rotation



5.1.2 Determining the Encoder Speed

The SLG47001 has 10-bit digital rheostats, which provide 1024 regulation steps. The adjustable voltage divider has two regulation modes: the output can be changed in steps of 1 digital code (mode 1), or 10 digital codes (mode 2). Frequency Detector is used to implement the two modes. Mode 1 provides smooth, accurate adjustment and is active when the knob is turned at a rate below 10 Hz. Mode 2 is active when the rate is above 10 Hz.

The One Shot define the time intervals for the required number of pulses.

The digital Multiplexer pass either one, or ten pulses to the rheostat CLK input according to the Frequency Detector output.

5.1.3 Detents and Pulses per Revolution

An encoder in which the number of pulses and detents differ was used in this project. With 15 pulses, there are two detents per full pulse: for each pulse (cycle) of the rotary encoder there are two detents — one at the rising edge and one at the falling edge. If a rotary encoder has one detent per pulse, it produces two changes per pulse. For that type of encoder the design is unchanged except for the Frequency Detector and One Shot

Figure 5. Encoder fast-rotation mode (Mode 2), showing the generation of 10 clock pulses

settings: their Edge Select should be set to “Falling” or “Rising”. For encoders in which the number of pulses and detents do not match, Edge Select should be set to “Both”.

5.2 Potentiometer Mode

This design uses the digital rheostats in potentiometer mode, which allows two 2-pin rheostats to operate as a single 3-pin potentiometer. When this mode is enabled, the user changes the value of the RH0 internal counter;

the RH1 counter value is then the inverted value of the RH0 counter. Note that the RH0_B and RH1_A pins must be connected externally.

6. Conclusion

The SLG47001 provides two digital rheostats that enable a wide range of useful applications. One example is using the digital rheostats to replace an analog potentiometer with the help of a modern encoder. This application note shows how to use the SLG47001 to implement an adjustable voltage divider — a versatile solution that can be applied to an adjustable power supply, amplifier gain control, and more. The solution is cost-effective and consumes little power. The same design is fully compatible with the SLG47003.

7. Revision History

Revision	Date	Description
2.00	Jun 24, 2026	Changed the base part number
1.00	Aug 25, 2021	Initial release.

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