Application Note

Analog Front-End for Electrocardiogram Monitor AN-CM-326

Abstract

This application note describes the design of an analog front-end for an electrocardiography device. The circuit utilizes the commonly used technique of measuring electrical heart activity using three electrodes applied to the arms and legs. These electrodes detect the small electrical signal that results from cardiac muscle contraction (the heartbeat). The unique auto-trim feature of the SLG47004 enables output signal level stabilization in conditions of interference and baseline drift. The application note also contains test results of a hardware prototype.

This application note comes complete with design files which can be found in the References section.

Contents

Figures

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1 Terms and Definitions

AFE	Analog Front-End
ECG	Electrocardiogram
HR	Heart Rate
IC	Integrated Circuit
OpAmp	Operational Amplifier
INSTAmp	Instrumentation Amplifier

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/products/greenpak/analog-greenpaks/slg47004

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-326 Analog Front-End for Electrocardiogram Monitor.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47004, Datasheet

[6] Filters for ECG digital signal processing / Ondracek O., Jozef P., Elena C. // International Conference “Trends in Biomedical Engineering”. - University of Zilina, September 7 - 9, 2005. P. 91-96

[7] ECG Noise Cancellation Using Digital Filters / Hosseini H., Nazeran H., Reynolds K. // 2nd International Conference on Bioelectromagnetism, 1998. P. 151-152

Author: Svyatoslav Skalskyy

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3 ECG Basics and Analog Front-End Requirements

An electrocardiogram is a recorded electrical signal resulting from a contraction of heart muscles. It can detect deviation from a normal heartbeat and can be used to diagnose illnesses or optimize a training load. The signal must first be amplified to a level that is suitable for recording (electrodes on the arms can give voltages in the range of tens of microvolts to a millivolt peak-to-peak). The bandwidth of the signal is from 0.05 to 100 Hz. To amplify such a small signal, an amplifier with a gain of around 1000 should be applied. AC interference from the power grid should be canceled out along with DC offsets from the electrodes. As a rule, an instrumentation amplifier with a large common-mode voltage suppression is used. The common mode voltage is then amplified, inverted, and fed into a leg electrode for active interference suppression. Additionally, a low-pass filter, high pass filter, and band suppression filter are applied after amplification.

All electrical connections of the amplifier have to be isolated from mains and from devices supplied from it. It is difficult to construct a power supply with a small amount of stray capacitance to mains, so we will choose a battery-powered device, which will provide a simple solution for a low cost and isolated power source with a minimum amount of stray capacitance.

The SLG47004 can deliver only one instrumentation amplifier, so we will use AC filtering on the digital side. We will use a simple DC reference point for a leg electrode without active interference cancellation.

4 Top Structure of the Analog Front-End

The simplified structural scheme is shown in Figure 1.

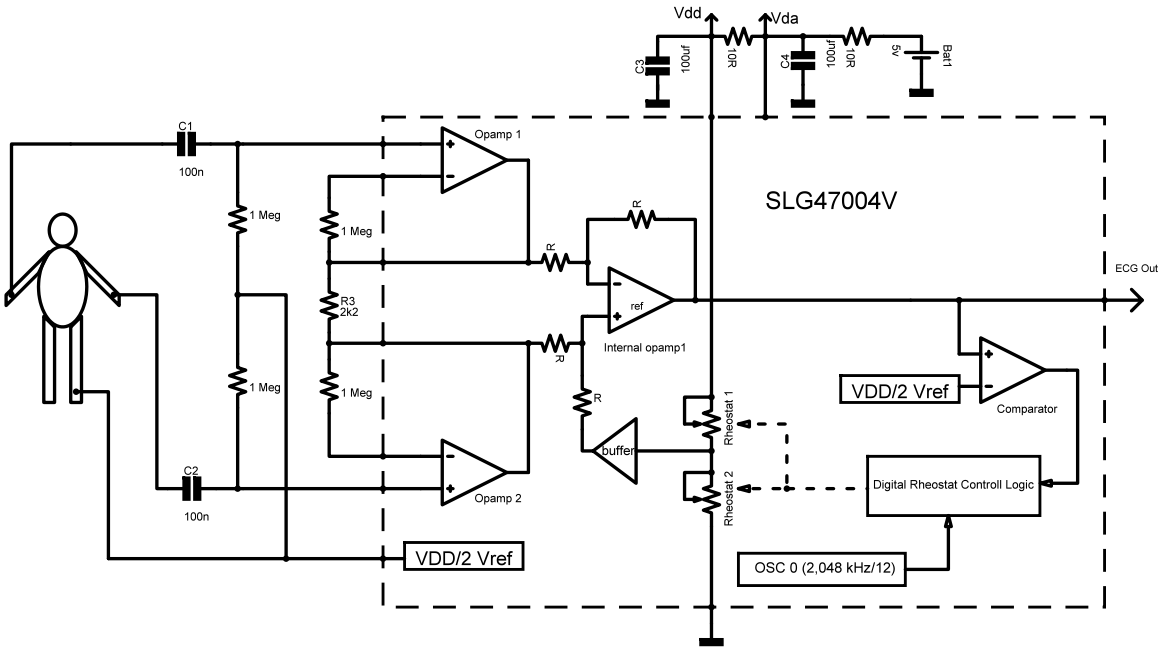

Figure 1: Structure of ECG Analog Front-End

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4.1 Typical Human ECG Waveform

A typical electric signal from a heart, picked up by the electrodes on the arms, is shown in Figure 2. The typical ECG waveform has 5 peaks called P-Q-R-S-T. These peaks correspond to the activity of different parts of the heart.

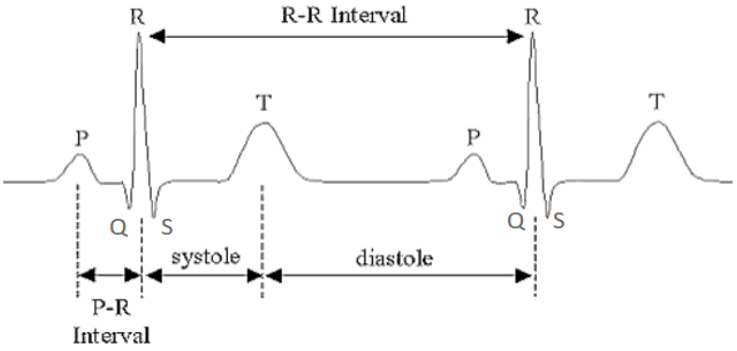

Figure 2: Typical ECG of Healthy Heart

5 SLG47004 Internal Design

The proposed design configuration is shown in Figure 3.

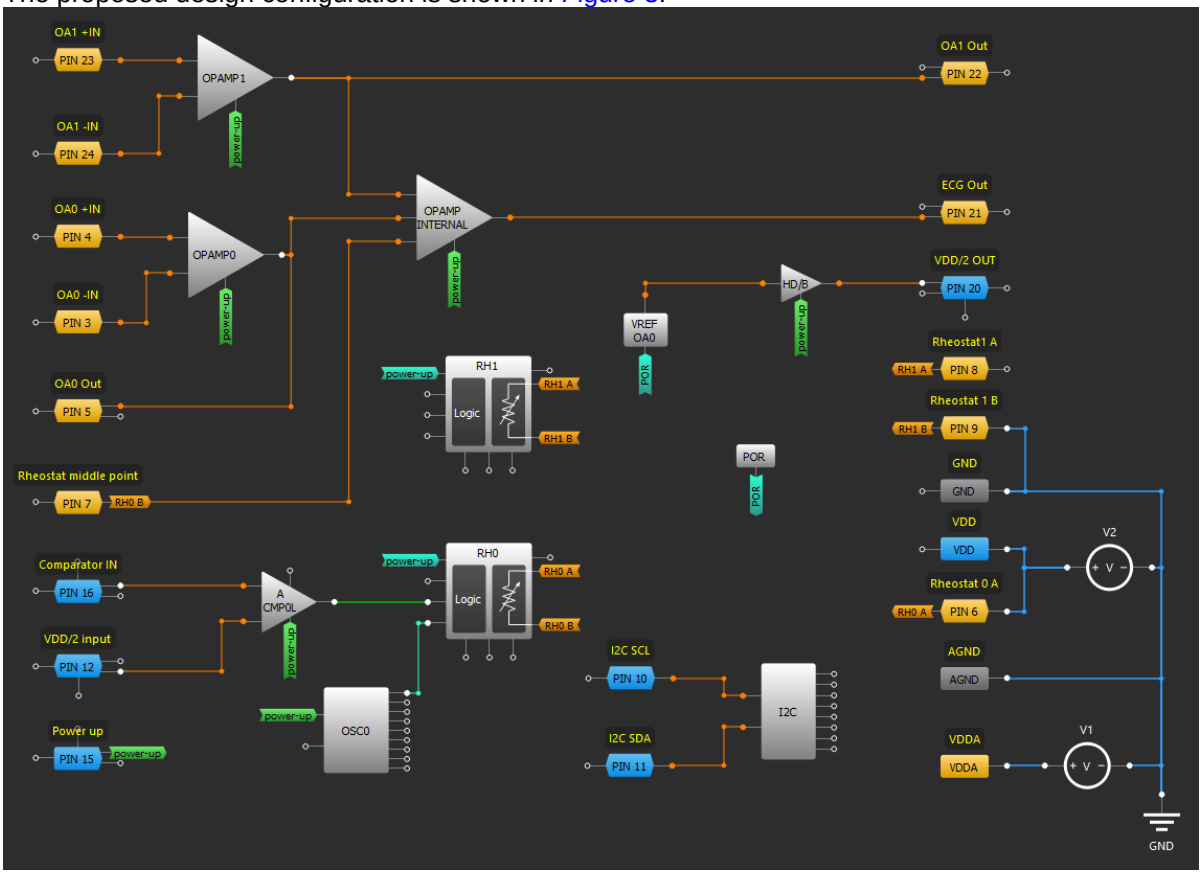

Figure 3: Design Configuration of SLG47004

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5.1 Electrical Schematic of Analog Front-End

The electrical schematic of the analog front-end is shown in Figure 4.

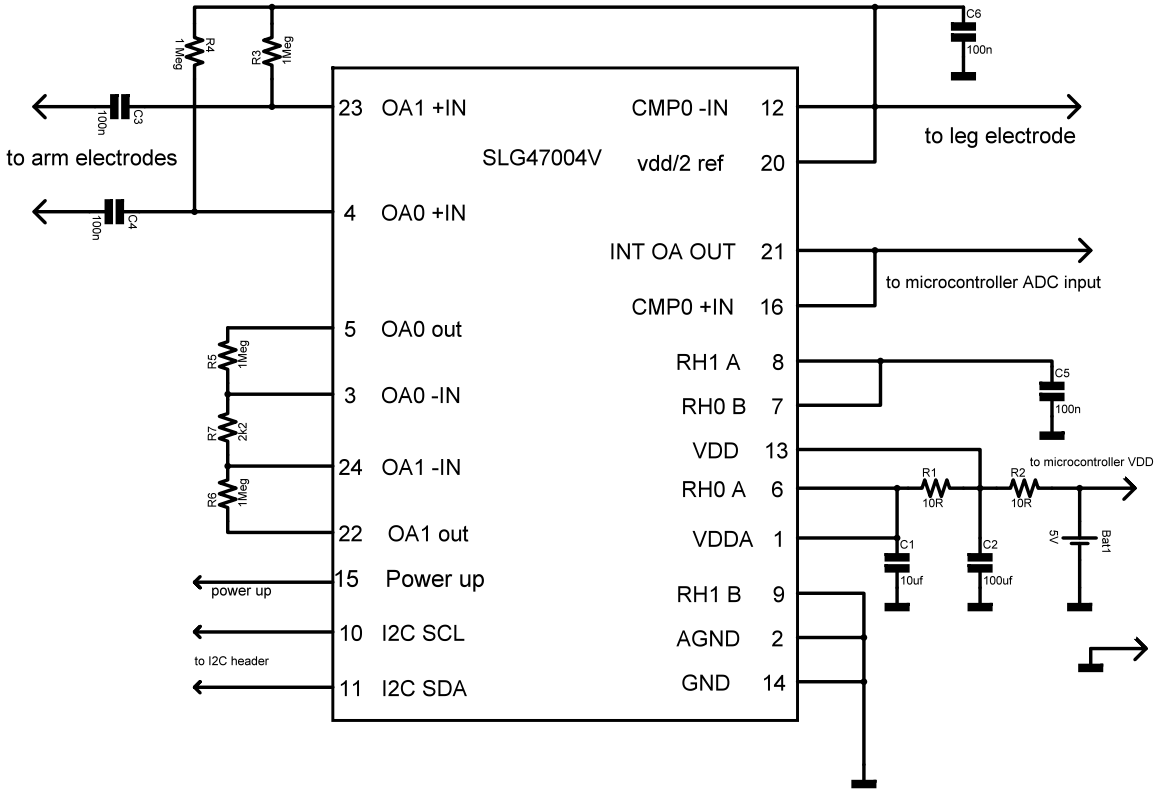

Figure 4: Electrical Schematic of Analog Front-End

6 Internal Block Configuration

6.1 OpAmp0 and OpAmp1 Configurations

OpAmp0 and 1 use the same configuration, shown in Figure 5.

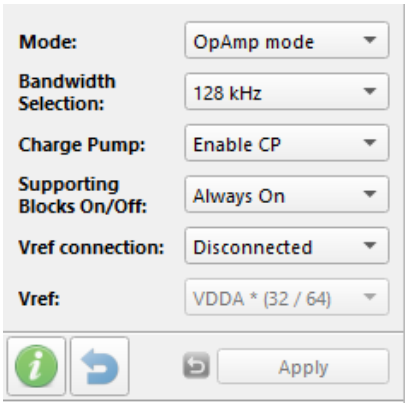

Figure 5: Operational Amplifier 0 and 1 Settings

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6.2 Internal OpAmp Configuration

The internal OpAmp configuration is shown in Figure 6.

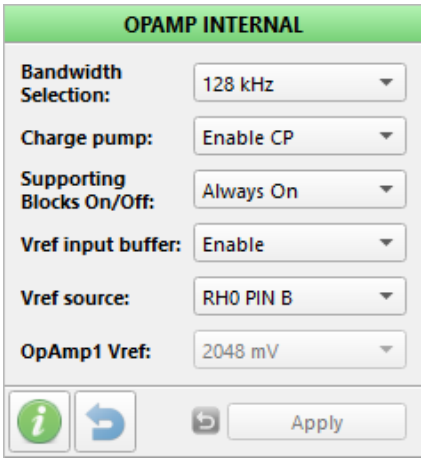

Figure 6: Internal OpAmp Settings

6.3 HD Buffer Configuration

The HD Buffer shares the voltage reference with OpAmp0. In the current project, the internal Vref is disconnected from OpAmp0. The HD Buffer and OpAmp0 Vref configurations are shown in Figure 7.

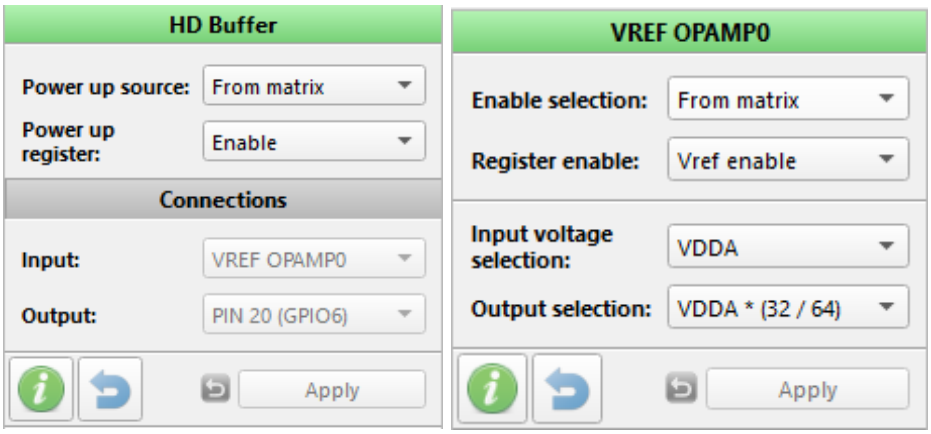

Figure 7: HD Buffer and OpAmp0 Vref Settings

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6.4 Rheostat0 and Rheostat1 Configuration

The rheostat in this project is configured as a digital potentiometer. Its configuration is shown in Figure 8.

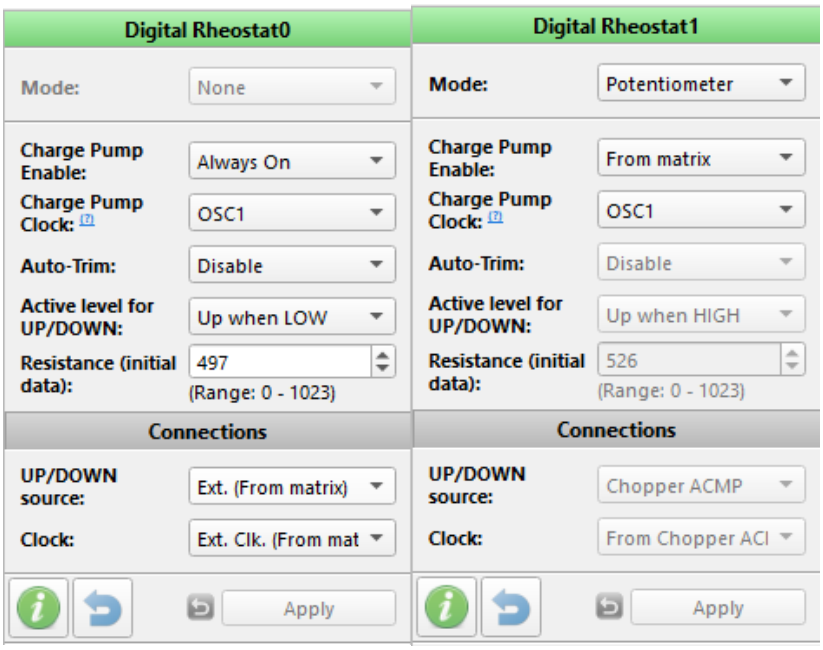

Figure 8: Digital Rheostat 0 and 1 Settings

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6.5 Oscillator Configurations

The configurations of Oscillator 0 and 1 are shown in Figure 9.

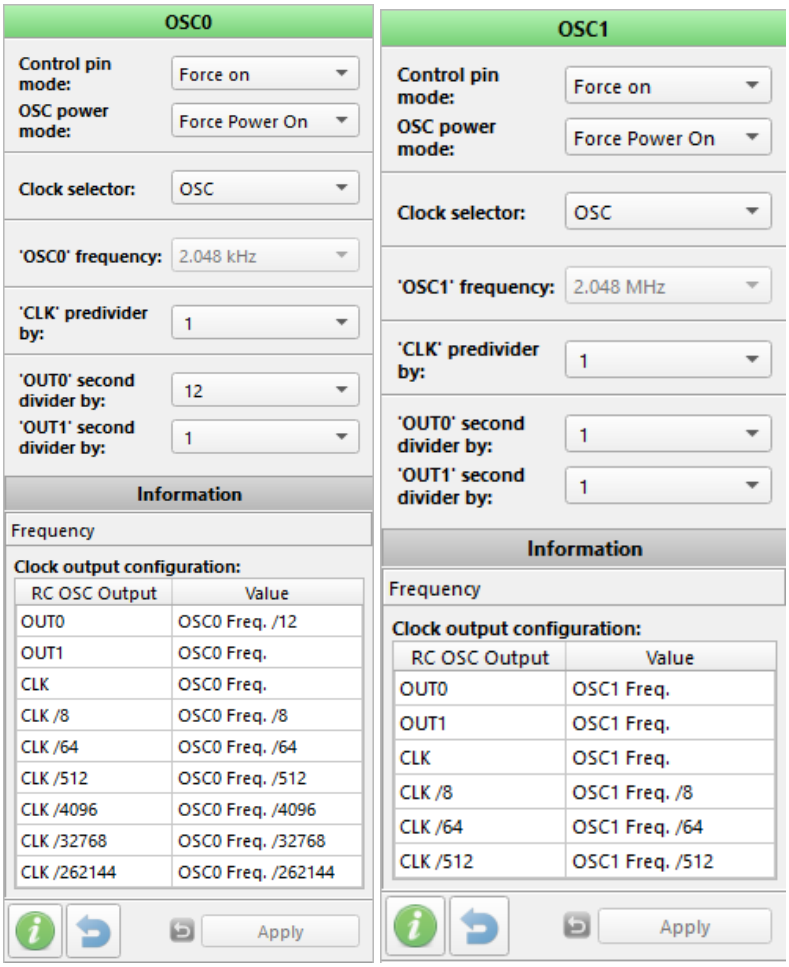

Figure 9: Oscillator 0 and 1 Settings

6.6 I²C Macrocell Configuration

The I²C macrocell uses default configurations.

6.7 GPIO Configurations

GPIO Pin 17,18,19,10, and 11 have the default configuration.

The remaining GPIO configurations are shown in Figure 10.

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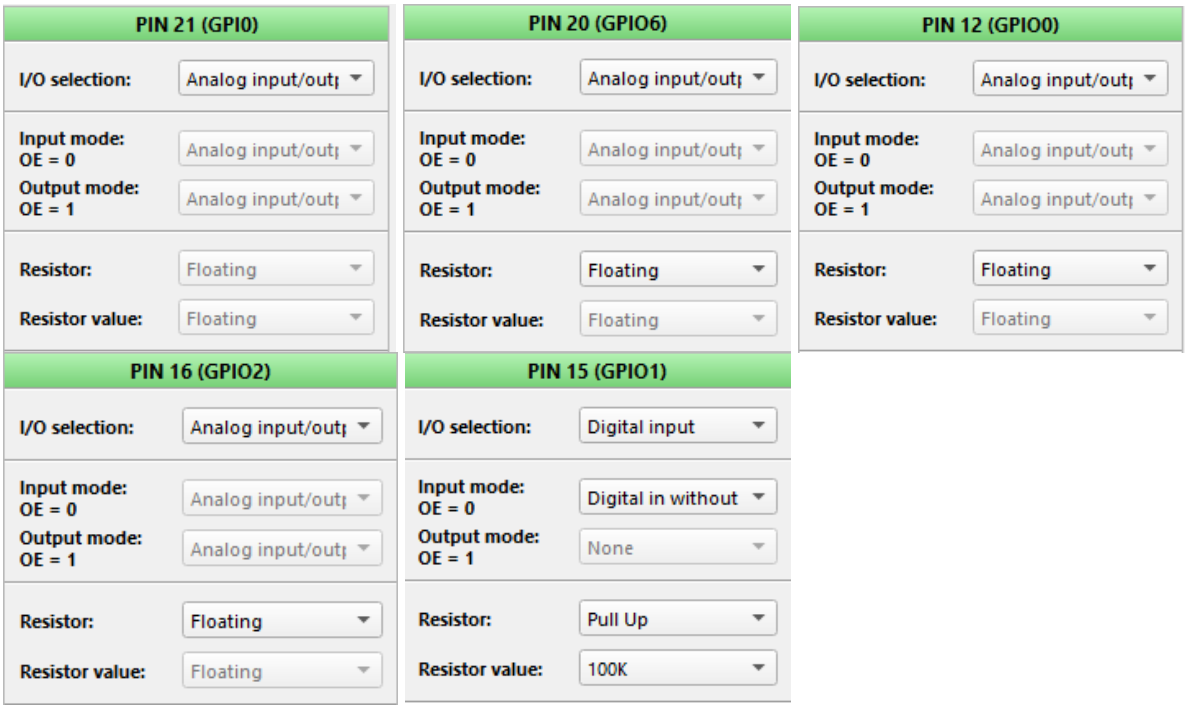

Figure 10: GPIO Settings

7 Normal Operation Mode

Power up Pin 15 has a 100kΩ pull-up resistor, and if left floating will by default power up the oscillator, all three op amps, and the rheostat. When Pin 15 is pulled down by external components, all internal blocks shut off and the SLG47004 goes into power saving mode.

Electrodes on the skin and body have a very high impedance, so common-mode AC power interference is accepted by the electrodes.

Instrumentation amplifiers are good at rejecting common-mode signals, and they also have high-impedance inputs, which are needed for amplification of the very small signal produced by heart muscles in the noisy environment. AC signals from arm electrodes go to an RC high-pass filter (R3, R4, C3, and C4 in Figure 4) with a low cut-off frequency, which eliminates a DC offset that might be present at the input due to the electrochemical processes between the electrode, conductive paste, and the skin. An even DC bias of VDD/2 is introduced to both of the op amp inputs to shift the operation point of the op amp, preventing it from going beyond rails. The voltage divider from R6, R7, and R5 (in Figure 4) forms an external negative feedback loop for an instrumentation amplifier from three op amps in the SLG47004 and has a gain of 910.

The Internal op amp has four resistors with the same value, forming a differential amplifier with a gain of 1.

Op amps have an input offset voltage. In our case, the SLG47004 has a max 1000 uV input offset voltage. This will be amplified by a factor of 910 and can produce up to 1 V of output voltage offset and reduce headroom for our signal, clipping it to GND or VCC (keep in mind that VCC is only 5 V).

To compensate for that error, an auto-trim circuit with digital potentiometer is used. This uses an analog comparator to switch the direction of the digital potentiometer change (up/down), which is clocked by the oscillator.

We are using slow tuning of the instrumentation amplifier reference point to cancel out op amp offset voltages. Multiplied by a large gain factor, they will overload the amplifier output without compensation. A slow floating offset voltage presented by muscle shaking, somatic tremor, or

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galvanic contact of electrode metals to the skin are all sources of interference that must be canceled out. The entire circuit of the comparator, reference voltage, potentiometers, and a clock signal slowly adjust an average DC level of the amplifier to a reference voltage level, which is set to VDD/2. The rate at which the voltage at the potentiometer output is changing is proportional to a clock frequency, fed into a potentiometer block. Assuming the potentiometer has 1023 steps and is connected to a supply voltage of 5 V, and has a clock of 170 Hz, the auto-trim control loop will have a slew rate of 0.83 V/s. It will also act as a high pass filter with a very low frequency cut-off.

We must consider the error presented by the constant auto-trim process, but in most use cases this is negligible and can be tolerated. If it is undesirable, it can be configured to be switched off after a trimming period using the internal SLG47004 logic.

A reference point of VDD/2 potential is fed into the leg electrode, which also becomes present at both sides of capacitors C3 and C4, preventing them from charging (so you don’t have to wait until the output signal settles due to the input capacitors' charging time).

8 Prototype Testing

Figure 11 and Figure 12: show the waveform at the analog output of the SLG47004. The raw analog output signal has a high level of 50 Hz noise. Such measurements can't be analyzed, and this is a typical problem for electrocardiography. That's why additional filtering should be applied to the signal.

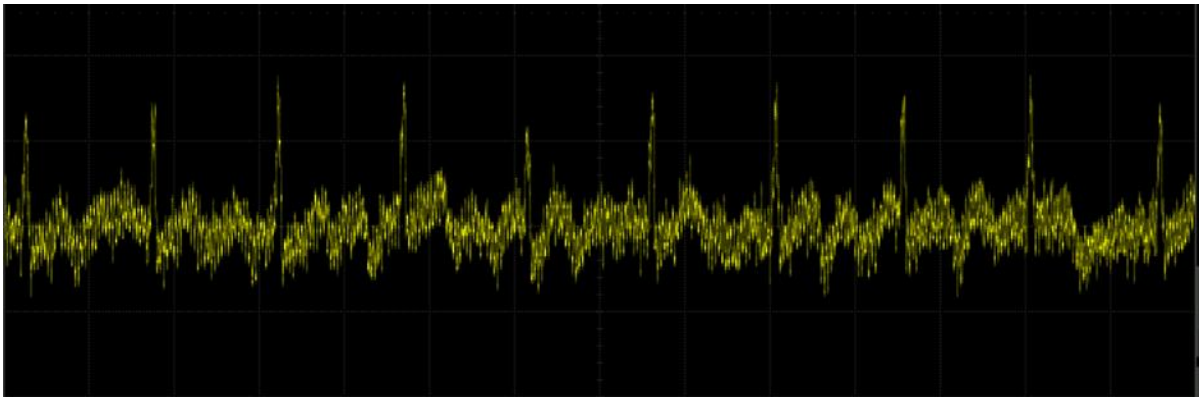

Figure 11: Seven Second Heart Waveform (500 mV/div, 500 ms/div).

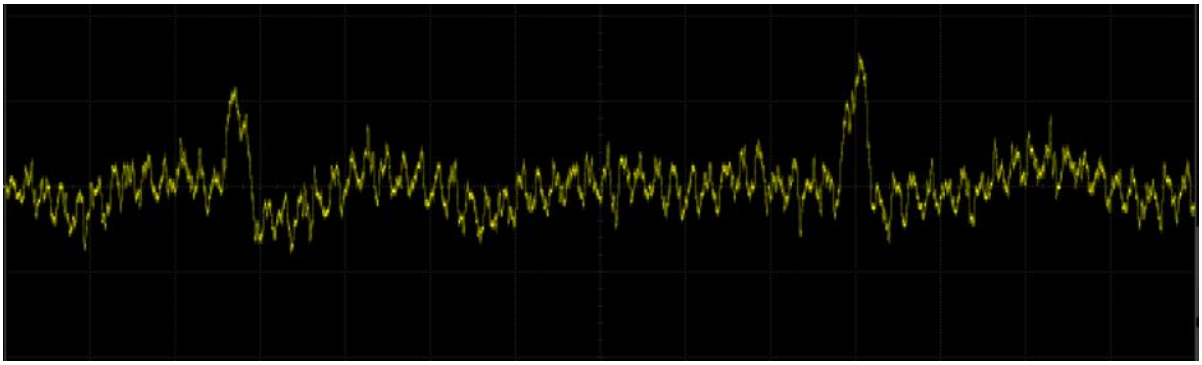

Figure 12: Zoomed Heart Waveform (100 mV/div, 500 ms/div).

The common approach is to apply digital filters to remove power grid noise as well as other noise components [2]. There are many articles that describe and compare different digital filtering approaches [2,3]. Since the purpose of this application note is to show the performance of the analog front-end, we will skip the digital filter synthesis procedure and show the filtered signal.

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Figure 13 shows the raw digitized signal. At the 1st filtering stage 50 Hz noise was removed (Figure 14). At the 2nd filtering stage a median filter was applied to the signal (Figure 15).

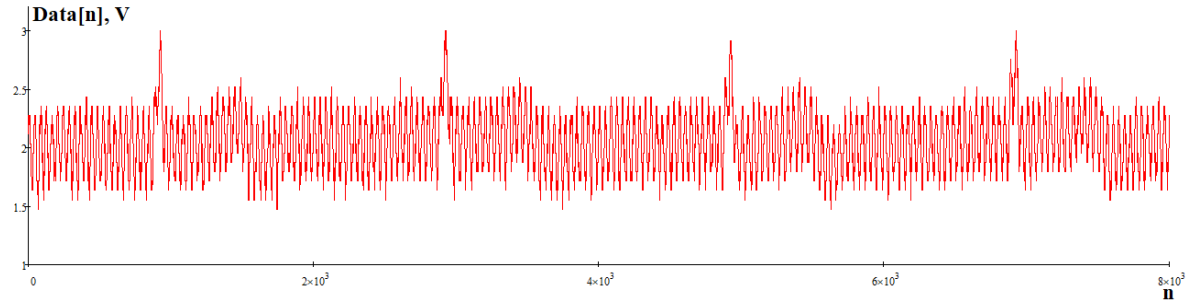

Figure 13: Raw Digitized Signal

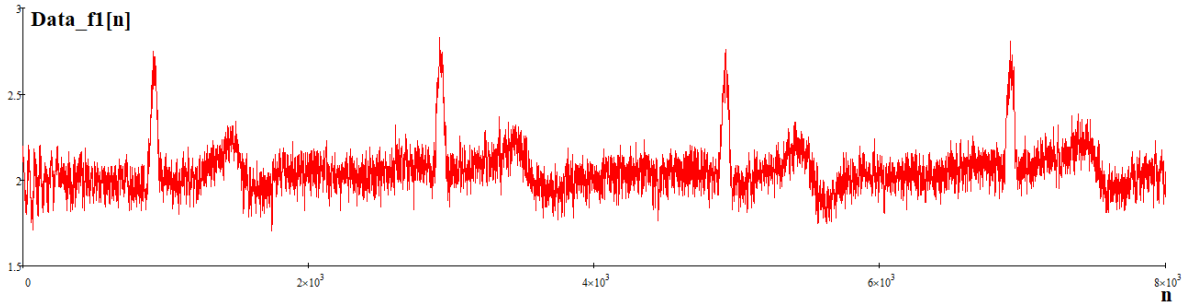

Figure 14: Signal Without 50 Hz Noise

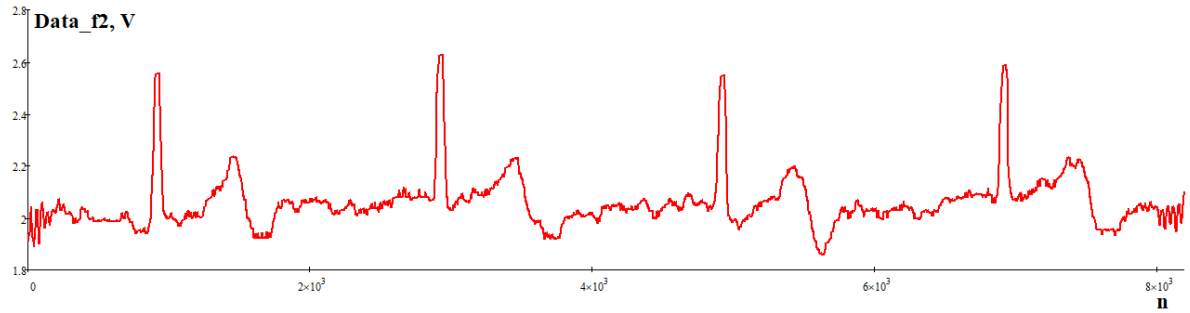

Figure 15: Signal After Median Filter

9 Conclusion

The SLG47004 can be used as a cost-effective integrated solution for the analog front-end of an electrocardiogram monitor. Its unique auto-trim feature allows it to cancel system offset as well as to provide steady output. The embedded instrumentation amplifier provides a good common mode interference rejection, the magnitude of which is much bigger than the signal itself.

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Revision History

Revision	Date	Description
1.0	08-Oct-2021	Initial version.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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