Using Renesas SLG59H1132V for Power Up on Heavy Loads
SLG59H1132V

This application note describes the use of the Renesas SLG59H1132V for power up on heavy loads.

Corresponding oscilloscope captures of operational behavior are included.

Contents

1. References

For related documents please visit:

Load Switches | Renesas

[1] SLG59H1132V Datasheet, Renesas Electronics

2. Terms and Definitions

MCU	Microcontroller Unit
SOA	Safe Operating Area
IC	Integrated Circuit
DC	Direct Current

3. Introduction

In modern times, every device strives to be as energy efficient as possible, especially in the case that the device runs on batteries or accumulators. In these instances, a load switch becomes a cheap and technological solution that makes it possible to control the power consumption of the device's various peripherals and/or sub-circuits. Additionally, a load switch has protection features that provide protection from overload or other power failures such as overvoltages, short-circuits, etc.

In case an application needs to control heavy load, the problem of efficiently avoiding a failure on start-up is raised. There may be certain Issues that can arise such as high in-rush current, as well as a possible exit outside of the safe operating zone of the FET that can cause start-up failure.

One of the ways to solve these problems simultaneously is to use a high-powered load switch with plenty of protection features. One of these load switches is the Renesas SLG59H1132V.

This article discusses how to use the Renesas SLG59H1132V to deal with heavy load properly and describe Safe Operating Area protection

4. FET Safe Operating Area Explanation

Apart from using power switches for controlling power rails On and Off, it is also important to have internal protection circuits inside the power switch that provides a self-saving function from situations such as overloading. Renesas' load switch devices have an internal Safe Operating Area (SOA) that helps to protect the device from overpower and overcurrent situations.

4.1 Overvoltage Transistor Junction Breakdown

This breakdown depends on Gate-Source Voltage (V_{GS}). When V_{GS} = 5 V, the transistor drain-source breakdown voltage is lower. This is because the gate voltage bias forms a drain-source charge channel, which lowers the voltage level to reach a condition known as Source Current Body Effect (SCBE). Once the gate voltage turns off (V_{GS} = 0 V), the FET can sustain higher drain-source voltage before breakdown. This is why Renesas' load switches have an overvoltage lockout (OVLO) feature to ensure that the FET immediately turns off the gate voltage if the drain voltage exceeds the manufacturer's specification. SOA curves for typical 24 V device are illustrated in Figure 1.

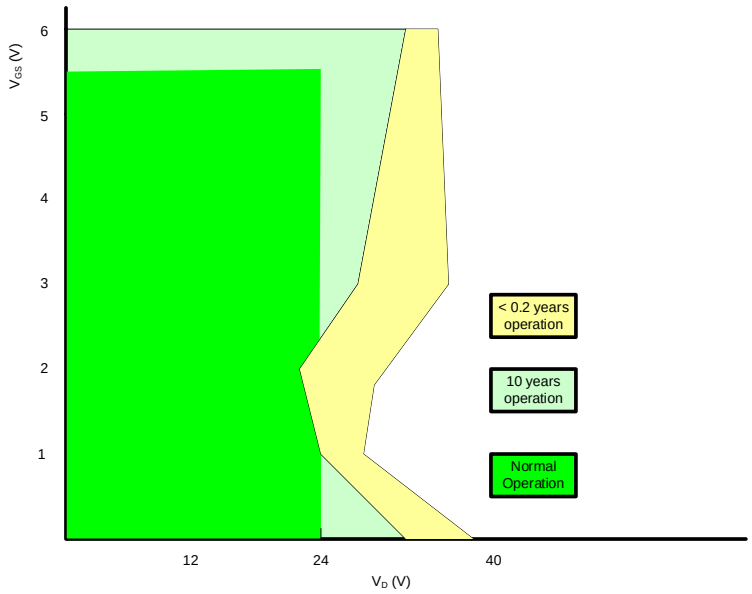

Figure 1: Safe Operating Area (SOA) for a typical 24 V device

4.2 Thermal Breakdown

Thermal breakdown may occur due to overheating from overcurrent or overpower operation. Overheating can be prevented by properly selecting the necessary RDS_{ON} for the maximum operating current on the system. Knowing the RDS_{ON} and maximum operating current, it is possible to calculate power dissipation on the FET:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

- PD_{TOTAL} = Total package power dissipation, in Watts (W)
- RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
- I_{DS} = Output current, in Amps (A)

Renesas provides the thermal data of the package as well as the layout guidelines to ensure efficient heat dissipation in all our power switch datasheets. Overheating from an overpower condition can occur when there is a soft short-circuit during start-up. The thermal rating (θ_{JA}) of most packages cannot handle more than 20 W. The temperature gradient is too high to dissipate this amount of power. An example of the power dissipation on the FET during start-up on a 10 Ω load is illustrated in Figure 2. To provide protection for Renesas' load switch, the V_{DS} and I_{DS} are monitored. This is the voltage and current across the drain-source of the FET and these two parameters are processed in the device to obtain the power across the FET. In Figure 2, the functional block diagram and operational timing diagram are illustrated. The next section will discuss how the Renesas load switch provides SOA protection.

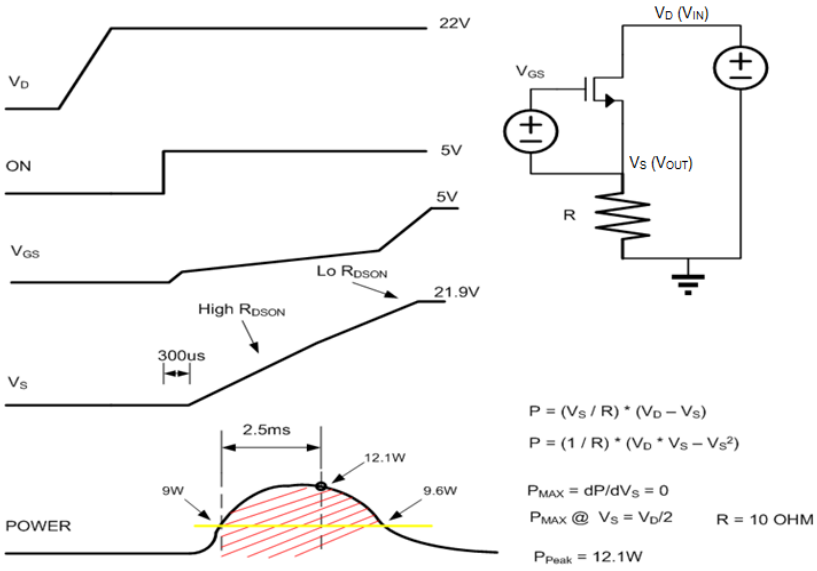

Figure 2: Power Dissipation on regular FET during power up without SOA

As can be seen from the graph above, the highest power dissipation with a linear increasing output voltage occurs at around the halfway point.

4.3 Calculating the Maximum Power Dissipation

To roughly calculate the maximum power dissipation during start-up on a resistive load only, use the equation below:

$$PD_{R\_MAX} = \frac{\left(\frac{V_{IN}}{2}\right)^2}{R_{LOAD}}$$

where:

- PD_{R_MAX} = Maximum package power dissipation for a resistive load only, in Watts (W)
- V_{IN} = Voltage applied to the FET Drain, in Volts (V)
- R_{LOAD} = Total resistive load, in Ohms (Ω)

When connecting to a capacitive load only, the power dissipation will be calculated by following equations:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV_{OUT}}{dt}$$

$$PD_C = I_{INRUSH} \times (V_{IN} - V_{OUT})$$

where:

- I_{INRUSH} = Capacitor charge current, in Ampere (A)
- C_{LOAD} = Output capacitance, in Farads (F)
- dV_{OUT}/dt = V_{OUT} slew rate, in Volts/ms (V/ms)
- PD_C = Package power dissipation for a capacitive load only, in Watts (W)

The maximum power dissipation will occur in the very first moment, as initially, the discharged capacitor behaves as a short circuit, and can be calculated by following equation:

$$PD_{C\_MAX} = I_{INRUSH} \times V_{IN}$$

where:

- PD_{C_MAX} = Maximum package power dissipation for a capacitive load only, in Watts (W)

However, in most applications, resistive loads are combined with a capacitive load. The maximum power dissipation for such cases is calculated in two steps.

First, calculate the relative coefficient k that determines which equation will be used for total package power dissipation calculations by the equation below:

$$k = \frac{V_{IN} - I_{INRUSH} \times R_{LOAD}}{2 \times V_{OUT(SR)}}$$

where:

- k = Relative coefficient
- I_{INRUSH} = Capacitor charge current, in Amperes (A)
- R_{LOAD} = Total output resistive load, in Ohms (Ω)
- V_{IN} = Input voltage, in Volts (V)
- $V_{OUT(SR)}$ = V_{OUT} Slew Rate, in Volts/ms (V/ms)

Next, the maximum power dissipation can be calculated by one of the following equations, depending on k:

$$PD_{MAX} = \frac{(I_{INRUSH} \times R_{LOAD} + V_{IN})^2}{4 \times R_{LOAD}}, \text{ if } k > 0$$

$$PD_{MAX} = PD_{C\_MAX}, \text{ if } k \leq 0$$

where:

- I_{INRUSH} = Capacitor charge current, in Amperes (A)
- R_{LOAD} = Total resistive load, in Ohms (Ω)
- V_{IN} = Input voltage, in Volts (V)
- PD_{MAX} = Maximum package power dissipation, in Watts (W)
- PD_{C_MAX} = Maximum package power dissipation for capacitive loads only, in Watts (W)

The diagrams below show the power dissipation waveforms for different types of load during power-up and indicate the peak package power dissipation for each load type. Please refer to Figure 3 for the case k > 0, and Figure 4 for k ≤ 0.

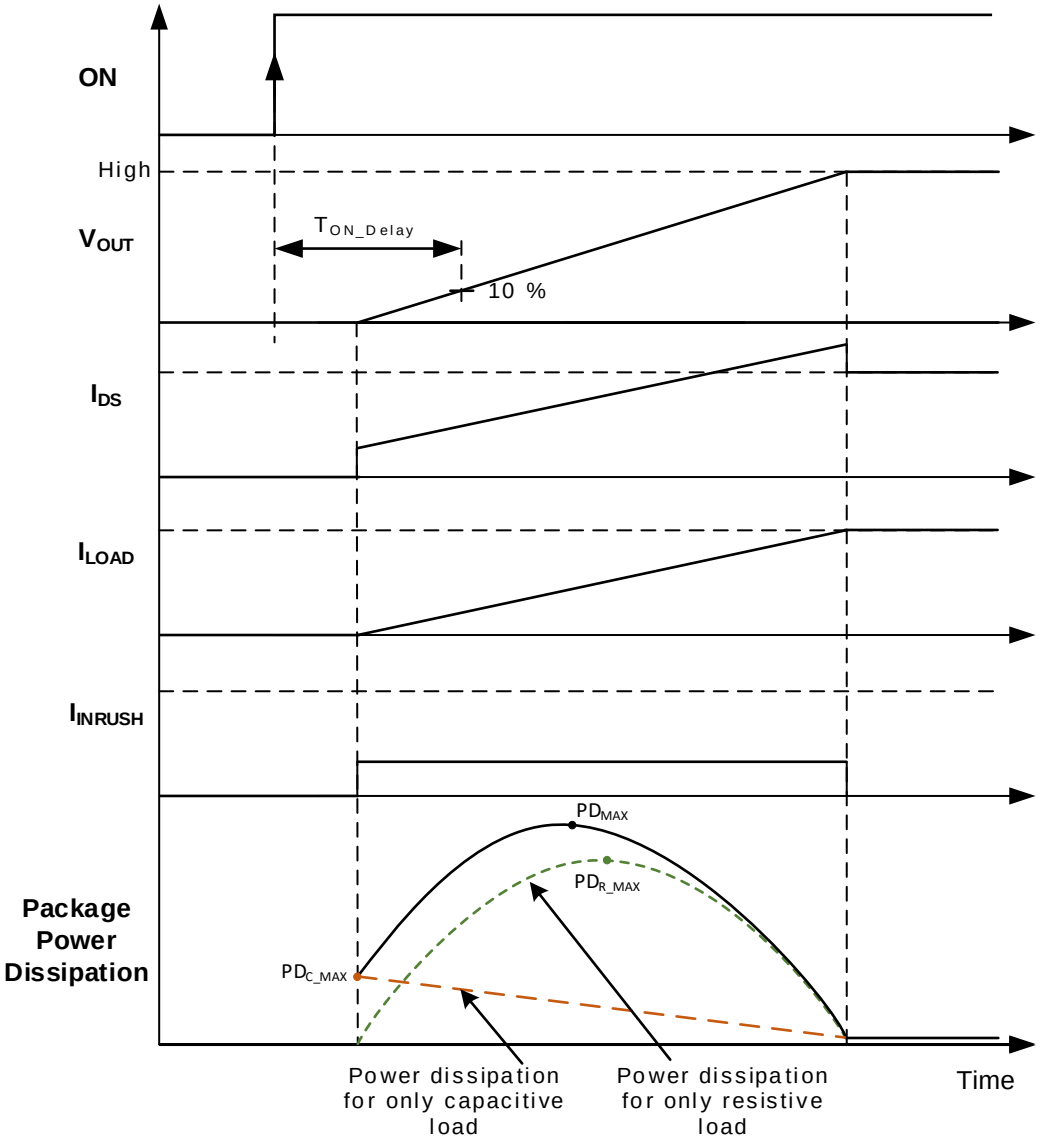

Figure 3: Package power dissipation waveforms for case: k > 0

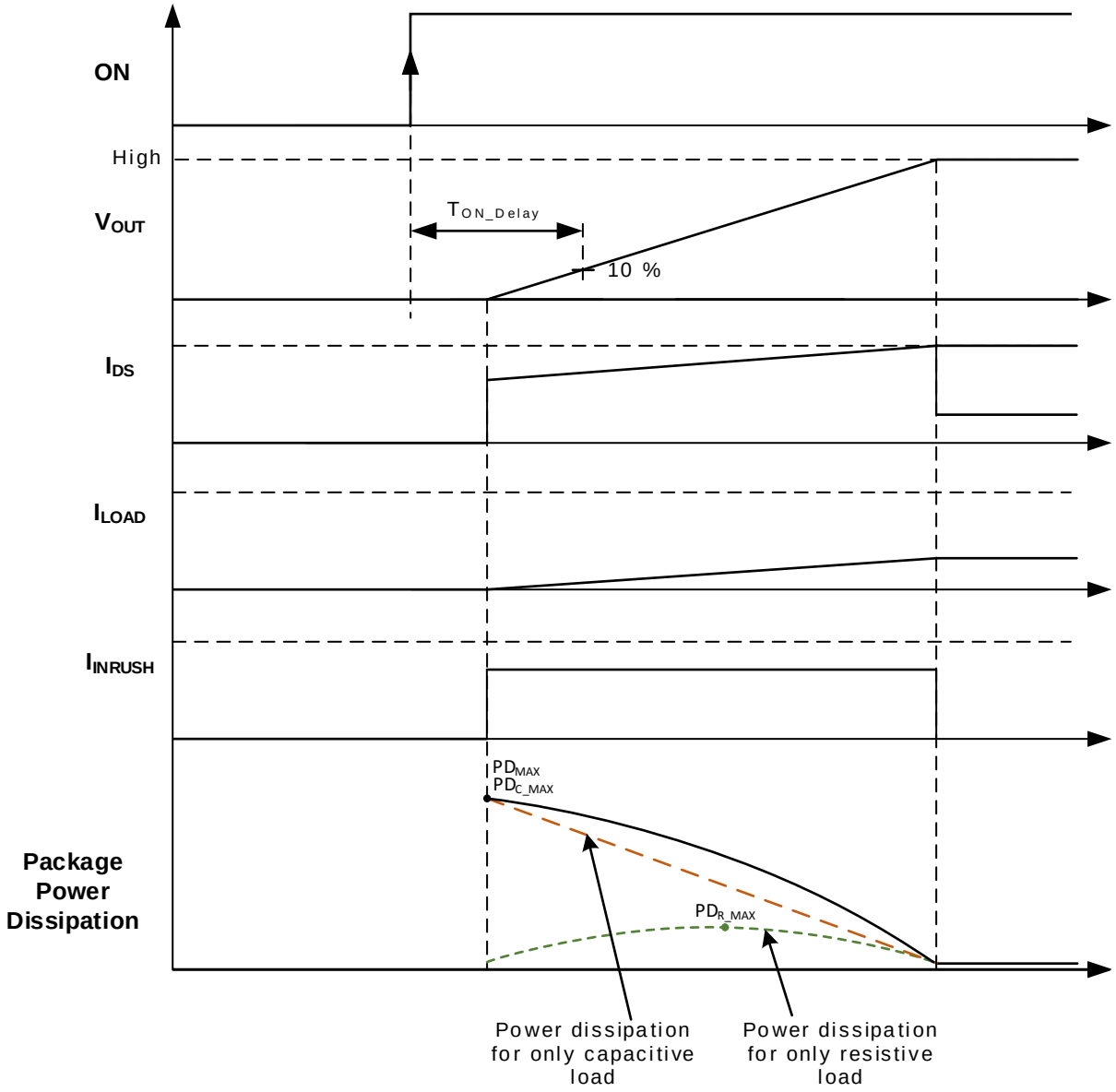

Figure 4: Package power dissipation waveforms for case: k ≤ 0

5. Application Information

5.1 SLG59H1132V Description

The SLG59H1132V is a 13 mΩ RDS_{ON} load switch designed to control 4.5 V - 22 V power rails and supports up to 6 A maximum operating current. It contains all the necessary logic blocks for protection against short-circuit, overcurrent, undervoltage and overvoltage lockout windows, overheating protection, and current monitoring.

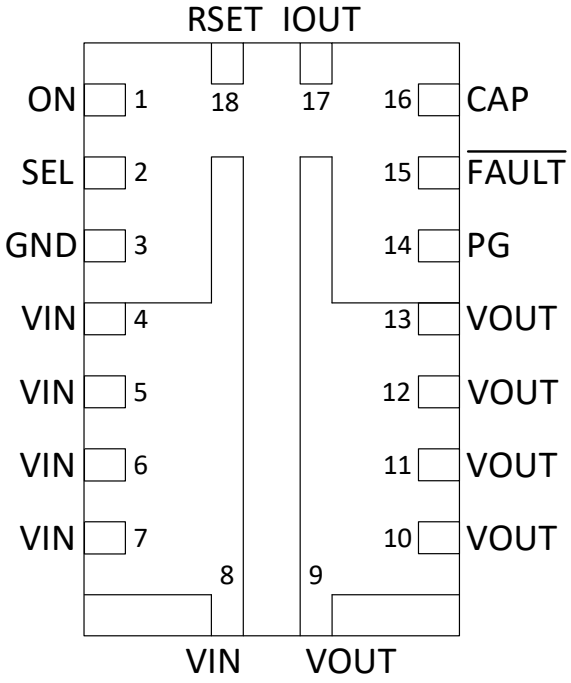

Figure 5: Pin Assignment for SLG59H1132V

The following list provides more details on the functions of each pin:

- **ON**: Initiates the operation of the SLG59H1132V's state machine when asserted HIGH. To disable the IC, the pin must be connected to GND as there is no internal pull-down resistor.
- **GND**: Ground connection. Connect this pin to system analog or power ground plane.
- **VIN**: Supplies the power for the operation of the SLG59H1132V, its internal control circuitry, and the drain terminal of the nFET load switch.
- **VOUT**: Source terminal pin of the nFET load switch.
- **SEL**: Selects one of the two overvoltage lockout thresholds.
- **FAULT**: Open drain output. FAULT is asserted within $TFAULT_{LOW}$ when a V_{IN} overvoltage, SOA protection, a current limit, or an over-temperature condition is detected.
- **PG**: Open drain output. PG is asserted within TPG_{HIGH} when V_{OUT} is higher than the SLG59H1132V's $PG_{TRIGGER}$ threshold.
- **CAP**: Sets the V_{OUT} slew rate and overall turn-on time.
- **IOUT**: Load current monitor output for the SLG59H1132V's power MOSFET.
- **RSET**: Sets the active current limit threshold. A 91 kΩ resistor sets the SLG59H1132V's active current limit to 1 A and a 14 kΩ resistor sets the active current limit to 7 A.

5.2 SLG59H1132V SOA Protection Overview

Each power switch has its own breakdown levels and as such, the SLG59H1132V load switch also has them. Internal SOA protection helps to expand these levels and protects the device from reaching them in the first place. To provide protection for Renesas' load switches, the V_{DS} and I_{DS} of the load switch are monitored. This is the voltage and current across the drain-source of the FET. These two parameters are processed in the device to obtain the power across the FET.

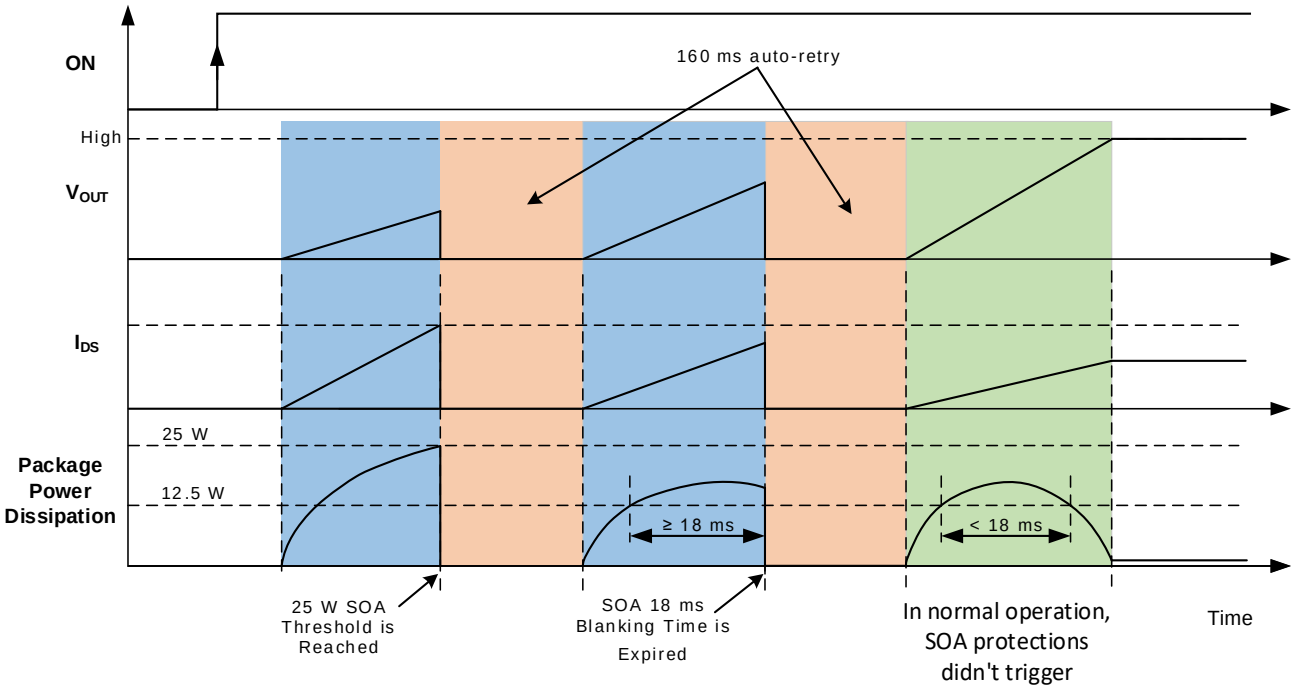

Figure 6: SOA operation during power-up at heavy load

The Renesas SLG59H1132V features two levels of SOA protection, as illustrated in Figure 6. The first level of SOA protection turns the device off immediately when the power dissipation exceeds the 25 W threshold. When shut down is initiated due to SOA protections, a restart is automatically attempted after a 160 ms delay. This timing interval allows time for the package to cool down and the device can return to normal operation once operating conditions return to normal. Figure 7 and Figure 8 are show the behavior of 25 W SOA protection.

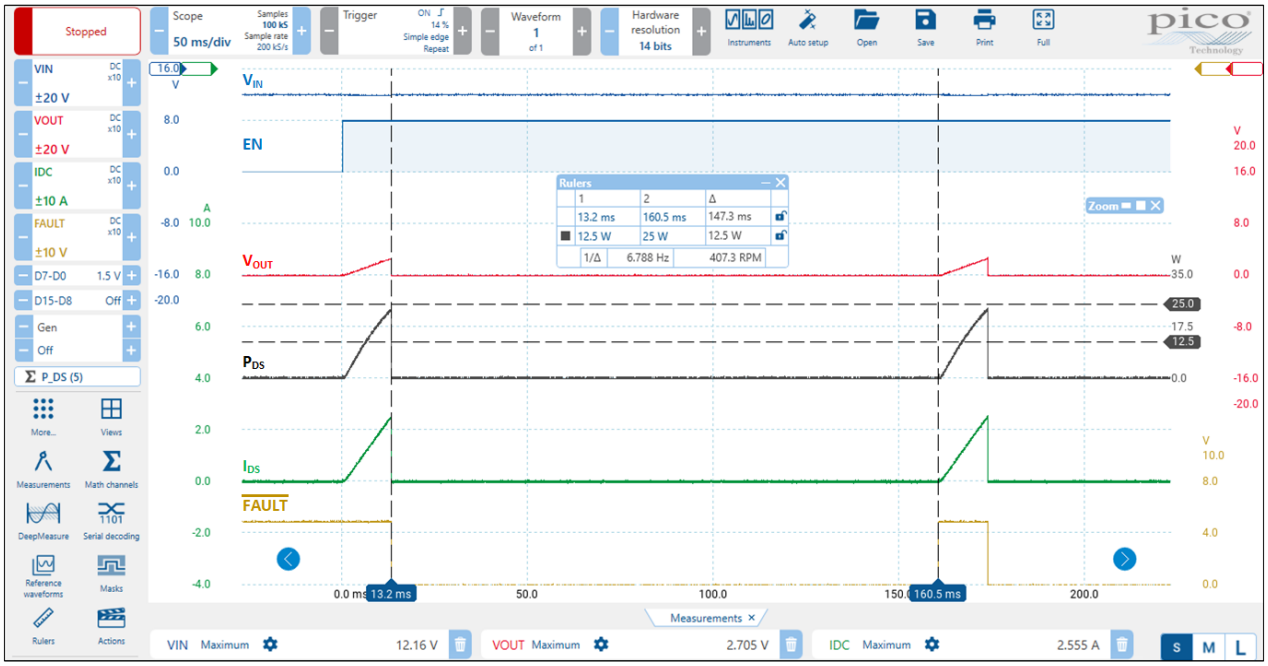

Figure 7: SLG59H1132V 25 W SOA operation waveform for V_{IN} = 12 V, ON = Low → High, C_{SLEW} = 150 nF, R_{SET} = 14 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = 1 Ω

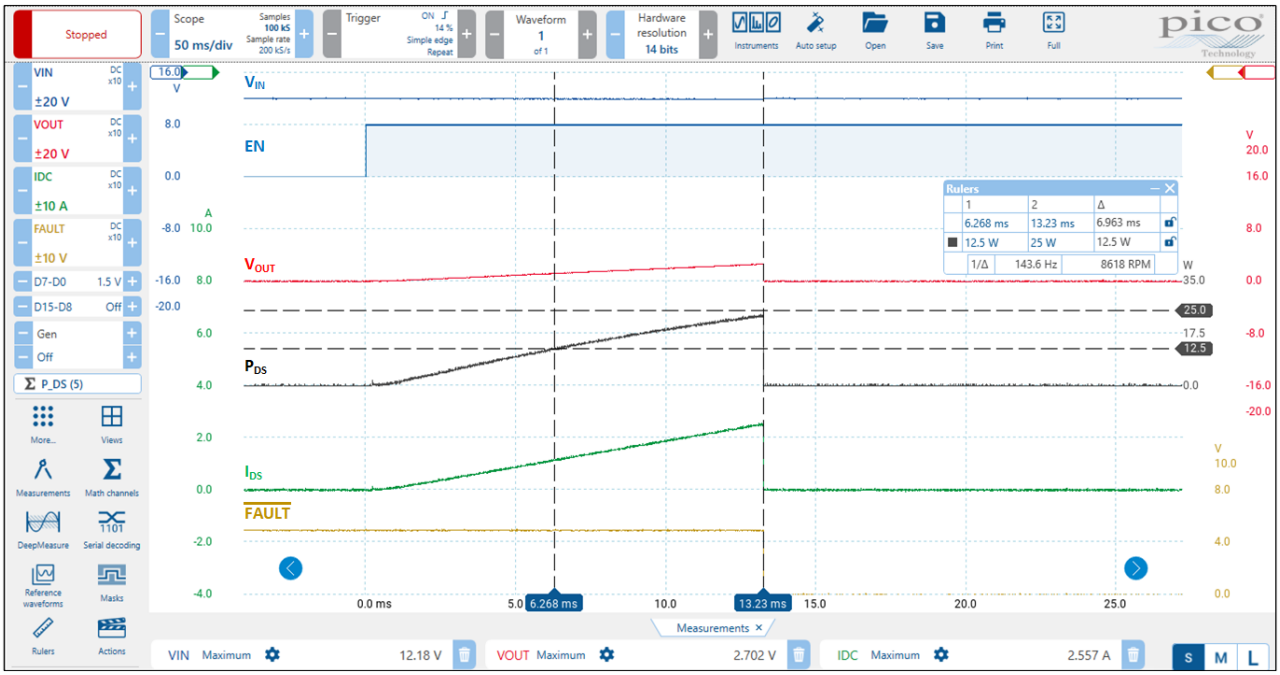

Figure 8: SLG59H1132V 25 W SOA operating waveform for V_{IN} = 12 V, ON = Low → High, C_{SLEW} = 150 nF, R_{SET} = 14 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = 1 Ω (Extended view)

The second level of SOA protection triggers an 18 ms delay, called a blanking time, after the power dissipation exceeds the threshold of 12.5 W. If the power dissipation is still greater than 12.5 W at the end of this blanking time, the device is turned off as shown in Figure 10. This helps to turn on the chip at high load and at the same time protects the FET from overloading and overheating. Similarly to the first case, a 160 ms auto-retry delay is also presented and shown in Figure 9.

Figure 9: 12.5 W SOA operating waveform for SLG59H1132V for V_{IN} = 12 V, ON = Low → High, C_{SLEW} = 150 nF, R_{SET} = 14 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = 2 Ω

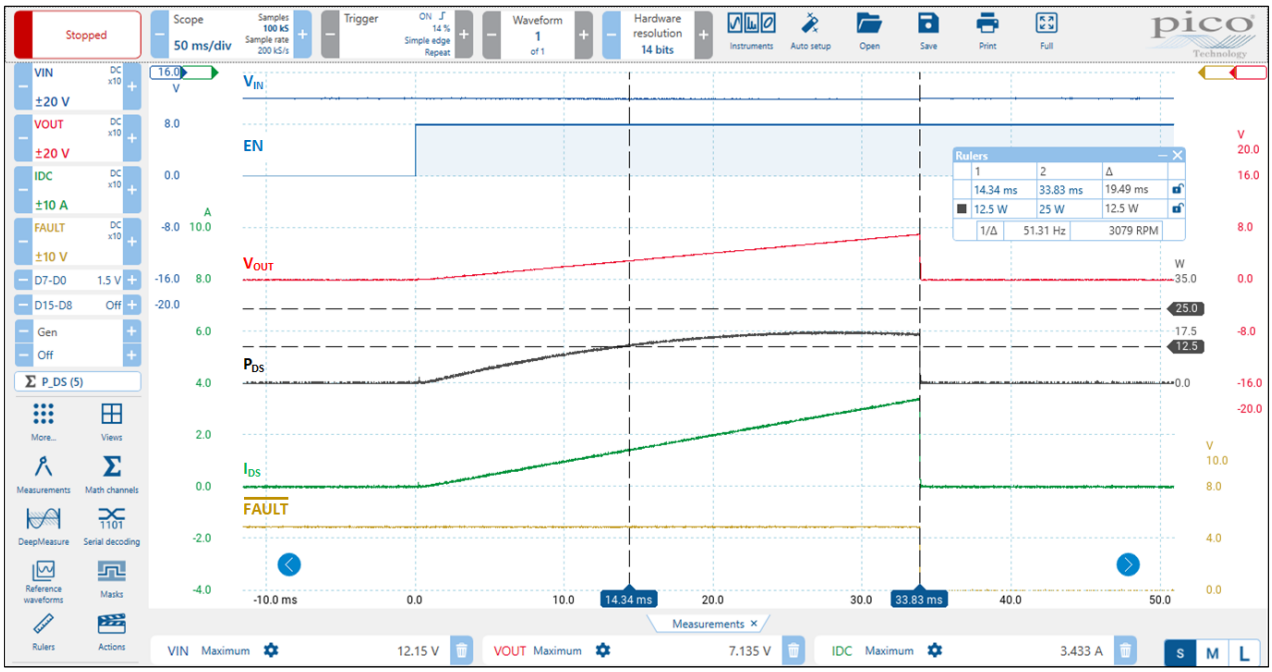

Figure 10: SLG59H1132V 12.5 W SOA operating waveform for V_{IN} = 12 V, ON = Low → High, C_{SLEW} = 150 nF, R_{SET} = 14 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = 2 Ω (Extended view)

Additionally, SOA protection works not only during power-up but also continuously monitors the power dissipation during the normal operation of the Renesas SLG59H1132V. This means that in case of reaching a current limit, SOA protection will turn off the device according to the principle described previously. SOA operation timing diagrams during a current limit event are illustrated in Figure 11 and Figure 12 while operational scopeshots are presented in Figure 13 - Figure 16. Thus, the Renesas SLG59H1132V is constantly self-protected against overpowering to provide high device reliability.

To calculate the power dissipation on the power MOSFET during current limit operation, use the equation below.

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS}$$

where:

- PD_{TOTAL} = Total package power dissipation, in Watts (W)
- V_{IN} = Voltage on the VIN pin (V)
- V_{OUT} = Voltage on the VOUT pin (V)
- I_{DS} = Output current, in Amps (A)

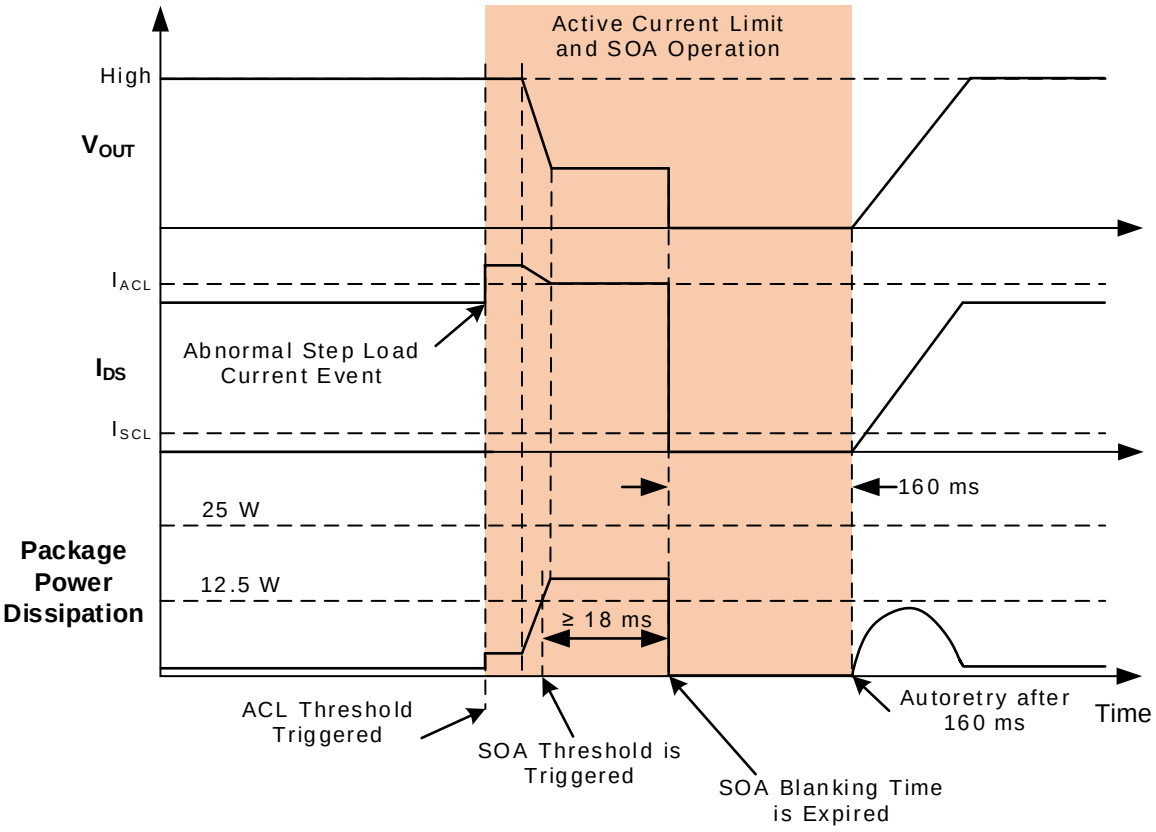

Figure 11: 12.5 W SOA operating diagram during Active Current Limit

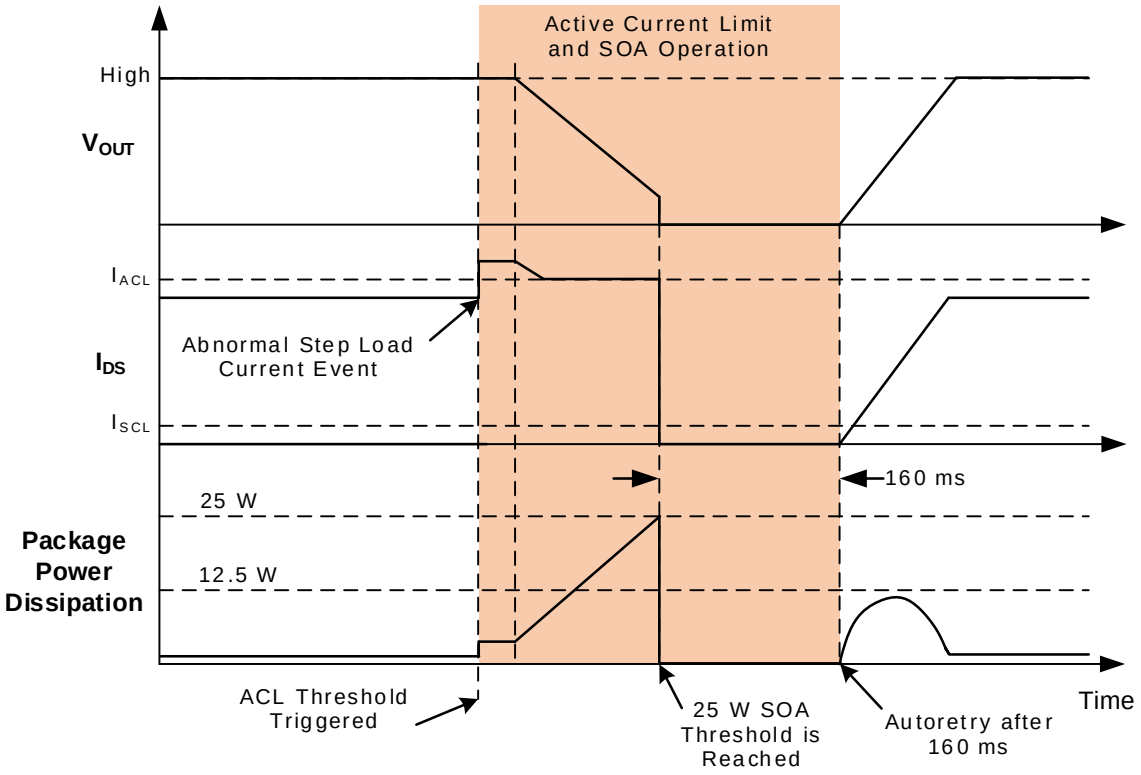

Figure 12: 25 W SOA operating diagram during Active Current Limit

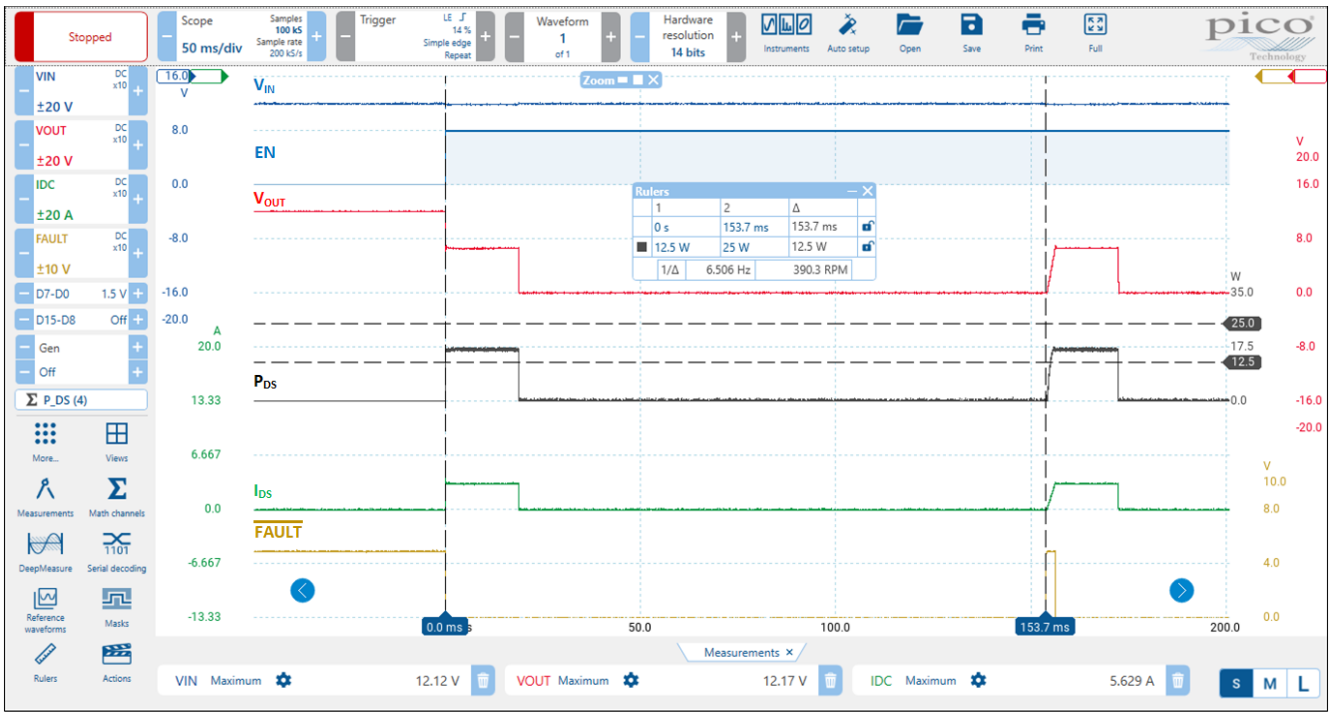

Figure 13: SLG59H1132V 12.5 W SOA operating waveform during Active Current Limit for V_{IN} = 12 V, C_{SLEW} = 10 nF, R_{SET} = 30.1 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = switch in 2 Ω

Figure 14: SLG59H1132V 12.5 W SOA operating waveform during Active Current Limit for V_{IN} = 12 V, C_{SLEW} = 10 nF, R_{SET} = 30.1 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = switch in 2 Ω (Extended view)

Figure 15: SLG59H1132V 25 W SOA operating waveform during Active Current Limit for V_{IN} = 12 V, C_{SLEW} = 10 nF, R_{SET} = 30.1 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = switch in 1 Ω

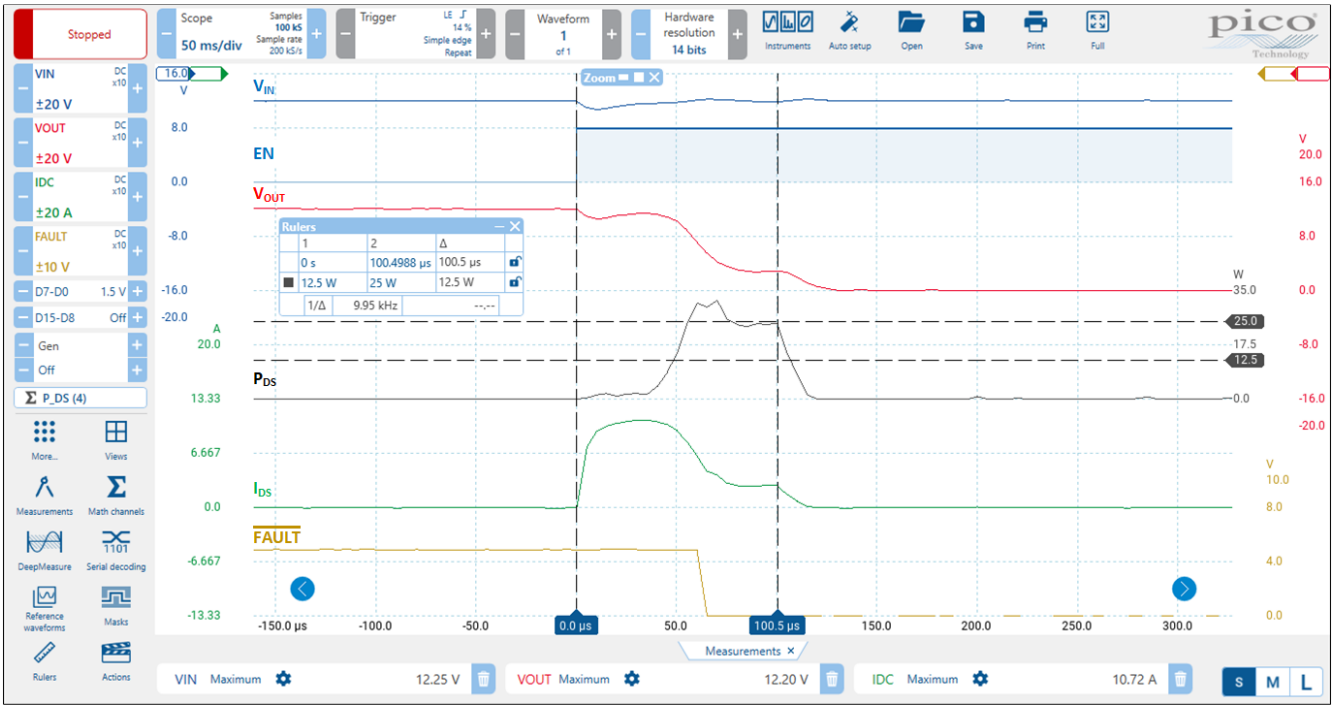

Figure 16: SLG59H1132V 25 W SOA operating waveform during Active Current Limit for V_{IN} = 12 V, C_{SLEW} = 10 nF, R_{SET} = 30.1 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = switch in 1 Ω (Extended view)

5.3 Using SLG59H1132V in High Load Applications

The SLG59H1132V is designed to be suitable for high-voltage and high-current power control applications, especially for power-up on heavy loads. To ensure that the load doesn't trigger the SOA protection, it is necessary to follow the recommendations from the table below for proper Slew Rate settings for particular C_{LOAD} and R_{LOAD} values.

V_{IN} [V]	Slew Rate [V/ms]	C_{SLEW} [nF]	C_{LOAD} [µF]	R_{LOAD} [Ω]
12	0.2	150	3300	6.2
	0.5	66	300	2
	1	33	500	2
	2	18	250	2
	3	10	160	2
	4	8.2	120	2
	5	6.8	100	2
24	0.5	66	500	12
	1	33	250	8
	1.5	22	160	8
	2	18	120	8
	2.5	13	100	8

5.3.1. Application Example

5.3.1.1. Power-up on Heavy Resistive Load

A typical application scheme using Renesas' SLG59H1132V in a real application which needs to power-up for V_{IN} = 12 V, R_{LOAD} = 2 Ω, C_{LOAD} = 10 µF and 4 ms rise time is shown in Figure 17.

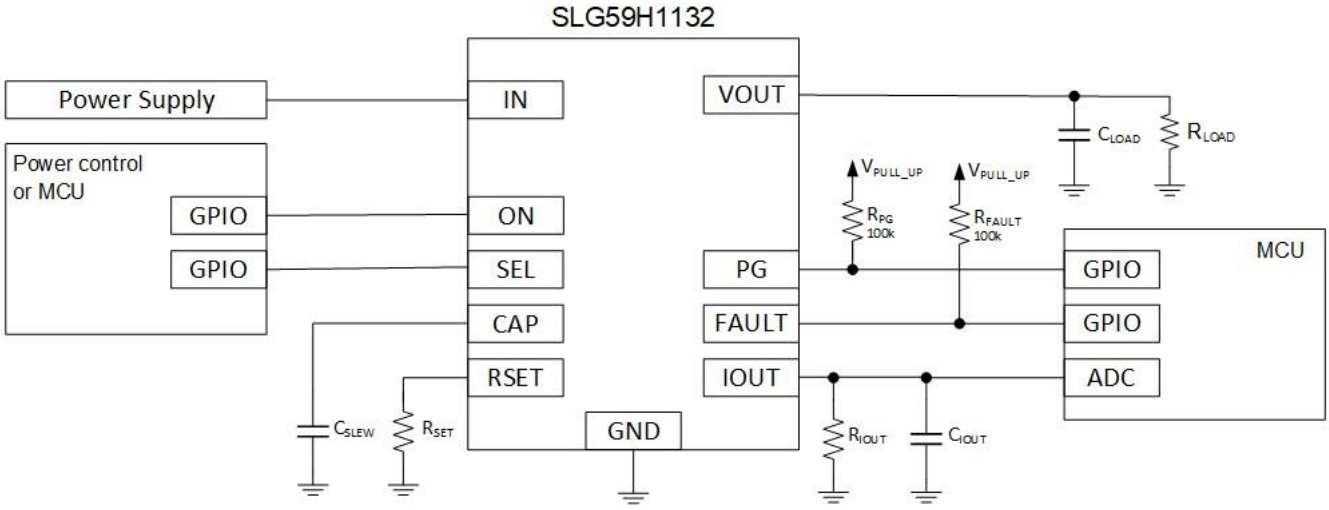

Figure 17: SLG59H1132V Application schematic

To meet the 4 ms rise time, the C_{SLEW} capacitor should be calculated using following equation:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 4.9\ \mu A \times \frac{20}{3}$$

$$C_{SLEW} = \frac{4}{12} \times 4.9\ \mu A \times \frac{20}{3} = 10.8\ nF \approx 10\ nF$$

Where:

- T_{RISE} = Total rise time from 10% V_{OUT} to 90% V_{OUT} (ms)
- V_{IN} = Input Voltage (V)
- C_{SLEW} = Capacitor value on CAP pin (nF)

Then, calculate the inrush current to ensure that this current does not exceed the maximum current that the power supply can handle and use equation below:

$$I_{INRUSH} = \frac{dV_{OUT}}{dt} \times C_{LOAD}$$

$$I_{INRUSH} = \frac{12 \times 0.8}{4\ ms} \times 10\ \mu F = 30\ mA$$

- where
  I_{INRUSH} = inrush current (A)
- C_{LOAD} = Total load capacitance connected to VOUT pin (F)
- dV_{OUT}/dt = the V_{OUT} voltage slew rate, calculated as 80% of V_{IN} divided by the desired T_{RISE}, in Volts/ms (V/ms)

Using equations from section 4.3 calculate relative coefficient k and max power dissipation:

$$k = \frac{V_{IN} - I_{INRUSH} \times R_{LOAD}}{2 \times V_{OUT(SR)}} = \frac{12 - 0.03 \times 2}{2 \times \frac{12 \times 0.8}{4}} = 1.875$$

$$PD_{MAX} = \frac{(I_{INRUSH} \times R_{LOAD} + V_{IN})^2}{4 \times R_{LOAD}} = \frac{(0.03 \times 2 + 12)^2}{4 \times 2} = 18.18\ W$$

Based on the calculations above, the 25 W SOA threshold shouldn't be triggered. The turn-on and off operation waveforms for this application are shown in Figure 18 and Figure 19.

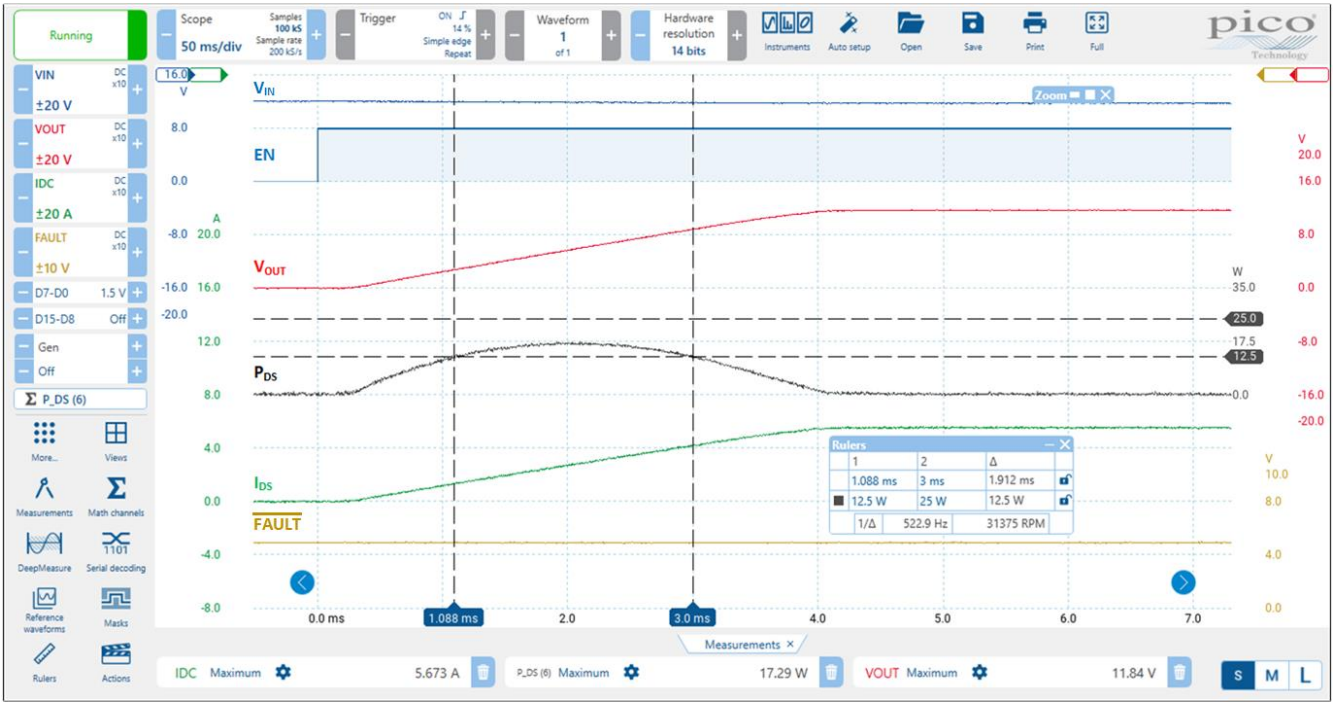

Figure 18. Turn-on operation waveform for V_{IN} = 12 V, C_{SLEW} = 10 nF, R_{SET} = 14 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = 2 Ω

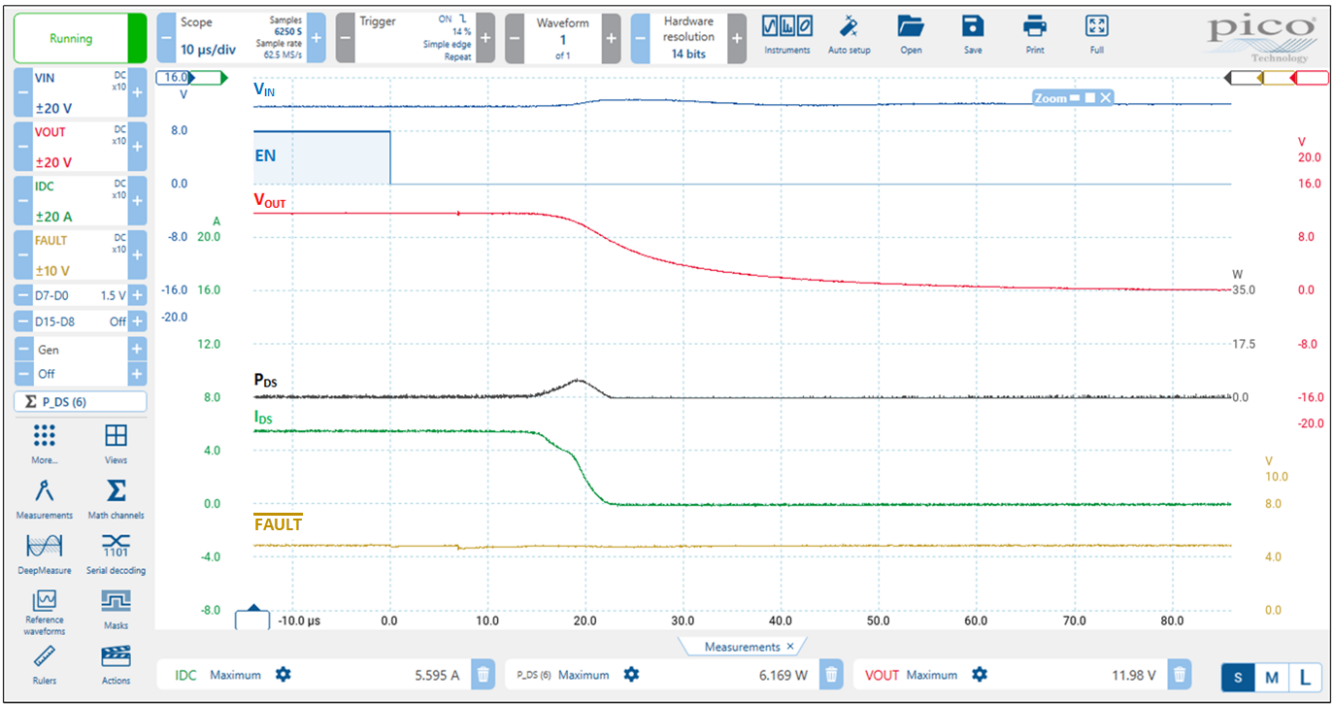

Figure 19. Turn-off operation waveform for V_{IN} = 12 V, C_{SLEW} = 10 nF, R_{SET} = 14 kΩ, C_{LOAD} = 10 µF, R_{LOAD} = 2 Ω

5.3.1.2. Power up on a heavy capacitive load

An application example using Renesas' SLG59H1132V in a heavy capacitive load situation with the following conditions: V_{IN} = 12 V, R_{LOAD} = 10 Ω, C_{LOAD} = 600 µF and 4 ms rise time, is provided. The typical scheme remains the same as in Figure 17.

Calculations are made in the same way as in the previous example:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 4.9\ \mu A \times \frac{20}{3} = \frac{4}{12} \times 4.9\ \mu A \times \frac{20}{3} = 10.8\ nF \approx 10\ nF$$

$$I_{INRUSH} = \frac{dV_{OUT}}{dt} \times C_{LOAD} = \frac{12 \times 0.8}{4\ ms} \times 600\ \mu F = 1.44\ A$$

$$k = \frac{V_{IN} - I_{INRUSH} \times R_{LOAD}}{2 \times V_{OUT(SR)}} = \frac{12 - 1.44 \times 10}{2 \times \frac{12 \times 0.8}{4}} = -0.5$$

$$PD_{MAX} = I_{INRUSH} \times V_{IN} = 0.96 \times 12 = 17.28\ (W)$$

Since this application uses a heavy capacitive load, the maximum power dissipation will be at the very first moment and based on the calculations, a 25 W SOA threshold is not reached. However, because the V_{OUT} slew rate is not stable at the beginning of the V_{OUT} ramp, a higher inrush current can be observed and internal SOA protection can be triggered as shown in Figure 20.

Figure 20. Turn-on operation waveform for V_{IN} = 12 V, C_{SLEW} = 10 nF, R_{SET} = 14 kΩ, C_{LOAD} = 600 µF, R_{LOAD} = 10 Ω

In this case it is recommended to increase the V_{OUT} rise time by increasing the slew rate capacitor (C_{SLEW}) and repeating the calculations again. It is recommended to change the rise time (T_{RISE}) to 6 ms in our application:

$$C_{SLEW} = \frac{6}{12} \times 4.9\ \mu A \times \frac{20}{3} = 16.33 nF \approx 16\ nF$$

$$I_{INRUSH} = \frac{12 \times 0.8}{6\ ms} \times 600\ \mu F = 960\ mA$$

$$k = \frac{12 - 0.96 \times 10}{2 \times \frac{12 \times 0.8}{6}} = 0.75$$

$$PD_{MAX} = \frac{(0.96 \times 10 + 12)^2}{4 \times 10} = 11.66\ (W)$$

Due to the smaller slew rate, the maximum power dissipation is reduced, making it possible to turn on without reaching the 25 W SOA threshold as shown in Figure 21. Turn off operation waveforms for this application are shown in Figure 22.

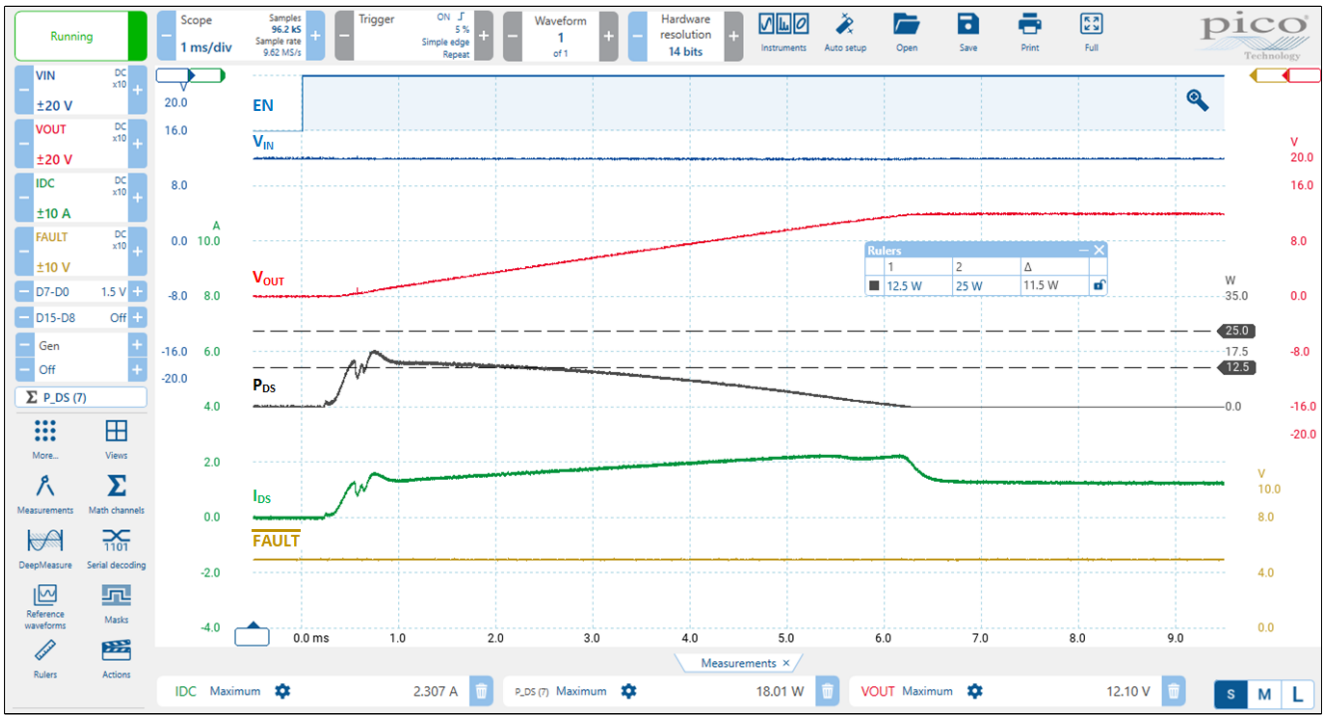

Figure 21. Turn-on operation waveform for V_{IN} = 12 V, C_{SLEW} = 16 nF, R_{SET} = 14 kΩ, C_{LOAD} = 600 µF, R_{LOAD} = 10 Ω

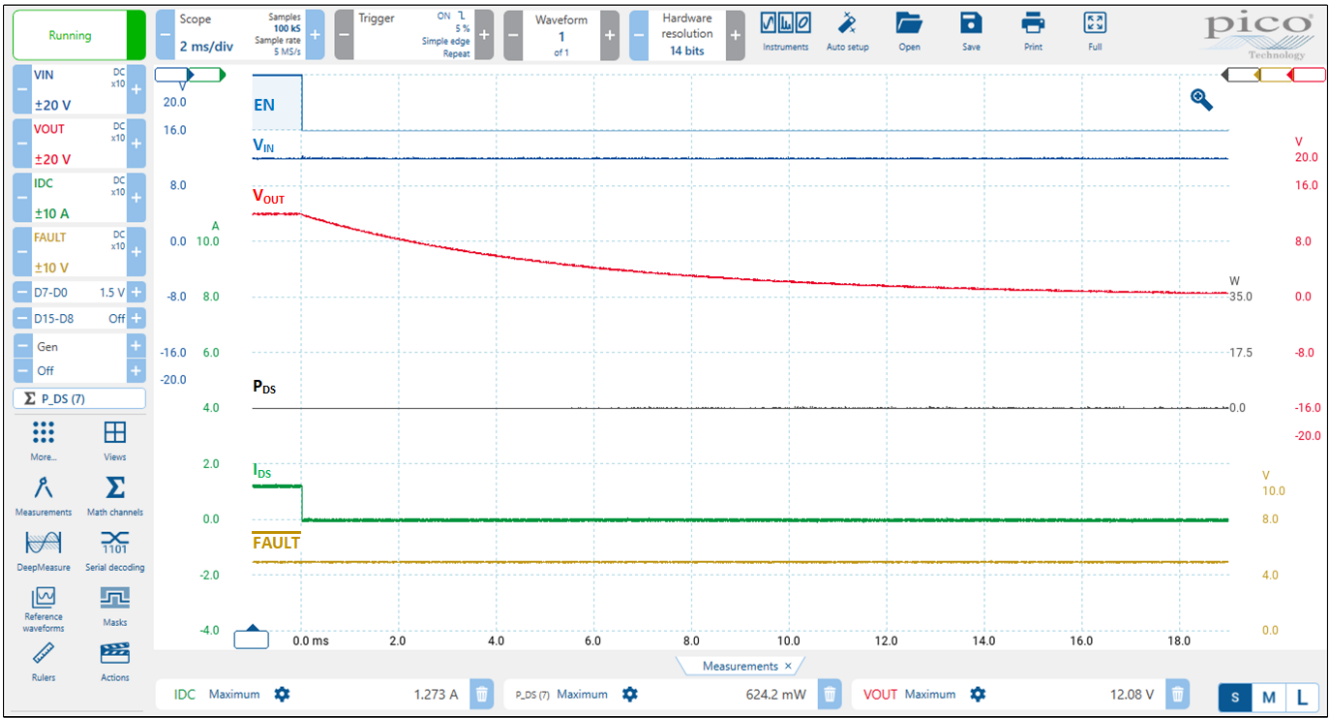

Figure 22. Turn-off operation waveform for V_{IN} = 12 V, C_{SLEW} = 16 nF, R_{SET} = 14 kΩ, C_{LOAD} = 600 µF, R_{LOAD} = 10 Ω

6. Conclusion

The Renesas SLG59H1132V is a highly reliable device with Safe Operating Area protection that significantly enhances overall device reliability, along with various other protection features such as current limit protection, short circuit protection, and more, making it suitable for high load applications such as telecommunications equipment, multi-function printers, and other similar devices.

7. Revision History

Revision	Date	Description
1.00	Sep 30, 2024	Initial release

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