12-bit ADC with Serial Output
SLG47011

This application note describes how to use the Renesas SLG47011 to implement 12-bit ADC with Serial Output. The application note comes complete with design files, which can be found in the References section.

Contents

References

For related documents and software, please visit:

AnalogPAK | Renesas

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-415 12-bit ADC with Serial Output.aap, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

Author: Ruslan Tykhovetskiy, Application Engineer, Renesas Electronics

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1. Introduction

In modern digital systems, ensuring high-quality analog signal conversion with a reliable and straightforward process for transmitting digitized data is essential. The use of serial data transmission is an excellent solution for systems that require fast and reliable data communication or cases where an I^2C interface is not available.

The SLG47011 from Renesas is well-suited for these tasks as it provides both analog signal digitization and serial output capabilities. Additionally, due to its extensive digital block resources, it enables the integration of additional functionality beyond standard analog signal conversion.

2. GreenPAK Design

Figure 1 shows the internal design of the ADC to serial output conversation in the Go Configure software Hub.

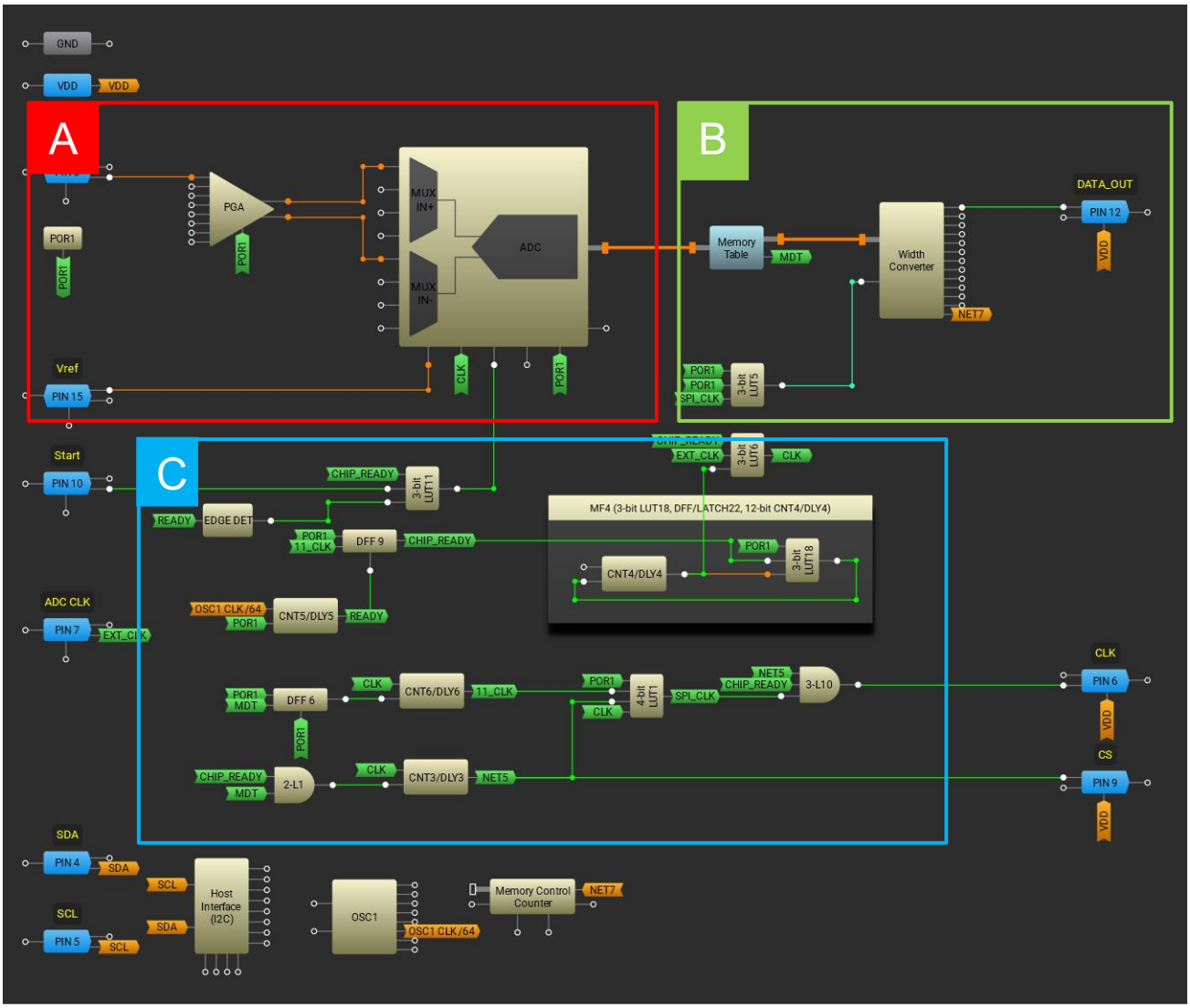

Figure 1. Design for converting an analog signal to a serial output

This design converts data from the ADC bus to a serial output and can transmit the data either continuously or word-by-word.

The design utilizes an external clock, a Vref, and a conversion start signal. If necessary, it can be easily modified to work with internal signals as well.

The design can be visually divided into the three following parts (A, B, and C) as pictured in Figure 2:

A: The ADC block, which performs the primary function of converting the analog input to a digital output.

B: The memory and bus conversion block that converts ADC digital output data into a serial output. The two key components are the Memory Table and the Width Converter, which will handle the serial data output. The Memory Table operates in `Addr to Data` mode, where the address is defined by the ADC output code. By default, the Memory Table is filled sequentially from 0 to 4095, so that each ADC value corresponds to a specific word in the table (Figure 2) (for example, if the ADC measures a value of 289, the memory table at that address will also store 289). However, these values can be rewritten to output specific data based on the input voltage. Once the Memory Table receives the word address from the ADC, it generates a data ready signal, prompting the Width Converter to start serial data transmission.

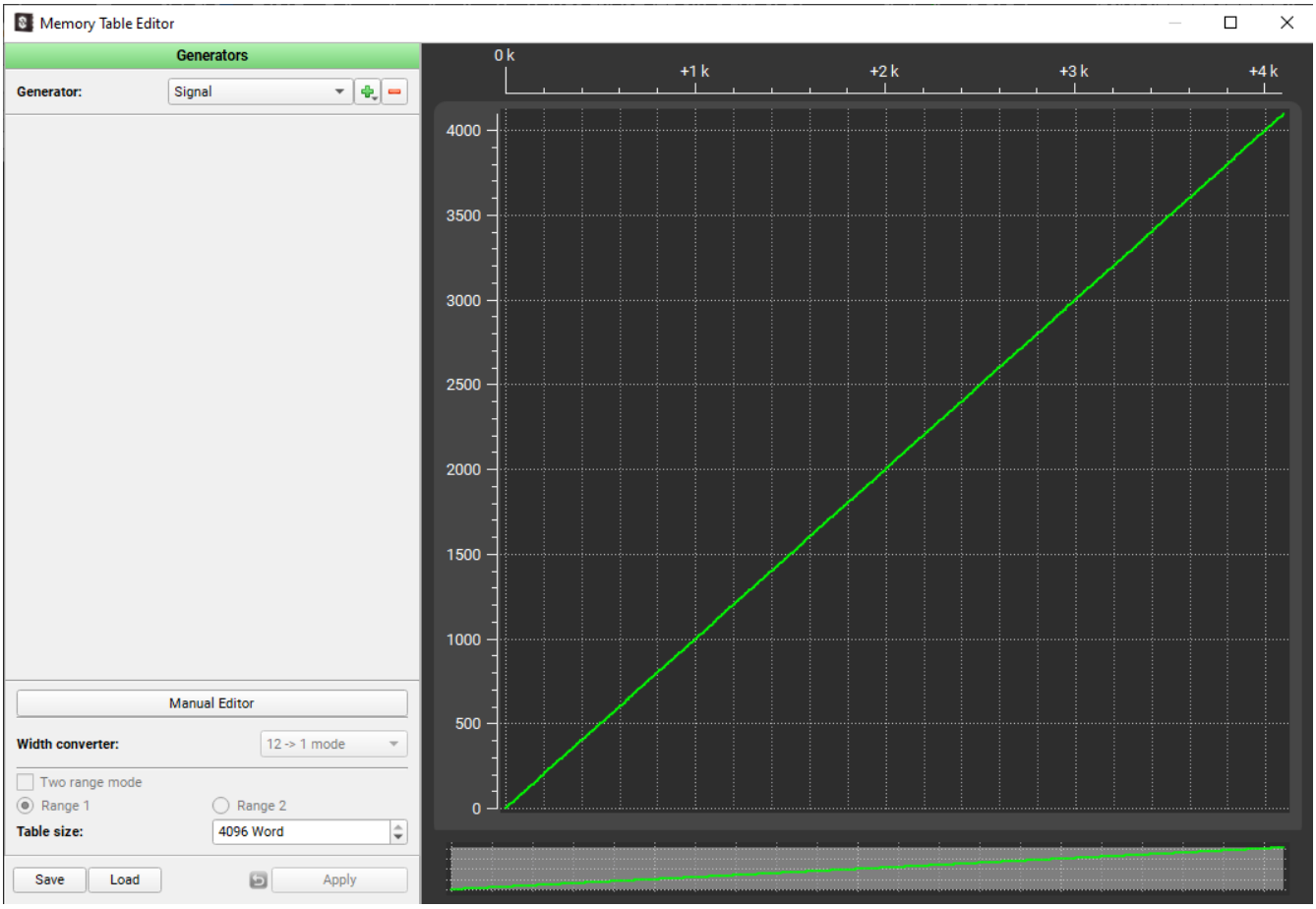

Figure 2. Memory Table Data

C: The most critical block of the system, responsible for the proper operation and synchronization of blocks A and B. Its operation can be described as follows:

- After powering on, the ADC must first be calibrated. This process is complete when the ADC Data Ready signal is generated.
- The next step is to synchronize blocks A and B. The first value is internally processed by the Width Converter without being output externally. This step is necessary to skip the initial twelve clock cycles during which the Width Converter outputs zeros, as it functions as a shift register.
- Once this process is complete, the system is now ready for operation.

It is crucial to properly skip the initial 12 clock cycles of the Width Converter as failing to do so will result in incorrect data output. The internal clock is only used during the synchronization process of blocks A and B; in all other cases, an external clock is utilized.

2.1 Design using an Internal Vref and CLK

The design below features an internal clock and a reference voltage (Vref). The architecture of the blocks and the operating principle are identical to the previous design, except for an additional block ‘D’, which generates the clock frequency after ADC calibration is completed to ensure synchronization and proper operation of all internal blocks.

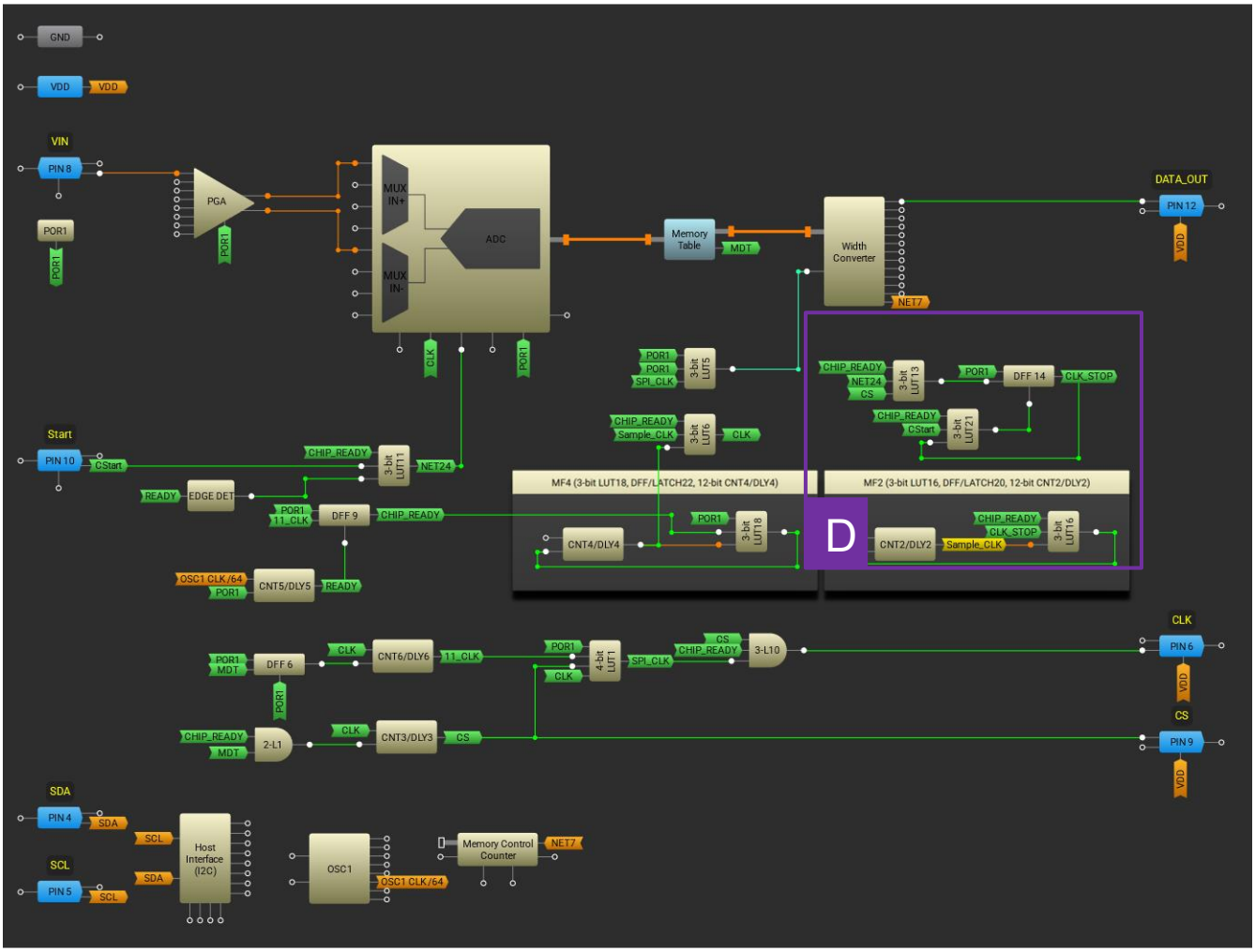

Figure 3. Design for internal CLK and Vref

The sample rate depends on CNT/DLY2 and is easily adjusted. It is calculated as follows:

$$\mathrm{SPS} = \frac{\mathrm{OSC}}{2 \times (\mathrm{CD} + 1) \times \mathrm{ADC}_{\mathrm{DEV}} \times (28 + \mathrm{DC})}$$

Where:

CD = DLY2 Counter data

ADC_DEV = Clock divider in ADC

DC = Delay between channels

It is important to note that, as with this design and the previous one, the delay between channels cannot be universal for all projects and must be adjusted specifically for each project.

3. Results

Figure 4 shows the design in continuous mode. The mode of operation depends on the state of PIN 10 (Start). As long as PIN 10 (Start) is high, the ADC will digitize the data.

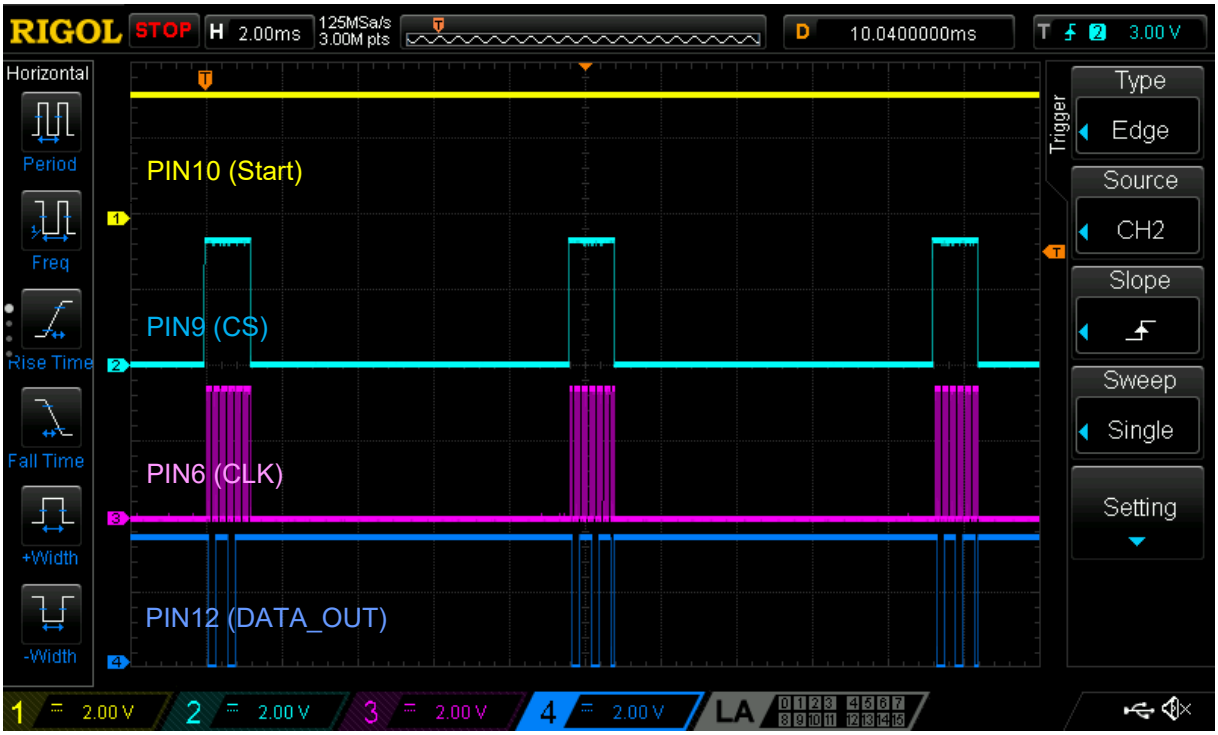

Figure 4. Continuous digitization

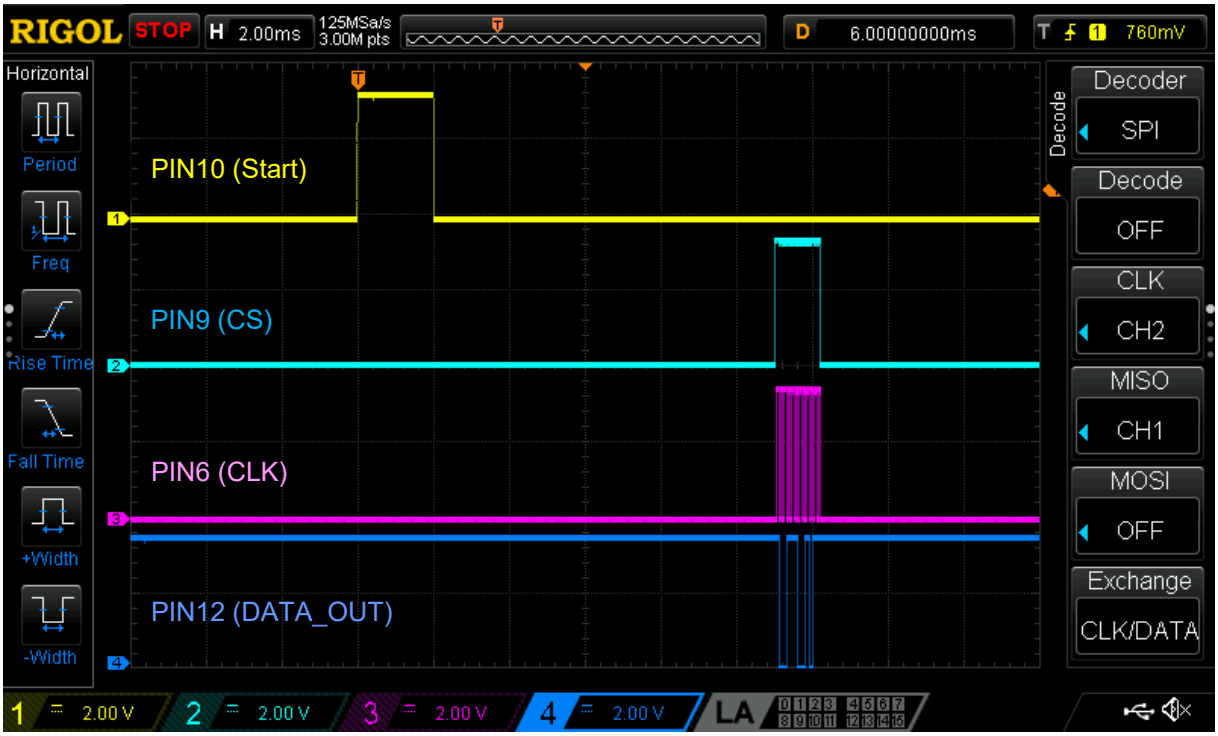

Figure 5. Single digitization

If a pulse shorter than the conversion period is applied to PIN 10 (Start), but no less than one clock cycle, then the chip will accordingly output data for only one value (as shown in Figure 5). By adjusting the duration in which PIN 10 remains high, the number of values output by the chip can be controlled.

There will be a delay between each data point or between the signal on PIN 10 and the ready data, which happens because the ADC digitizes the data during this period. To verify the functionality of the design, a setup with Data Buffer0 connected to the ADC is used, from which values were read via I²C (Figure 7) for comparison with the serial data output. The entire design is tested on the **Advanced Development Board**.

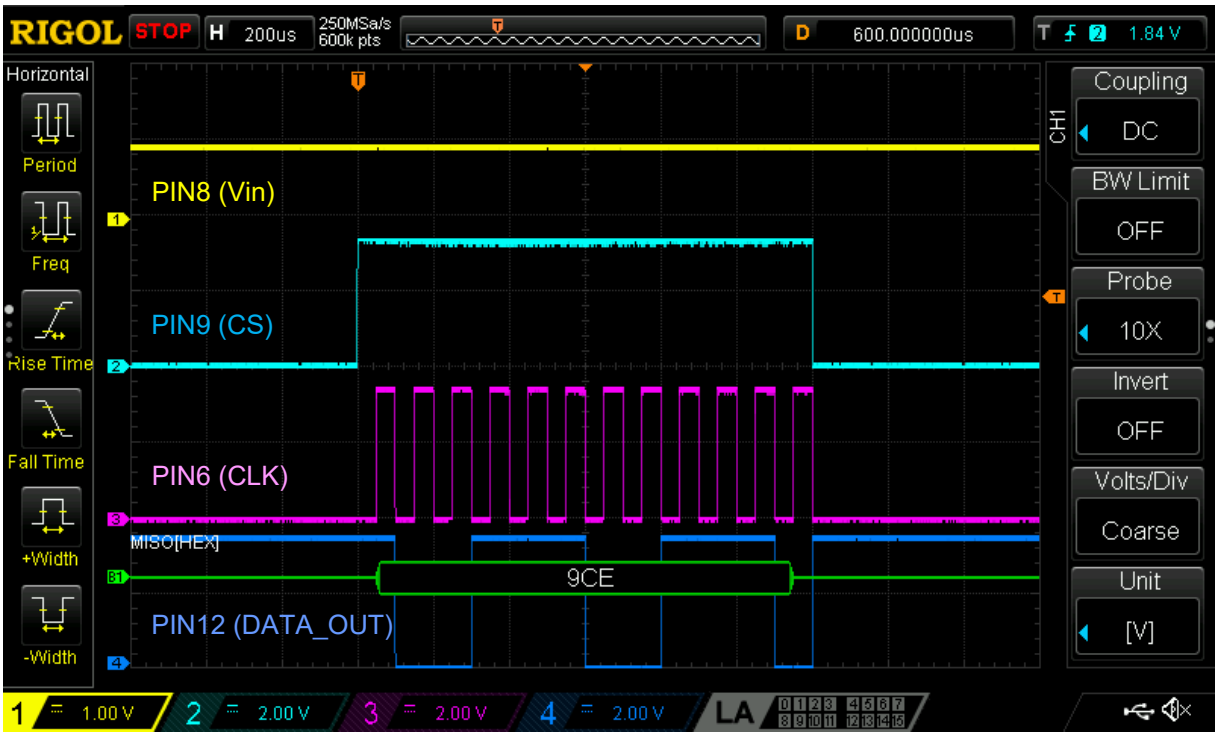

Figure 6. Example of data output

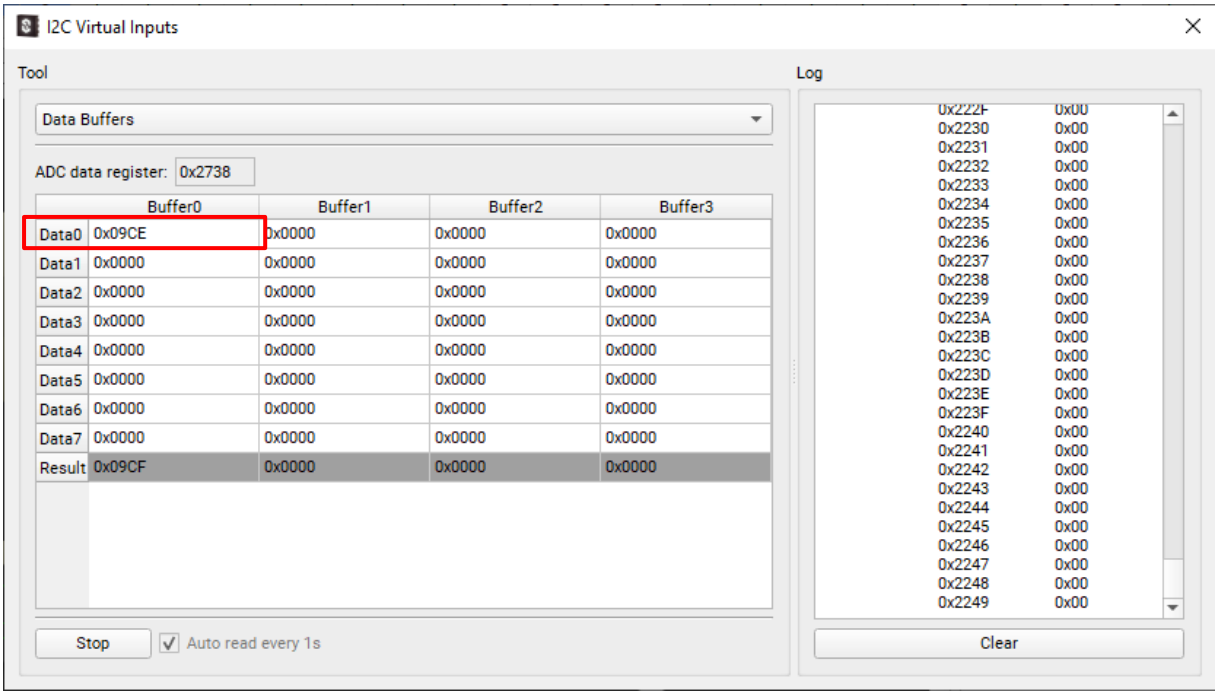

Figure 7. Data from ADC

Figure 6 and Figure 7 show the consistency of the output data.

4. Conclusion

The presented design provides an efficient solution for converting analog data to a serial output. By leveraging an external clock and modular architecture, it ensures flexibility, reliability, and accuracy in data transmission. The presence of programmable memory allows for easy adaptation to specific user requirements, making it a versatile tool for various tasks in digital systems.

5. Revision History

Revision	Date	Description
1.00	June 27, 2025	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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