Multi-channel Sampling Analog Comparator
SLG47003

This Application Note provides step-by-step recommendations for using the multi-channel sampling analog comparator (MS-ACMP) within the Renesas SLG47003. This project utilizes a combination of analog and digital components, creating a precise and flexible system for monitoring input signals and generating digital outputs based on specified threshold levels. The system monitors three voltage levels and detects when any of these levels fall outside of their allowable window, ensuring reliable operation and accurate signal management.

Design files for reproducing and configuring this system are available in the Reference section.

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1. Terms and Definitions

CH	Channel
CNT/DLY	The Counter/Delay
I^2C	Inter-integrated circuit (bus)
LUT	Look-up Table
MS ACMP	Multichannel Sampling Analog Comparator
OSC	Oscillator
V_{ref}	Voltage reference

2. References

For related documents and software, please visit:
AnalogPAK | Renesas
Download our free GreenPAK Designer software [1] to open the .app files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.
[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics
[2] AN-CM-416 Multi-channel Sampling Analog Comparator.aap, Design file, Renesas Electronics
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics
[4] Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics
[5] SLG47003 Datasheet, Renesas Electronics

Author: Viktor Levchenko, Product Development Engineer, Renesas Electronics

3. Introduction

This design implements a multiplexed analog comparator (MS ACMP) with support for multiple input signal channels. It monitors three voltage levels with typical values of 3.3 V, 2.5 V, and 1.8 V and generates an output signal if the input voltage is within the acceptable range. Each channel has a unique trigger threshold defined as a fraction of the selected reference voltage of 2.016 V. The system uses an internal V_{REF} generator and internal ACMP (gain control) channel dividers to provide accurate and reliable threshold levels. Output signals are generated based on the input signal levels relative to these thresholds.

4. The main characteristics of the MS-ACMP

The SLG47001/03 has one multi-channel sampling analog comparator (MS-ACMP) that can take periodic samples from up to six input channels and latches the results at the six outputs (Figure 2). The available inputs for the MS-ACMP consist of the following: GPIO0, GPIO1, GPIO2, GPIO3, OA0_OUT, OA1_OUT, RH1A, RH1B, TS_OUT, or VDD. GPIO8 and GPIO9 are also available in STQFN-24 package option. Users can select from one to six channels to be sampled (for example, Channel0, Channel1, and Channel2).

The channels are sampled in fixed order from Channel0 to Channel5. Each channel has an individual voltage reference with programmable low-to-high and high-to-low thresholds. The V_{REF} voltage ranges from 32 mV to 2016 mV with 32 mV steps, and each channel has two separate registers, 6-bit for the low-to-high V_{REF} threshold and another 6-bits for the high-to-low V_{REF} threshold selection. The non-inverting input of the MS-ACMP has a voltage divider (Gain of 1, 1/2, 1/3, and 1/4) that can configure the gain of each channel individually.

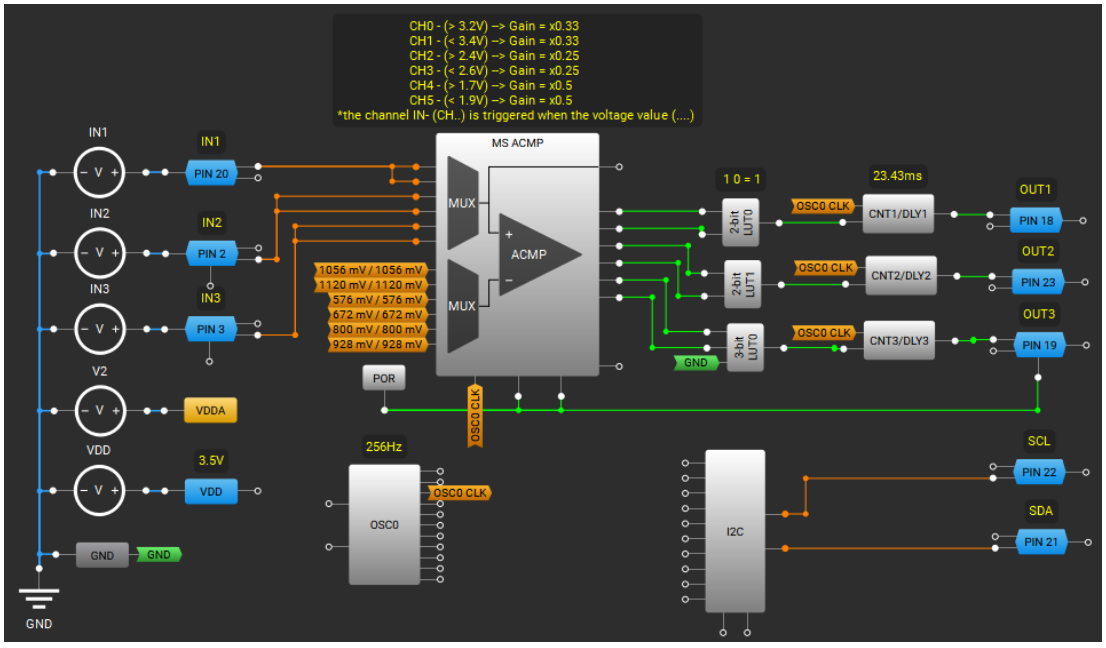

Figure 1. MS-ACMP design block diagram

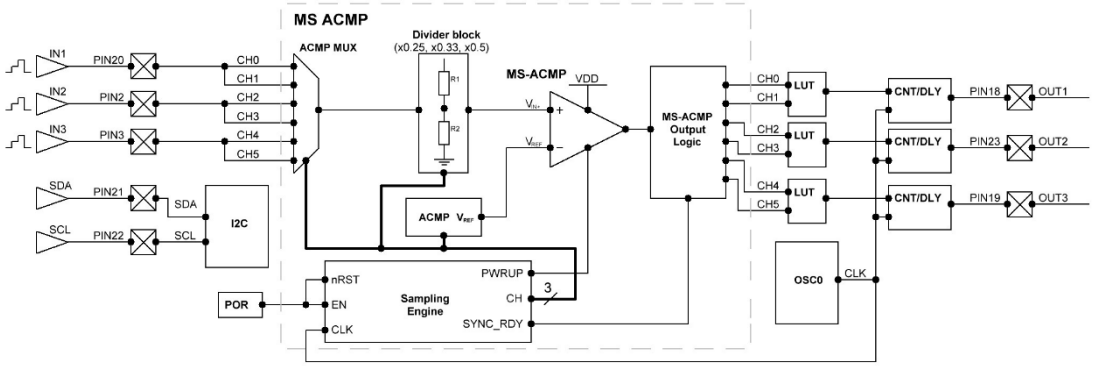

Figure 2. MS-ACMP typical application circuit

The MS-ACMP uses the internal oscillator (OSC0) or an external clock (max. 10 kHz with 50% duty cycle) to switch between channels, change V_{REF}, and latch the results. The clock from OSC0 can be divided by 2, 4, or 8 within the MS-ACMP. If the 'Auto Power-on' setting of OSC0 is selected, a HIGH-level voltage (or a rising edge depending on the setting) on the EN input starts the internal oscillator (OSC0). Table 1 shows the recommended MS-ACMP clock frequencies when interfacing sensors with high output impedance.

Table 1: Recommended MS-ACMP Clock Frequencies

Parameter	Range 1	Range 2	Range 3	Range 4	Range 5	Unit
Sensor Output Resistance	< 1	1 to 2	2 to4	2 to 6	> 6	MΩ
MS-ACMP Clock Frequency	≤ 10	≤ 5	≤ 2.5	≤ 1.25	≤ 0.5	kHz

The outputs of the MS-ACMP can be configured to be either asynchronous or synchronous.

- In asynchronous mode (ACMP_SYNC_MODE = 0), the results appear continuously after each channel is sampled.
- In synchronous mode (ACMP_SYNC_MODE = 1), the results at the output appear simultaneously after the last selected channel is sampled.

This design for the MS-ACMP uses sampling mode (ACMP_RNG_MODE = 0) with Level-sensitive Detection (ACMP_DET_MODE = 0). In this mode, the MS-ACMP switches between up to six sampled channels and latches the result every pulse at the CLK input while the EN input is high. When the EN signal goes low, the MS-ACMP finishes the sampling sequence and enters power-down mode.

5. Design Operation

5.1 MS-ACMP Settings

VDD input: Disable (default)
Temp Sensor input: Disable (default)
Force bandgap on: Enable (default)
Output nReset: Connected to POR
Hysteresis: Hysteresis options for each channel are disabled (0 mV).
IN+ Gain: For channel CH0, CH1 – x0.33; For channel CH2, CH3 – x0.25; For channel CH4, CH5 – x0.5.

5.2 Connections:

IN+ CH0: Non-inverting analog input source terminal of Channel 0. (GPIO8)
IN+ CH1: Non-inverting analog input source terminal of Channel 1. (GPIO8)
IN+ CH2: Non-inverting analog input source terminal of Channel 2. (GPIO1)
IN+ CH3: Non-inverting analog input source terminal of Channel 3. (GPIO1)
IN+ CH4: Non-inverting analog input source terminal of Channel 4. (GPIO0)
IN+ CH5: Non-inverting analog input source terminal of Channel 5. (GPIO0)
IN- CH0: Inverting analog input source terminal of Channel 0. (1056 mV Vref)
IN- CH1: Inverting analog input source terminal of Channel 1. (1120 mV Vref)
IN- CH2: Inverting analog input source terminal of Channel 2. (576 mV Vref)
IN- CH3: Inverting analog input source terminal of Channel 3. (672 mV Vref)
IN- CH4: Inverting analog input source terminal of Channel 4. (800 mV Vref)
IN- CH5: Inverting analog input source terminal of Channel 5. (928 mV Vref)
CLK: Sampling clock source of MS ACMP. (Default – OSC0)
Enable: Connect Enable matrix input through a POR
nReset: Connect nReset matrix input through a POR
OUT CH0: Connect to IN1 (2-bit LUT0)
OUT CH1: Connect to IN0 (2-bit LUT0)
OUT CH2: Connect to IN1 (2-bit LUT1)
OUT CH3: Connect to IN0 (2-bit LUT1)
OUT CH4: Connect to IN2 (3-bit LUT0)
OUT CH5: Connect to IN1 (3-bit LUT0)

5.3 MS-ACMP Channel Configuration:

- IN- CH0: Threshold $V_{TH_0} \approx 3.26\ V$
- IN- CH1: Threshold $V_{TH_1} \approx 3.4\ V$
- IN- CH2: Threshold $V_{TH_2} \approx 2.39\ V$
- IN- CH3: Threshold $V_{TH_3} \approx 2.72\ V$
- IN- CH4: Threshold $V_{TH_4} \approx 1.72\ V$
- IN- CH5: Threshold $V_{TH_5} \approx 1.86\ V$

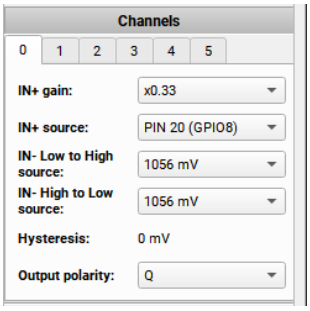

Figure 3. Channel Configuration

5.4 Operating Principle

5.4.1. Input Signal Multiplexing

- The analog multiplexer selects the input signal for comparison with the corresponding threshold.
- The signal on each input is checked using the comparator.

5.4.2. Comparison

The system utilizes two comparators to perform window comparison. The first comparator compares the input signal with the lower threshold value. If $V_{IN\_CH0} > V_{TH0}$, its digital output “MS ACMP OUT CH0” transitions to a “HIGH” state (logical 1). Similarly, the second comparator compares the input signal with the upper threshold. If $V_{IN\_CH1} > V_{TH1}$, the MS-ACMP’s digital output also transitions to a “HIGH” state (logical 1). Both digital outputs of the comparator are processed by a 2-bit LUT logic block, which generates the system's output signal. For example, as a result, the output signal is set to a high state only when the input voltage is within the specified range. For the OUT1 output, this range is 3.2 V to 3.4 V.

Otherwise, the MS ACMP output $OUT\ CH_i$ transitions to a “LOW” state (logical 0).

5.4.3. Signal Generation

Each $OUT\ CH_i$ output generates a signal that can be used for monitoring or control purposes. However, it is recommended to additionally add a CNT/DLY block at the output.

Delay blocks are used in the circuit to generate stable pulses at the output. In this case, the CNT/DLY block performs dual functions:

- **Stabilization of output signals.** The comparator analyzes input signals and determines when the voltage level exceeds a certain threshold. However, if the input signal is at the switching threshold, the CNT/DLY macrocell helps reduce the risk of false triggering by maintaining the signal state (high/low) for a set period before the next transition.
- **Glitch filtering.** Without the DLY block, the circuit may respond to short voltage spikes. Adding this block makes it possible to filter out short pulses that do not correspond to actual signal changes.

5.4.4. Synchronization

The **SYNC READY** signal indicates the completion of the multiplexing process and readiness for a new processing cycle

6. Design Software Simulation

6.1 Input Signals (IN1, IN2, IN3)

Input voltages vary over time across different ranges.

6.2 Digital Outputs (OUT CH0, OUT CH1, OUT CH2, OUT CH3, OUT CH4, OUT CH5)

Outputs switch to a "HIGH" state at points where $V_{IN\_CHi} > V_{THi}$. For example, OUT_CH0 is activated when $V_{IN\_CH0} > 3.26$ V, and OUT_CH1 is activated when when $V_{IN\_CH1} > 3.4$ V.

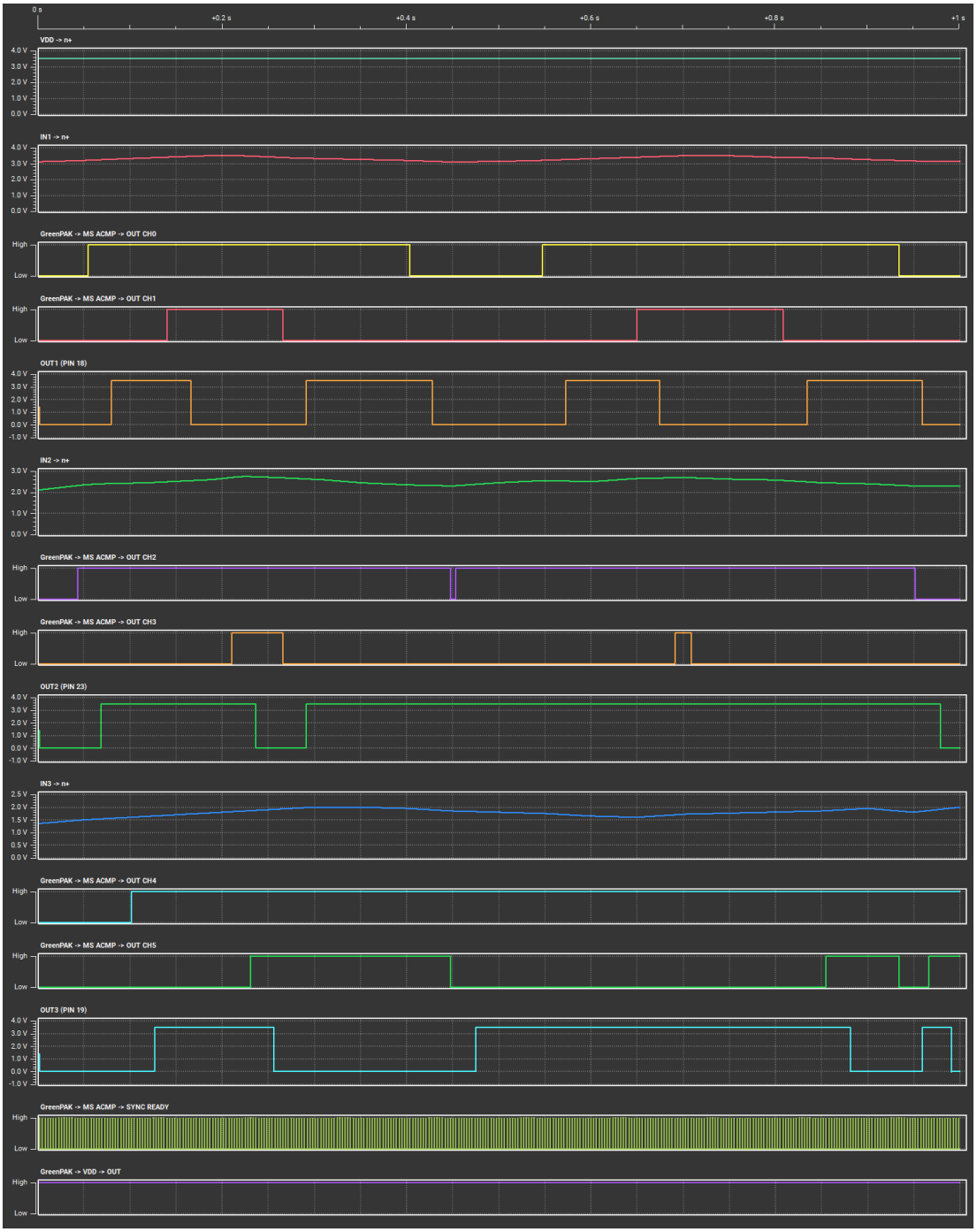

Figure 4. MS-ACMP Input/Output graphs

7. Conclusion

The application note describes how to implement an accurate six-channel analog comparator system for monitoring three voltage levels using the MS-ACMP of the Renesas SLG47003. Each voltage level is evaluated using precise thresholds, leveraging internal reference generators and configurable gain settings to ensure reliable operation even with variations in the supply voltage. This design offers flexibility and robustness for a wide range of voltage monitoring and control applications.

This application note is perfectly suited for:

- **Voltage Monitoring:** Monitoring battery or power supply status.
- **Protection Systems:** Triggering emergency scenarios in cases of overvoltage/undervoltage.
- **Automation:** Detecting events within specified voltage ranges.

8. Revision History

Revision	Date	Description
1.00	September 16, 2025	Initial release.