DA1459x Application Hardware Design Guidelines

This document provides the reference schematic of the DA1459x evaluation kit board, circuit explanation and design guidelines for Bluetooth® Low Energy applications based on the SoC of DA14592 and DA14594.

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1. Terms and Definitions

ADC	Analog-to-Digital Converter
BOD	Brown-Out Detection
CPU	Central Processing Unit
DCDC	DC/DC (buck) Converter
ENOB	Equivalent Number of Bits (ADC)
FCQFN	Flip Chip Quad Flat No-lead (chip package)
FPU	Floating Point Unit
GPADC	General Purpose ADC
GPIO	General Purpose Input Output
LDO	Low Dropout (voltage regulator)
LPF	Low Pass Filter (RF)
MAC	Media Access Controller
OSR	Over Sampling Rate (ADC)
OTP	One-Time Programmable (memory)
PCB	Printed Circuit Board
PDC	Power Domain Controller
PMU	Power Management Unit
POR	Power On Reset
PWM	Pulse Width Modulation
RDS	Reduced Drive Strength (GPIO)
RAM	Random-Access Memory
RF	Radio Frequency
SDK	Software Development Kit
SoC	System on Chip
QSPI	Quad Serial Peripheral Interface
SDADC	Sigma-Delta ADC
SINAD	Signal to Noise And Distortion ratio
SRAM	Static Random-Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transceiver
WLCSP	Wafer Level Chip Scale Package

2. References

[1] DA1459x Datasheet, Renesas Electronics.

[2] CE-BT-001 DA1459x Errata, Renesas Electronics.

[3] UM-B-167, DA1459x Hardware Pro-Development Kit, Manual, Renesas Electronics.

[4] AN-B-027, Designing Printed Antennas for Bluetooth, Application Note, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

The DA1459x SoC is a multi-core wireless microcontroller, combining the latest Arm® Cortex® M33™ application processor with floating-point unit, advanced power management functionality, a cryptographic security engine, analog and digital peripherals, a software configurable protocol engine with a radio that is compliant with Bluetooth® 5.2 Low Energy (DA14592) or Bluetooth® 5.3 Low Energy (DA14594) standard and has 256 kB of embedded Flash accompanied by 96 kB of SRAM.

The DA1459x SoC is based on an Arm® Cortex®-M33 CPU with an eight-region MPU and a single-precision FPU offering up to 96 dMIPS at 64 MHz. The dedicated application processor executes code from embedded Flash or RAM through an 8 kB four-way associative cache controller. Bluetooth® 5.2 Low Energy or other protocol connectivity is guaranteed by a new software-configurable Bluetooth® Low Energy protocol engine (MAC) based on an Arm® Cortex®-M0+™ with an ultra-low-power radio transceiver, capable of +6 dBm output power and -97 dBm sensitivity offering a total link budget of 103 dB.

A variety of standard and advanced peripherals enable interaction with other system components and the development of advanced user interfaces and feature-rich applications. See Ref. [1].

Table 1 shows the differentiation between the DA14592 product versions.

4. DA1459x Product Differentiation

Two packages for the DA14592 and DA14594 exist: WLCSP39 and FCQFN52. Figure 1 shows the ball and pin assignments of both packages and Table 1 shows the differences in features between both versions.

Table 2 shows the chip revisions, and these can be read from Chip_Revision_Reg (0x50050214) and Chip_Test1_Reg (0x500502F8).

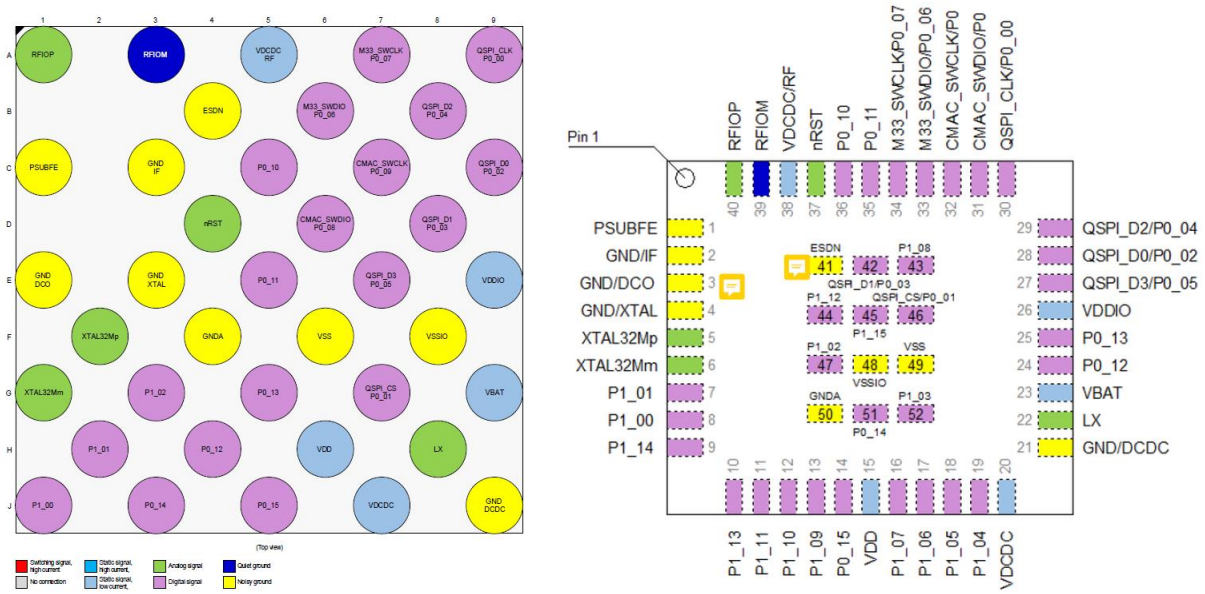

Figure 1. WLCSP39 and FCQFN52 outlines and pin locations

Table 1. DA1459x versions and features

Features	DA1459x WLCSP39	DA1459x FCQFN52
Number of balls or pins	39 balls	52 pins
Number of GPIOs	19	32 (30 when Xtal32K is used)
XTAL32K support	No, use internal RCX instead	Yes (Note 1)
SRAM	96 kB	96 kB
Cache RAM	16 kB	16 kB
Embedded Flash	256 kB	256 kB
QSPI RAM/Flash Controller	Yes	Yes
GP-ADC/SD-ADC inputs	4 and VBAT internally	8 and VBAT internally
SD-ADC ext. reference voltage	No support.	Supported.
Package size	3.32 mm x 2.48 mm	5.1 mm x 4.3 mm
Ball/Pin pitch	0.42 mm diagonal	0.4 mm

Note 1 Optional, XTAL32K pins P1_13 and P1_14 may also be used as GPIO.

Table 2. Chip revision numbering

Chip version	Chip_Revision (0x50050214)	Chip_Layout_Revision (0x500502F8)
DA14592 WLCSP39	0x41 (A)	0x45 (E)
DA14592 FCQFN52	0x41 (A)	0x45 (E)
DA14594 WLCSP39	0x41 (A)	0x47 (G)
DA14594 FCQFN52	0x41 (A)	0x47 (G)

5. Minimal Design for DA1459x SoC

The DA1459x SoC requires a minimum number of external components for proper operation. The necessary sections required for the minimal system operation are:

- Power section
- 32 MHz crystal oscillator
- Radio section
- JTAG interface
- UART interface
- Proper PCB routing

The minimal design for the DA1459x is shown in the evaluation kit schematics for the two packages, WLCSP39 and FCQFN52, Figure 2 and Figure 3 respectively.

The FCQFN52 schematic shows the 32.768 kHz crystal as optional. Pins P1_13 and P1_14 are shown for GPIO functionality. Resistors R12 and R14 in Figure 3 must be removed when using the XTAL32K oscillator.

The WLCSP39 version of the chip has no support for a 32.768 kHz crystal because of the limited number of P1 GPIOs.

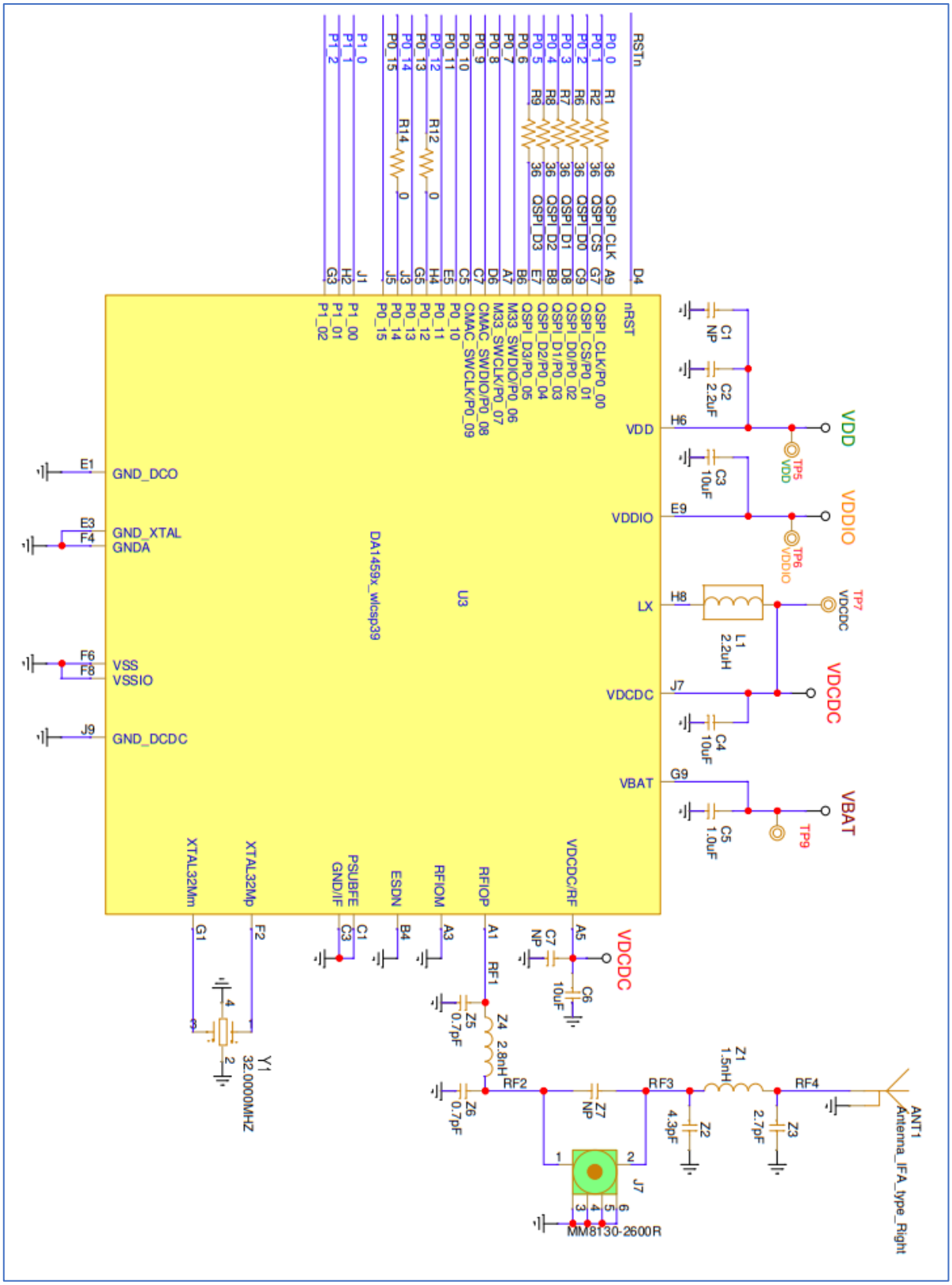

Figure 2. DA1459x WLCSP32 schematic

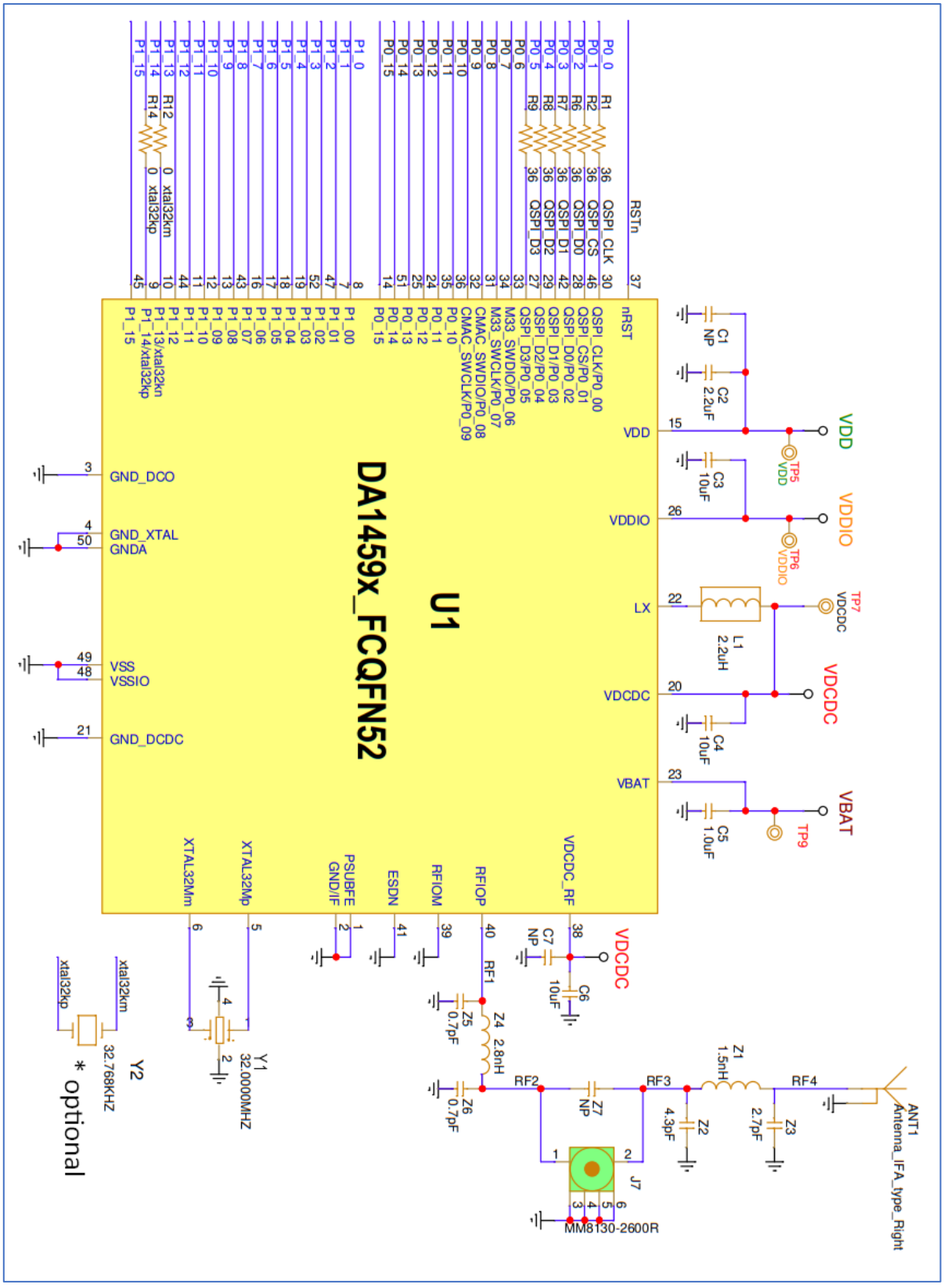

Figure 3. DA1459x FCQFN52 schematic

5.1 Power Section

The DA1459x SoC has a complete integrated Power Management Unit (PMU). This includes a buck DCDC converter, several LDOs for the different power rails of the system, and brownout detection:

- Synchronous Single Inductance Single Output Buck DCDC converter with a programmable output 1.1 V to 1.4 V.
- Capability of using the DCDC converter both in active as well as in Sleep modes.
- LDO that can be used instead of the DCDC in Active and Sleep mode: LDO_LOW/_RET.
- Active and retention LDO for the digital core: LDO_CORE/_RET.
- Active and retention LDO for the I/O-s having 20 mA or 2 mA current capability: LDO_IO/_RET
- Separate LDOs for the radio operation supporting High-Performance and Low-Power modes.
- Brownout detection on all internal voltage rails (Section 5.3).

There is one main power input, namely VBAT. The VBAT rail directly supplies several circuits like the DCDC Converter, the embedded Flash, the RCX oscillator, the Bandgap, two RC oscillators, the LDO_LOW which supplies the VDCDC rail when the DCDC is not active, and the LDO_IO which supplies the VDDIO rail. The VDD rail is powered by the LDO_CORE from the VDCDC rail.

The VDCDC rail also supplies the Radio LDOs, the ADC LDOs, the 32.768 kHz crystal oscillator and the LDO_XTAL which supplies the 32 MHz crystal oscillator and the Clock doubler.

At cold boot, the LDO_LOW is used to power the VDCDC rail. The DCDC can be enabled by the software, the LDO_LOW is disabled automatically.

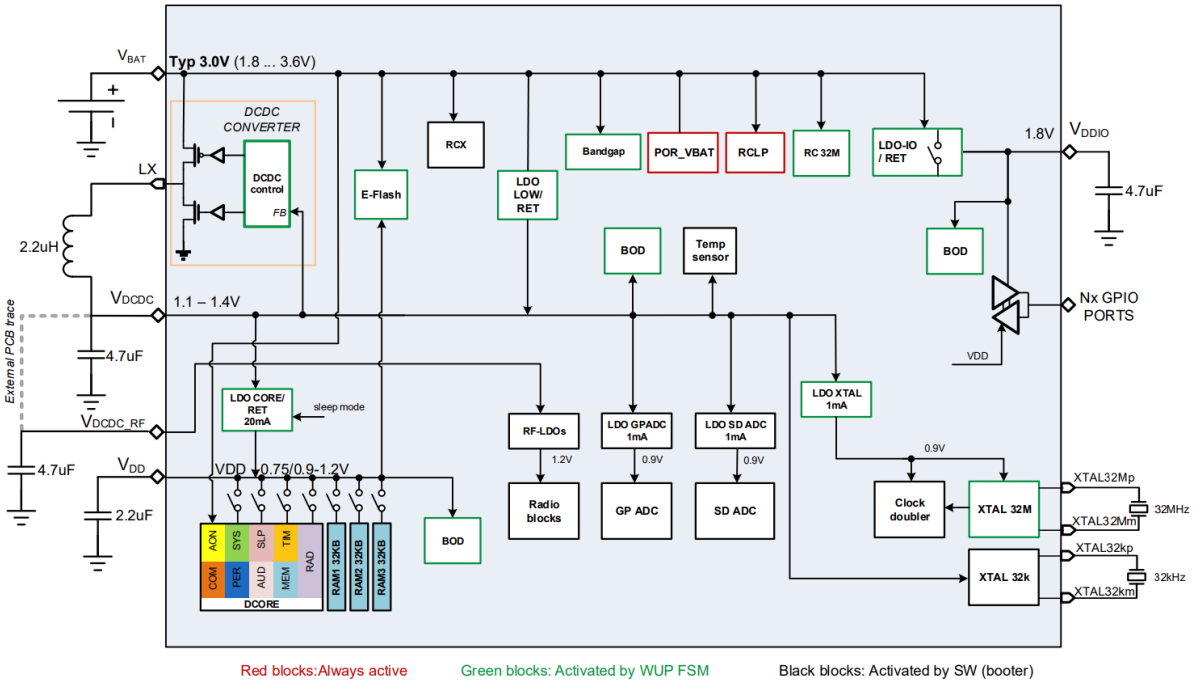

Figure 4. DA1459x power management unit architecture

In Figure 4, the circuits marked red are always active: POR_VBAT, RCLP, and PD-AON. The green blocks are activated by the wake-up FSM and the black blocks by software.

The VDCDC, VDDIO, and VDD rails all have an external decoupling capacitor. All rails have the possibility to use a BOD. The decoupling capacitor values in Figure 5 are the nominal, rated values.

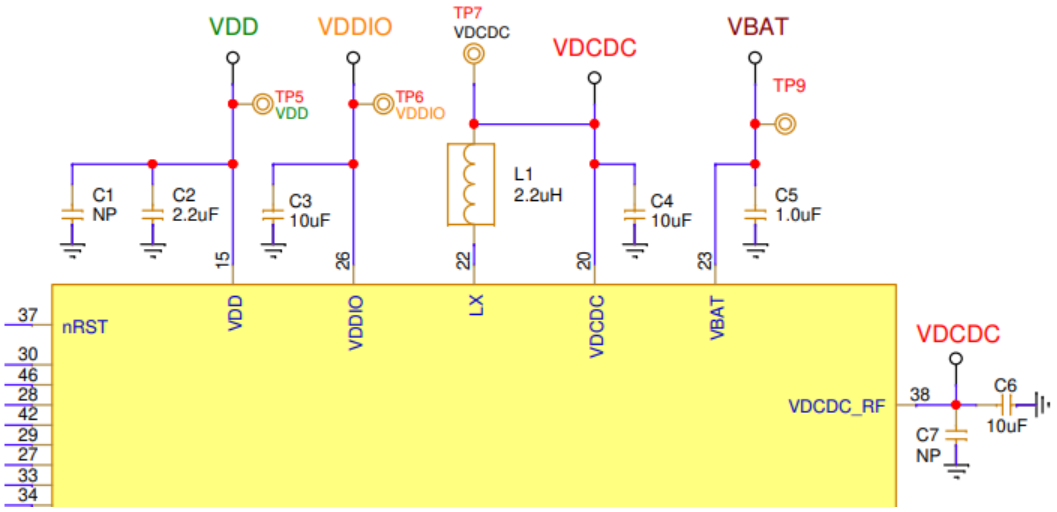

Figure 5. DA1459x power section schematic

- **VBAT**: main supply from the battery. VBAT supplies the DCDC, LDO_LOW and LDO_IO. The VBAT pin needs to be decoupled with a 1 µF/6.3 V/X5R ceramic capacitor.
- **VDD**: internal use only. Supplied by the LDO_CORE which in turn is supplied by the DCDC or by the LDO_LOW. The LDO_CORE is supplying the core with a programmable voltage between 0.9 V and 1.25 V. The VDD rail needs to be decoupled with at least a 2.2 µF/6.3 V/X5R ceramic capacitor.
- **VDDIO**: supplied by the LDO_IO. The LDO_IO provides a stable 1.8 V to the VDDIO rail. This rail supplies all GPIOs and peripherals connected to VDDIO.

The VDDIO rail needs to be decoupled with a 10 µF/6.3 V/X5R ceramic capacitor.

⚠	**CAUTION**
The LDO_IO has a current capability of 20 mA. This yields the total current to all 1.8 V peripherals connected to the VDDIO rail plus the current sourced to all GPIOs including QSPI. This becomes of importance when applying QSPI Flash or QSPI PSRAM memory devices having large read/write/erase currents. For situations having sufficient LDO headroom, that is for VBAT voltages larger than or equal to 2.1 V, it is allowed to draw incidental currents quite over 20 mA from the LDO_IO.	

⚠	**CAUTION**
The LDO_IO By-Pass switch as depicted in Figure 4 cannot be used because enabling the LDO_IO By-Pass mode results in an increased current consumption. See Ref. [2]. If VBAT supply is 3 Volt and peripherals designed for 3 V interface levels are to be connected to the DA1459x, then the VDDIO rail's voltage should also be made 3 V. To achieve this, one can directly connect the VDDIO rail with the VBAT rail and not use the LDO_IO By-Pass mode. The highest allowed voltage for both VBAT and VDDIO is 3.6 V. As such, the LDO_IO should be disabled: POWER_CTRL_REG[LDO_IO_ENABLE] = 0x0.	

The VDDIO rail can be discharged quickly by an internal circuit using a discharge current of 20 mA. This use this, set DISCHARGE_RAIL_REG [RESET_VIO] = 0x1. Note that the source is not disabled. Do not use this command if the VDDIO rail is shorted to VBAT.

- **VDCDC and VDCDC_RF**: internal use only. The VDCDC output and the VDCDC_RF input must be connected externally. This rail supplies the radio, the ADCs, the XTAL oscillators and the clock doubler. The VDCDC rail is powered by the DCDC or the LDO_LOW. The output voltage is programmable between 1.1 V and 1.45 V.

Each supply pin requires a 10 µF/6.3 V/X5R ceramic decoupling capacitor.

NOTE
The external connection (on PCB) from the VDCDC output rail to the VDCDC_RF pin supplying the radio are as shown in Figure 4 and Figure 5.

- **DCDC Converter:** supplying the VDCDC rail. The buck DCDC converter requires a low ESR power inductor: inductance 2.2 µH, at least 0.1 A saturation current, preferably having a little higher current capability, and

0.2 Ω maximum ESR for good efficiency of the DCDC converter. The peak switching-current in the DCDC inductor is 96 mA.

The DCDC Converter can be bypassed if desired. Subsequently the VDCDC rail is supplied by the internal LDO_LOW. Follow the required steps:

1. Disable the DCDC converter: DCDC_CTRL_REG[DCDC_ENABLE] = 0x0. The LDO_LOW is enabled automatically.
2. Remove the DCDC inductor, the DCDC Lx pin can be left floating.

Table 3. Recommended decoupling capacitors for DA1459x application

Rail	Designator	Capacitance	Rated voltage	Type	Size
VDD	C2	2.2 µF	6.3 V	X5R	0603M
VDDIO	C3	10 µF	6.3 V	X5R	1005M
VDCDC and VDCDC_RF	C4, C6	10 µF, close to each pin.	6.3 V	X5R	1005M
VBAT	C5	1 µF	6.3 V	X5R	0603M

5.2 Reset Pin (RSTn)

The RSTn pad is active Low and has an internal 25 kΩ pull-up resistor to VBAT. The RSTn pin should be driven externally using FET or a single button connected to the ground.

When active for a short time, it triggers a hardware reset. When active during a programmable time delay, it triggers a Power-On Reset (POR). The default time delay is ~3 s. Alternatively, a POR can be generated by an assigned GPIO.

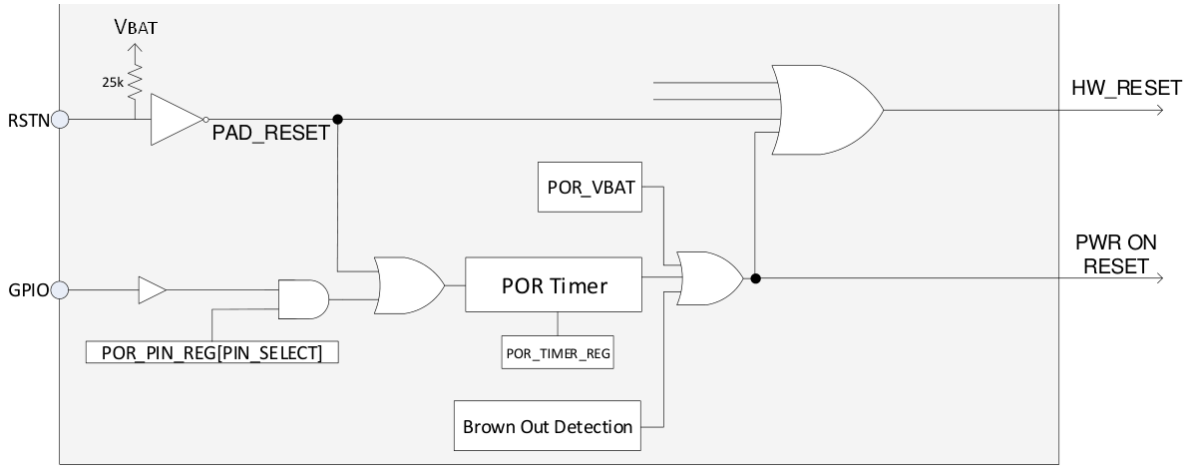

Figure 6. Reset, POR, and BOD block diagram

5.3 Brown-Out-Detector and Power-On-Reset Circuit

The DA1459x incorporates a single Power-On-Reset (POR) circuit, POR_VBAT on the VBAT rail, which has a threshold of ~1.5 V. When the VBAT voltage drops below this level, it triggers a POR.

The other rails, that are VDDIO, VDCDC, and VDD, are protected by the Brown-Out-Detector (BOD). These BOD circuits can be found in the power management block diagram (Figure 4).

The VDD rail has a programmable BOD level to cope with different voltage levels in Active and Sleep mode.

To avoid false BOD triggering on the VDD rail when going into Sleep mode and when waking up, it is recommended to disable or mask the BOD_VDD during sleep. Masking is the preferred method. Masking the BOD_VDD comparator output is done as follows: BOD_CTRL_REG [BOD_VDD_MSK] = 0x1: POR trigger due to BOD blocked. This was implemented in the latest SDK release.

5.4 Digital I/O Pins

All GPIOs have software-configurable input/output pin assignment.

- Selectable pull-up and pull-down resistor of 25 kΩ.
- Selectable pull-up and pull-down resistor of 40 kΩ for the QSPI pads.
- Programmable Open-Drain functionality.
- Pull-up voltage to VDDIO or to VBAT.
- All GPIOs except P0_00 ~ P0_05 can be used in Low-Drive mode (reduced drive strength).

These pin assignments can be configured in Px_yy_MODE_REG. Figure 7 shows the port block diagram.

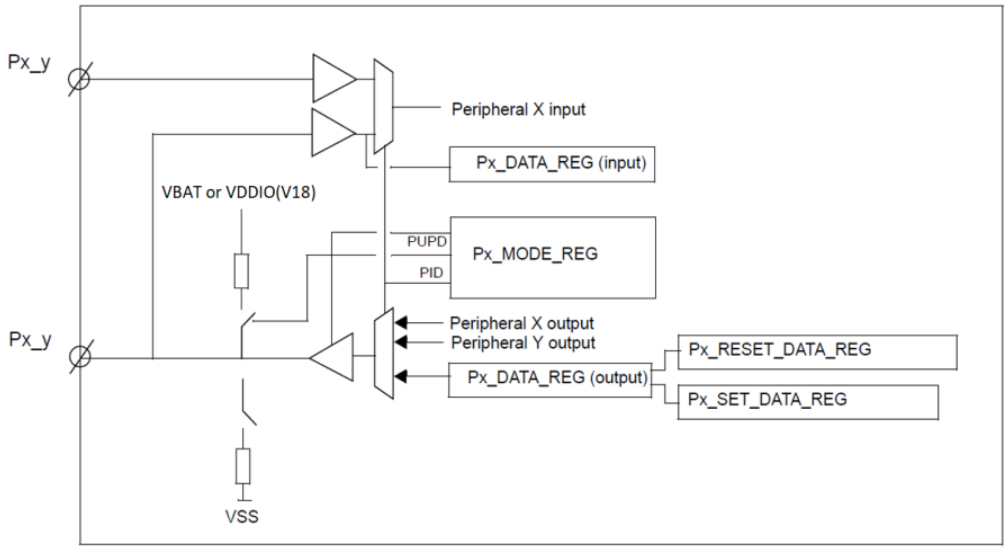

Figure 7. Port P0 and P1 with programmable pin assignment

The GPIO VOL and VOH voltages are defined for a sink or source current of 3.5 mA. A little more current than 3.5 mA may be sourced or sunk, but the VOH or VOL voltage becomes lower or higher respectively. It's advised not to sink or source more than 5 mA current from a GPIO. The total maximum source or sink current in all GPIOs must be limited to 20 mA.

When used in Low-Drive mode, the source or sink current is limited to 0.35 mA to be compliant to the VOL and VOH levels as listed in the datasheet. The advised maximum sink or source current in the Low-Drive mode is 0.5 mA. The Low-Drive mode can be selected per pin in Px_WEAK_CTRL_REG [Px_LOWDRV].

The QSPI port has a stronger drive strength: 4, 8, 12, or 16 mA maximum when used in QSPI mode. The QSPI drive strength can be programmed in QSPIC_GP_REG [QSPIC_PADS_DRV]. The QSPI pins also have Slew Rate Control: from ~1.8 V/ns (weak) to ~2.6 V/ns (strong) at CL = 6 pF and Idrive = 16 mA: QSPIC_GP_REG [QSPIC_PADS-SLEW].

5.4.1 GPIO Interference to the 32 MHz Crystal Oscillator and to the Radio

The listed GPIOs in Table 4 and Table 5 are potentially affecting the radio performance, in particular the RF sensitivity, when toggling at frequencies far above 1 MHz. Around and below 1 MHz toggle frequency the interference to the radio is negligible. Make sure that the listed GPIOs causing medium degradation are not toggling fast when the radio is active.

The worst GPIO is P1_12: it also degrades the performance a little at 1 MHz or lower frequencies.

The most robust P0 GPIOs are: P0_01, P0_02, P0_04, P0_05, and P0_14.

The most robust P1 GPIOs are: P1_03 and P1_11.

All other GPIOs can cause a minor (2 dB max.) or a medium (4 dB max.) radio performance degradation only when toggled much faster than 1 MHz. These are listed in Table 4 and Table 5.

When RDS (Low Drive Strength) is enabled, no performance degradation is observed for all GPIOs. Low Drive Strength (P0_/P1_LOWDRV) can be enabled in P0_/P1_WEAK_CTRL_REG.

P0_WEAK_CTRL_REG (0x500206A4)

Bit	Mode	Symbol/Description	Reset
15:6	R/W	P0_LOWDRV 0 = P0_x port is driven with normal drive strength (default) 1 = P0_x port is driven with reduced drive strength	0x0

P1_WEAK_CTRL_REG (0x500206A8)

Bit	Mode	Symbol/Description	Reset
15:0	R/W	P1_LOWDRV 0 = P1_x port is driven with normal drive strength (default) 1 = P1_x port is driven with reduced drive strength	0x0

Figure 8. P0 and P1 low drive setting

Table 4. Interfering GPIOs of FNQFN52 – port 0

FCQFN52 GPIOs	Toggling ≤ 1 MHz	Toggling >> 1 MHz	RDS enabled
P0_00	Negligible	Minor degradation	x
P0_03	Negligible	Minor degradation	x
P0_08	Negligible	Medium degradation	None
P0_09	Negligible	Medium degradation	None
P0_10	Negligible	Medium degradation	None
P0_11	Negligible	Medium degradation	None
P0_12	Negligible	Minor degradation	None

Table 5. Interfering GPIOs of FNQFN52 – port 1

FCQFN52 GPIOs	Toggling ≤ 1 MHz	Toggling >> 1 MHz	RDS enabled
P1_00	Negligible	Minor degradation	None
P1_01	Negligible	Minor degradation	None
P1_02	Negligible	Minor degradation	None
P1_04	Negligible	Medium degradation	None
P1_05	Negligible	Minor degradation	None
P1_06	Negligible	Minor degradation	None
P1_07	Negligible	Minor degradation	None
P1_08	Negligible	Medium degradation	None
P1_09	Negligible	Medium degradation	None
P1_10	Negligible	Minor degradation	None
P1_12	Minor degradation	Medium degradation	None
P1_13	Negligible	Medium degradation	None
P1_14	Negligible	Medium degradation	None
P1_15	Negligible	Medium degradation	None

Additionally, it is important to mention that, for example, clock signals or high-speed lines (I^2C, SPI, QSPI, PWM, and so on) must not be routed near the XTAL32M oscillator and the RFIO port. This must be avoided.

Figure 9 shows the possibly interfering GPIOs, in the red colored rectangles, causing medium radio performance degradation when toggling fast and is not using the RDS feature.

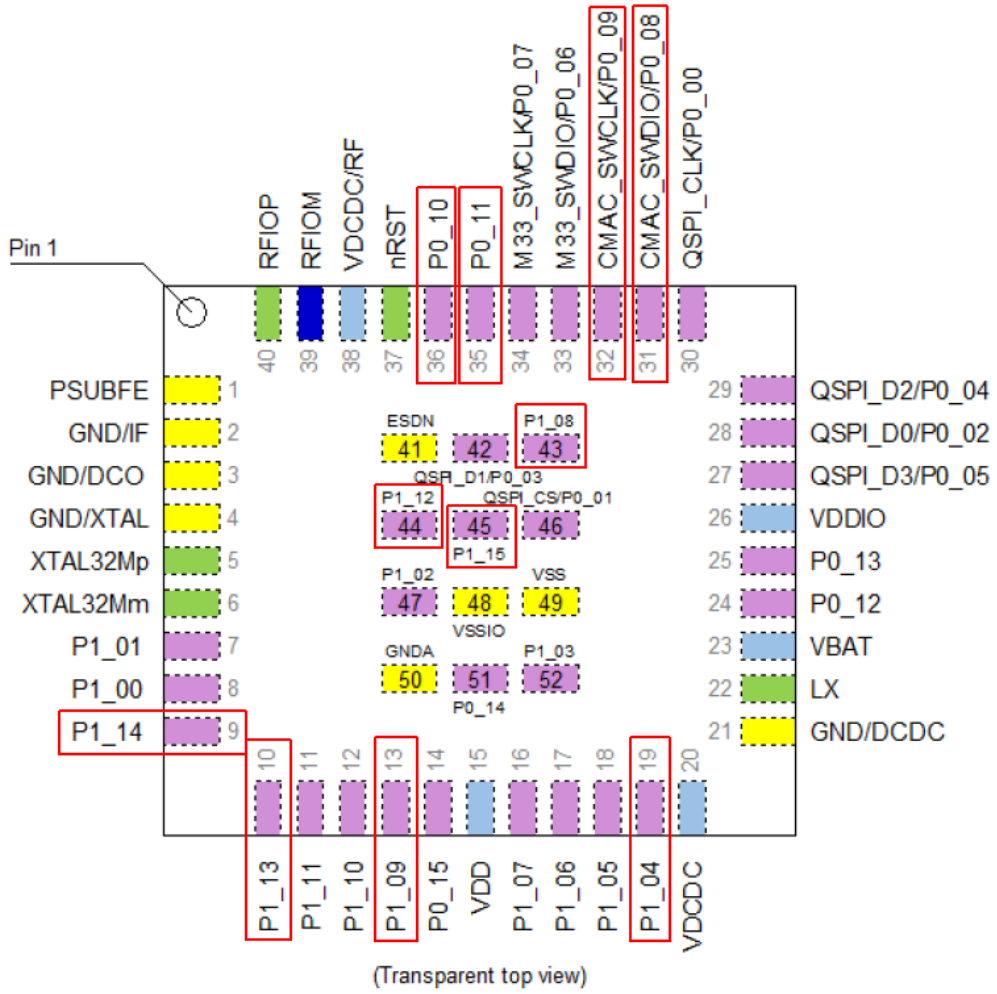

Figure 9. Potentially interfering GPIOs when fast toggling

5.5 Crystals and Clocks

The DA1459x comprises two digitally controlled crystal oscillators: a 32 MHz crystal oscillator (XTAL32M) and a low-power 32.768 kHz crystal oscillator (XTAL32K) used in Sleep mode. The XTAL32K low-power oscillator is only available in the FCQFN52 package.

5.5.1 XTAL32M Oscillator

For the specification of 32 MHz crystals, see Ref. [1] (section 3.15). Table 6 lists a few examples of suitable 32 MHz crystals.

Table 6. Examples of suitable 32 MHz crystals

32 MHz crystals	muRata	NDK
Part number	XRCGB32M000F1S1AR0	NX2016SA-32MHZ-EXS00A-CS10925
Frequency	32 MHz	32 MHz
Frequency tolerance	±10 ppm	±20 ppm
Temperature Frequency Drift	±10 ppm	±20 ppm
Aging	±2 ppm max./year	±3 ppm max./1 year ±5 ppm max./5 years
Load capacitance	6 pF	6 pF
Shunt capacitance	0.69 pF	0.6 pF

32 MHz crystals	muRata	NDK
Equivalent Series Resistance (ESR)	50 Ω max	60 Ω max
Drive Level	300 µW max	200 µW max
Temperature Range	-30°C ~ +85°C	-40°C ~ +85°C
Size L x W x H (mm)	2.0 x 1.6 x 0.65	2.0 x 1.6 x 0.45

The 32 MHz crystal oscillator is trimmable over a frequency range of approximately +/- 50 ppm when applying a crystal having a CL value = 6 pF using the XTAL32M_TRIM_REG register. The XTAL32M_TRIM value setting varies from 0 to 255 (0xFF). Applying value 0 results in the minimum load capacitance and hence the maximum XTAL32M oscillator frequency, applying a value 255 results in the maximum load capacitance and hence the minimum XTAL32M oscillator frequency.

The XTAL32M Trim capacitance, which forms the load capacitance for the 32 MHz crystal, follows the equation: CLoad = 3.25 pF + 0.05 pF * TRIM, in which TRIM can vary from 0 to 255.

A typical XTAL32M frequency versus Trim value behavior measured for the DA1459x Pro-DK daughterboard is shown in Figure 10.

The XTAL32M frequency varies from approximately +85 ppm for XTAL32M_TRIM value = 0, to -55 ppm for XTAL_TRIM value = 255.

In this measured board, the correct XTAL frequency (32.000 MHz) was obtained when applying XTAL32M_Trim value = 95.

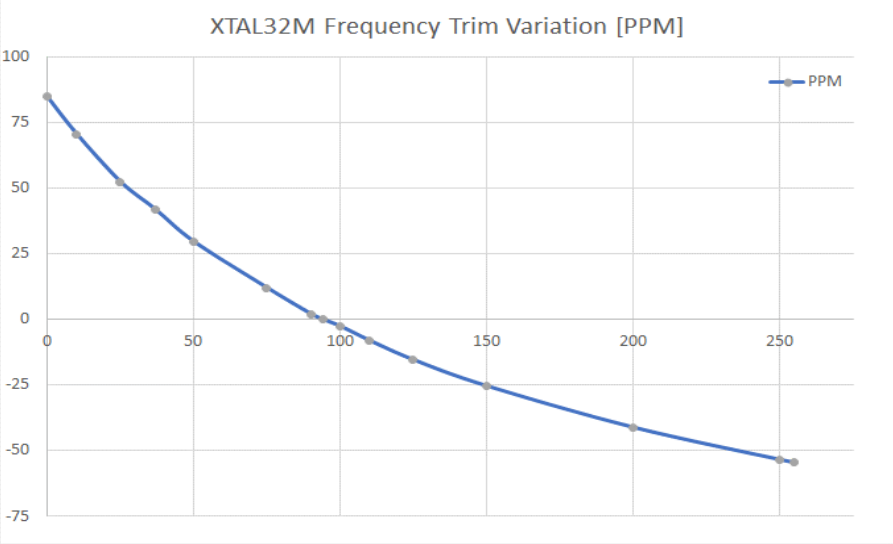

Figure 10. Typical XTAL32M trim range: frequency (ppm) vs XTAL32M_Trim value

5.5.2 XTAL32K Oscillator (DA1459x FCQFN52 Only)

For the specification of 32.768 kHz crystals, see Ref. [1] (section 3.14). Table 7 lists a few examples of suitable 32.768 kHz crystals.

Table 7. Examples of suitable 32.768 kHz crystals

32.768 kHz crystals	Abracon Corp.	Seiko Epson Corp.
Part number	XTAL_ABS06-32.768	FC1610AN
Frequency	32.768 kHz	32.768 kHz
Frequency tolerance	±20 ppm	±20 ppm
Load capacitance	7 pF typ.	7 pF typ.
ESR	80 kΩ max	90 kΩ max
Drive Level	0.1 µW typ, 0.5 µW max.	0.5 µW max.
Size L x W x H (m m)	2.0 x 1.2 x 0.6	1.65 x 1.05 x 0.5

In case no 32.768 kHz crystal is applied, the XTAL32K pins P1_13 and P1_14 can be used as GPIO.

5.5.3 Outputting Clocks

Outputting the LP_CLK to GPIO P0_12:

Outputting the LP_CLK, being RCLP, RCX or XTAL32K, to P0_12 is also working during sleep. Follow the required steps:

1. Set PUPD of P0_12 to Output (0x3). Leave the PID at its default value 0x0.
2. Enable PMU_CTRL_REG [LP_CLK_OUTPUT_EN] = 0x1.
3. The selected Low Power Clock is exported. The exported XTAL32K square-wave signal has 1.8 Vpp amplitude (VDDIO level) and a duty-cycle of about 70%. See Figure 11.
4. To select another LP Clock as source and for output, select it in CLK_CTRL_REG [LP_CLK_SEL]: RCLP, RCX or XTAL32K. See Figure 12.

Figure 11: Exported XTAL32K clock 1.8Vpp

3:2	R/W	LP_CLK_SEL Sets the clock source of the Lower Power clock 0x0: RCLP 0x1: RCX 0x2: XTAL32K through the oscillator with an external Crystal.	0x0

Figure 12. CLK_CTRL_REG [LP_CLK_SEL]

Outputting any clock to any available GPIO:

This method only works in Active mode. Follow the required steps:

1. Select an available GPIO, set its PUPD to 0x3 (Output), and its PID to 0x17 (CLOCK).
2. In GPIO_CLK_SEL_REG, set FUNC_CLOCK_EN = 0x1, and select which clock to be exported in FUNC_CLOCK_SEL. For example, XTAL32M = 0x3. See Figure 13.

3	R/W	FUNC_CLOCK_EN If set, it enables the mapping of the selected clock signal, according to FUNC_CLOCK_SEL bit-field.	0x0
2:0	R/W	FUNC_CLOCK_SEL Select which clock to map when PID = FUNC_CLOCK. 0x0: XTAL32K 0x1: RCLP 0x2: RCX 0x3: XTAL32M 0x4: RC32M 0x5: DIVN	0x0

Figure 13. GPIO_CLK_SEL [GPIO_CLK_SEL_REG]

5.6 UART

The DA1459x contains two UART instances: UART and UART2. Both support DMA. Only UART2 supports hardware flow control signals RTS and CTS.

Supported Baud Rates range from 1200 to 1000000 when using the 32 MHz clock and can be extended to 3000000 when using the SYS_CLK = 64 MHz (enabling the Doubler).

The UART boot pins are assigned to P0_13 and P0_15, UART Boot TX and UART Boot RX respectively.

Table 8. UART boot pins

Function	GPIO	WLCSP39 pin	FNQFN52 pin
UART Boot TX	P0_13	G5	25
UART Boot RX	P0_15	J5	14

5.7 SWD (JTAG)

The DA1459x SoC has two Serial Wire Debug (SWD) interfaces. One for the CMAC Arm® Cortex® M0+ and one for the Arm Cortex M33 CPU.

If the debugger is not enabled (SYS_CTRL_REG [DEBUGGER_ENABLE = 0x0), the listed SWDIO and SWCLK pins in Table 9 can be used as GPIO.

Table 9. SWD debug pins

Function	GPIO	WLCSP39 pin	FNQFN52 pin
M33 SWDIO	P0_06	B6	33
M33 SWCLK	P0_07	A7	34
CMAC SWDIO	P0_08	D6	31
CMAC SWCLK	P0_09	C7	32

5.8 QSPI Flash and QSPI RAM Controller

The Quad SPI Controller (QSPIC) provides an interface to serial QSPI Flash or PSRAM memory devices. The QSPIC supports the standard Serial Peripheral Interface (SPI) and a high performance Dual/Quad SPI Interface. The QSPI RAM feature provides a low-cost RAM extension for infrequently used data.

The Quad SPI Controller supports the following SPI modes:

- Single: Data transfer through two unidirectional pins.
- Dual: Data transfer through two bidirectional pins.
- Quad: Data transfer through four bidirectional pins.

The QSPI_CS is an active-low output chip-select signal. An external pull-up resistor to VDDIO is not needed. The QSPI_CLK clock frequency is up to 64 MHz.

To avoid signal integrity issues, keep the distance between the processor and the QSPI Flash or PSRAM memory device as short as possible, try to have the length of the traces as equal as possible, and route with enough spacing to avoid crosstalk.

The QSPI device normally would be supplied by the VDDIO rail, the internal LDO_IO. For higher IO voltage levels than 1.8 V and the current limitation of the internal LDO_IO, see Section 5.1: VDDIO.

NOTE
When adding a QSPI Flash or QSPI RAM device (U2) to the DA1459x evaluation board, remove the serial resistors R1, R2 and R6 ~ R9 connected to P0_0 ~ P0_5 of the motherboard interface connector to avoid QSPI signal integrity issues. See Figure 2 and Figure 3.

5.9 Hibernation Mode and Wake-up

Hibernation mode is enabled by setting HIBERN_CTRL_REG [HIBERNATION_ENABLE]. All LDOs including the Retention LDOs are turned off in Hibernation mode. VBAT supplies the wake-up from hibernation controller which resides in the Always-On Power-Domain (PD_AON).

Only two GPIOs are available to wake up the chip from hibernation mode: P0_14 and P1_04.

Table 10. Hibernation wake-up pins

Hibernation wake-up	GPIO	WLCSP39 pin	FNQFN52 pin
Wake-up source 1	P0_14	J3	51
Wake-up source 2	P1_04	Not available	19

The wake-up pin selection is done in HIBERN_CTRL_REG [HIBERN_WKUP_MASK]. The polarity of the wake-up pin is set in HIBERN_CTRL_REG [HIBERN_WKUP_POLARITY]. Wake-up source 2 is available in the FNQFN52 version only, not in the WLCSP39 version.

NOTE
When the wake-up polarity is set to active low, the GPIO must be pulled up externally. For example, VBAT. Reason: the VDDIO supply is turned off in Hibernation mode. For the same reason, GPIO State Retention is not possible in Hibernation mode.

5.10 GPADC and SDADC

5.10.1 GPADC

The DA1459x SoC is equipped with a high-speed ultra-low power 10-bit general purpose Analog-to-Digital Converter (GPADC). The ADC analog part is internally clocked with 100 MHz, the logic part by the system clock (SYS_CLK). The ADC can operate in Unipolar (Single-Ended) mode and Bipolar (Differential) mode.

The ADC has its own voltage regulator (LDO) of 0.9 V that represents the full-scale reference voltage. Hence the base input voltage range is 0.9 V. By selecting the 2x, 3x, or 4x attenuator the maximum input voltage to the ADC may be 1.8 V, 2.7 V, or 3.6 V respectively.

The VBAT voltage can be measured internally and automatically the 4x attenuator is applied. The total GPADC attenuator resistance is 240 kΩ.

The impedance from the signal source to the unbuffered ADC input pin must be very small. Otherwise, filter capacitors are required from the input pins to ground (single-ended mode) or from pin to pin (differential mode).

By applying up to 128x averaging, which is handled by hardware, the Effective Number of Bits (ENOB) can be as high as 11.5 bits.

The FCQFN52 package incorporates eight single-ended or four differential ADC inputs. The WLCSP39 package has half the number of inputs: four single-ended or two differential ADC inputs. Figure 14 shows the GPADC block diagram.

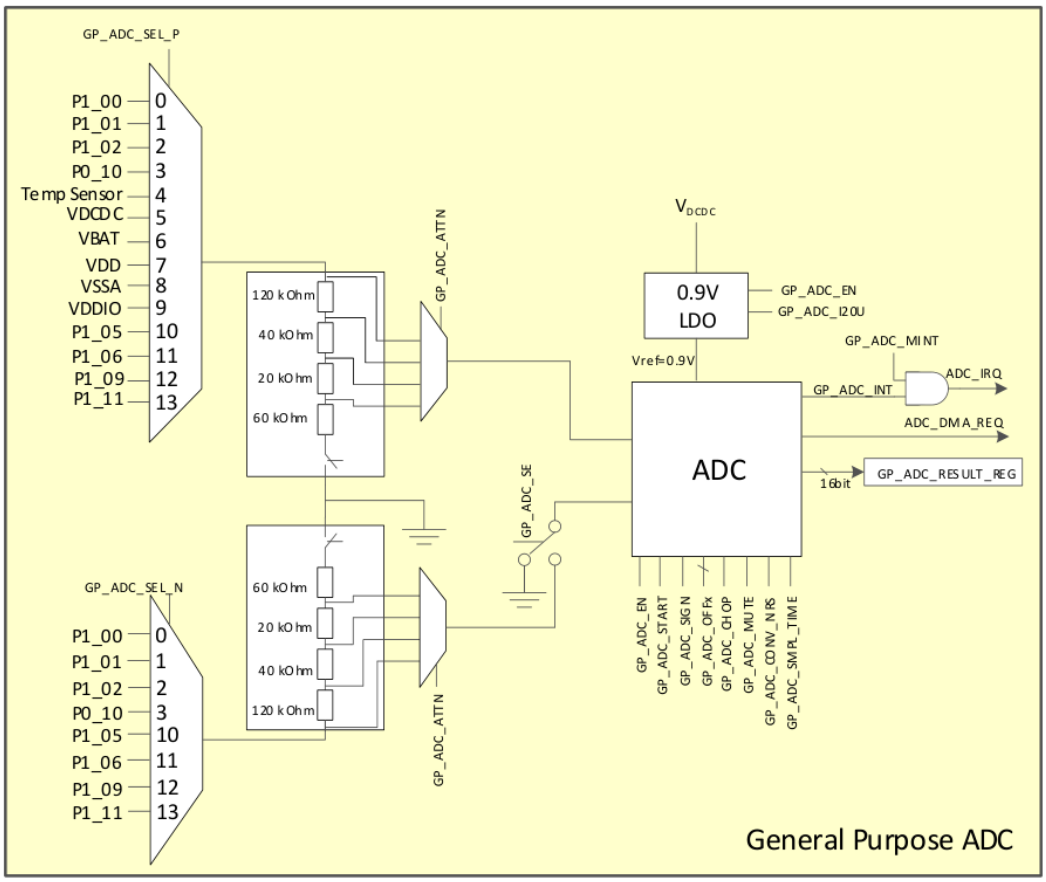

Figure 14. GP-ADC block diagram

5.10.2 SDADC

The DA1459x SoC is equipped with a ΣΔ ADC that supports two operation modes: sensor mode and audio mode. Audio mode delivers a SINAD value of almost 70 dB at a rate of 16 ksamples/s. Sensor mode implements a third order filter that can achieve almost 13 ENOB at 968 samples/s rate by applying an oversampling rate of 1024 (SDADC_OSR = 2).

The FCQFN52 package incorporates eight single-ended or four differential ADC inputs. The WLCSP39 package has half the number of inputs: four single-ended or two differential ADC inputs. Two inputs are reserved for the Programmable Gain Amplifier (PGA) in Audio mode.

The VBAT voltage again can be monitored internally by using the internal 4x attenuator with 12 bits accuracy.

The internal reference voltage is equal to 0.9 V and is selected by default.

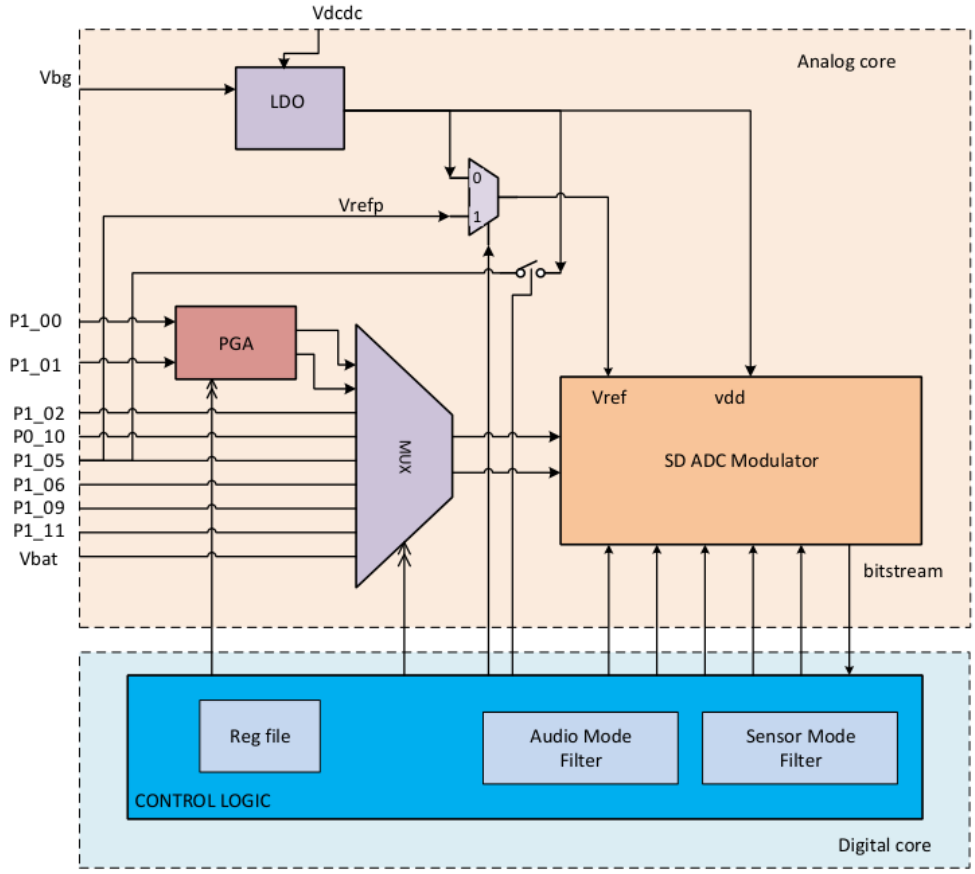

Figure 15. SDADC block diagram

NOTE
The following information is for the DA1459x FCQFN52 package only.

An external voltage reference input (SDADC_REFp) for the SDADC is available for more precise ADC results. The external voltage reference must be applied to P1_05 and may not exceed 0.9 V. The SDADC_REFn pin (P1_06) must be grounded. See Figure 16.

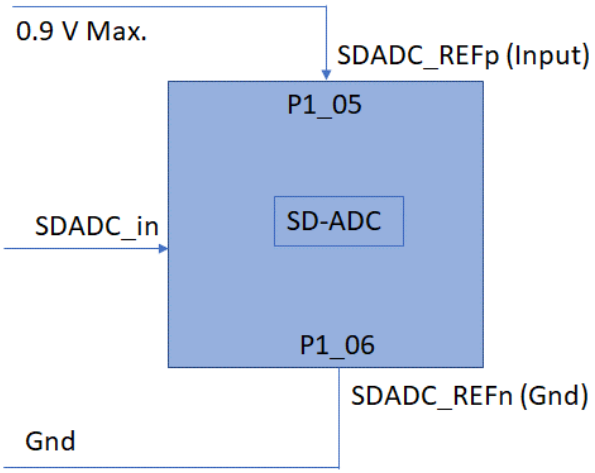

Figure 16. SDADC using external voltage reference

The internal voltage reference from the LDO, being 0.9 V, can be output to P1_05 and can be used as a reference voltage for the used sensor. This feature amongst others can be used for accurate temperature measurements using an NTC. Sensor supply voltage variations do not affect the NTC measurement anymore, the internal SDADC reference voltage and the supply voltage for the NTC network are the same. This feature is shown in Figure 17.

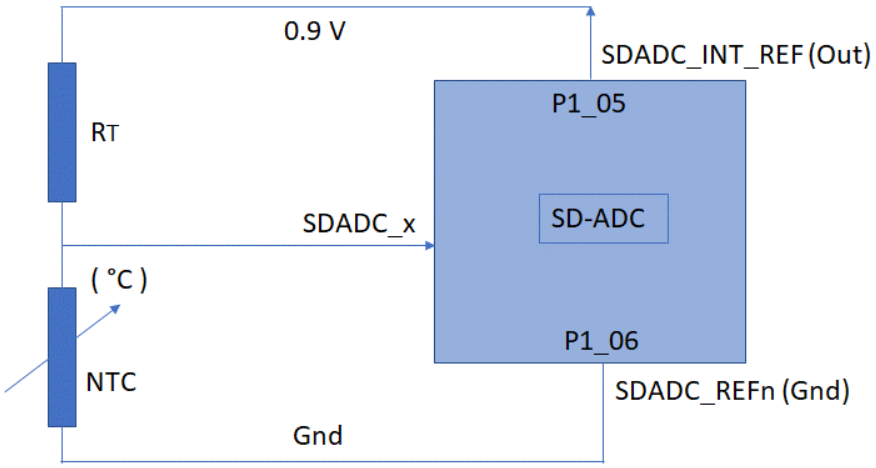

Figure 17. Example of accurate temperature measurement

NOTE
The maximum current that the internal voltage reference LDO can supply is 1 mA. Make sure the NTC network does not draw a higher current than this. To save power, it is advised to use a value of 10 kΩ or higher for resistor R_T. The SDADC_4 and SDADC_5 inputs are not available as ADC input in the above two application cases. These pins are now used for SDADC_REFp (or SDADC_INT_REF) and SDADC_REFn.

5.11 RFIO Port

The RFIO port is a combined single-ended RF input and RF output. Its impedance is 50 Ω. Figure 18 shows the RF output circuitry, including the on-board printed IFA antenna, ANT1. See Ref. [4].

Z2, Z1, and Z3 form the antenna matching filter. The values of this matching filter must be determined for each new design. The matching filter must be placed close to the antenna feed point.

Z5, Z4, and Z6 form an RF Low-Pass Filter (LPF). This filter is required to suppress the TX harmonics to meet FCC and ETSI requirements on spurious emissions and is required when the TX output power is +6 dBm. This filter must be placed as close as possible to the RFIOp pin (pin 40) of the DA1459x device.

NOTE
Till the release date of this document, it was not known whether the LPF filter would be required for output powers below +6 dBm. This also depends on the frequency characteristics of the antenna matching filter: low-pass or high-pass and board design. As soon this information is available, it is provided.

The RF PCB track sections RF1, RF2, RF3, RF4 must have a characteristic impedance of 50 Ω. Best to be realized with a ground plane under the RF part. Z7 may be either a capacitor having a value of 10 pF or it may be omitted. All listed filter parts have mounting size 0603M (0201).

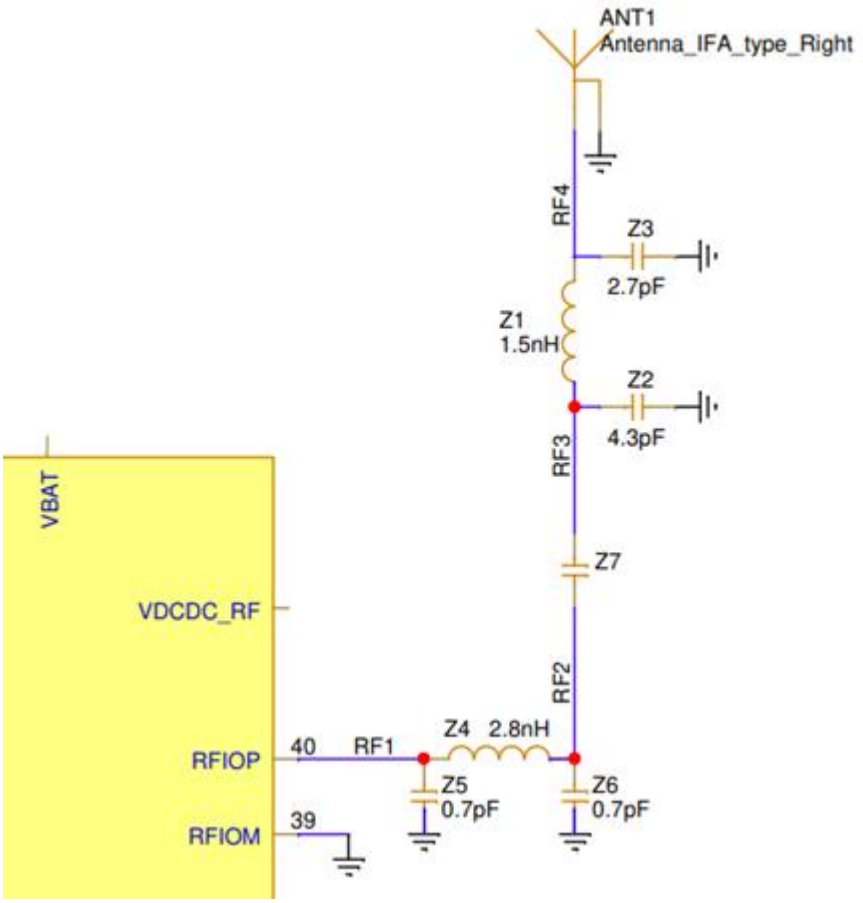

Figure 18. RFIO port and RF circuitry

5.12 ESD Protection

If a GPIO or the antenna can be touched by users, provide an ESD protection device for them. For the RF input an ultra-low capacitance device must be used.

The ESD protected signal lines should be routed directly to the transient-voltage-suppression diode. Ground connections should be made directly to the ground plane to minimize parasitic inductance.

For connectors, the transient-voltage-suppression devices should be placed as close to the connector as possible to reduce transient coupling into nearby traces.

The secondary effects of radiated emissions can cause upset to other areas of the board, even if there is no direct path to the connector.

Apply Uni-Directional ESD protection devices on signals having only positive polarity. Such devices have a lower forward bias voltage for better clamping of negative ESD voltages.

6. DA1459x PCB Layout

6.1 WLCSP39 PCB Design

The DA1459x WLCSP39 board of the evaluation kit is a four-layer design. Micro-vias are used due to the fine pitch of 0.42 mm.

The board has a solid ground-plane on the second inner-layer L3. It also has a ground plane and some supply and signal routing on the first inner-layer L2, the layer directly under the top layer, for low impedance routing of high-speed clock signals and as reference ground for 50 Ω PCB tracks where required. The chip is grounded to the L3 ground layer.

Total thickness of the WLCSP39 PCB is 0.99 mm. Dielectric distances between top layer or bottom layer and inner layers are 0.065 mm. Dielectric distance between the inner layers is 0.71 mm. Table 11 lists the PCB structure.

Table 11. DA1459x WLCSP39 PCB layer structure

Subclass name	Type	Material	Thickness (mm)
	Surface	Air	-
L1 TOP Layer	Conductor	Copper	0.03
	Dielectric	FR-4	0.065
L2 1st Internal Layer	Plane	Copper	0.03
	Dielectric	FR-4	0.71
L3 2nd Internal Layer	Conductor	Copper	0.03
	Dielectric	FR-4	0.065
L4 BOTTOM Layer	Conductor	Copper	0.03
	Surface	Air	-

6.2 FCQFN52 PCB Design

The DA1459x FCQFN52 board of the evaluation kit is a four-layer design. Due to the fine pitch of 0.4 mm and the number of pins in the FCQFN52 package, it requires a dense micro-via approach.

The designed board has a solid ground-plane on the first inner layer, the one directly under the top layer, for low impedance routing of high-speed clock signals and as reference ground for 50 Ω PCB tracks where required. The other layers are used for routing but have ground planes too. The top layer ground amongst others is used to shield the RFIO trace and is connected by many vias to the first inner layer ground plane.

Total thickness of the FCQFN52 PCB is 0.982 mm. Dielectric distances between top layer or bottom layer and inner layers are 0.24 mm. The dielectric distance between the inner layers is 0.36 mm. Table 12 lists the PCB structure.

Table 12. DA1459x FCQFN52 PCB layer structure

Subclass name	Type	Material	Thickness (mm)
	Surface	Air	-
L1 TOP Layer	Conductor	Copper	0.0355
	Dielectric	FR-4	0.24
L2 first Internal Layer	Plane	Copper	0.0355
	Dielectric	FR-4	0.36
L3 second Internal Layer	Conductor	Copper	0.0355
	Dielectric	FR-4	0.24
L4 BOTTOM Layer	Conductor	Copper	0.0355
	Surface	Air	-

6.3 PCB Routing Guidelines

6.3.1 General PCB Routing Guidelines

- Active components operating at high frequency should have a layout as compact as possible to prevent the cross-coupling between lines and to minimize the parasitic effects which have negative impacts on the operating parameters.
- Always provide a solid grounding to the radio IC. Use as many vias as possible to create a solid GND under the IC itself and connect the IC to the inner GND layer.
- Remove GND under the pads of high speed and fast switching power components, such as QSPI flash and crystals.

6.3.2 RF Specific Guidelines

- It is important to properly route the RF strip line to the antenna. The design of RF GND is also important. See Figure 19 and Figure 20.
- FCQFN52: RFIOm (#39), PSUBFE (#1) and GND/IF (#2) are connected to the same ground at top layer and to the inner ground plane L2: highlighted in yellow. Grounding the RFIOm pin separately by using a via to the ground plane is also a good strategy. DCO GND (#3) is grounded to the ground plane using a separate via: highlighted in light blue. See Figure 19.
- WLCSP39: RFIOm (#A3) is grounded directly to the top layer ground and to the inner layer grounds L2 and L3. PSUBFE (#C1) and GND_DCO (#E1) are grounded to the top layer ground using their own ground connection. Additionally, GND_IF (#C3), GND_XTAL (#E3), and GNDA (#F4) are shorted to each other on the top layer and grounded to the ground at L3. The top layer (L1) ground is connected to the inner ground layers. See Figure 20.
- The RFIO 50 Ω track is routed over a ground plane and has ground along both sides of the track to shield the track. The ground area along the track is connected to the inner ground plane by multiple vias.
- The antenna must not have ground under its feedline and the antenna pattern itself. Else it cannot radiate freely. And some free area must be reserved around the antenna for optimal performance. Allow ~5 mm free area (no copper) between both ends of the antenna to other copper areas and ~5 mm free area between the antenna strip and the PCB ground area.
- The antenna pattern is routed on the top layer, on both inner layers and on the bottom layer and stitched together by multiple vias. The antenna feed is on top layer (L1) only, see Ref. [4].

In Figure 19, the top layer copper (L1) is colored red, the inner ground layer copper (L2) is colored purple/blue.

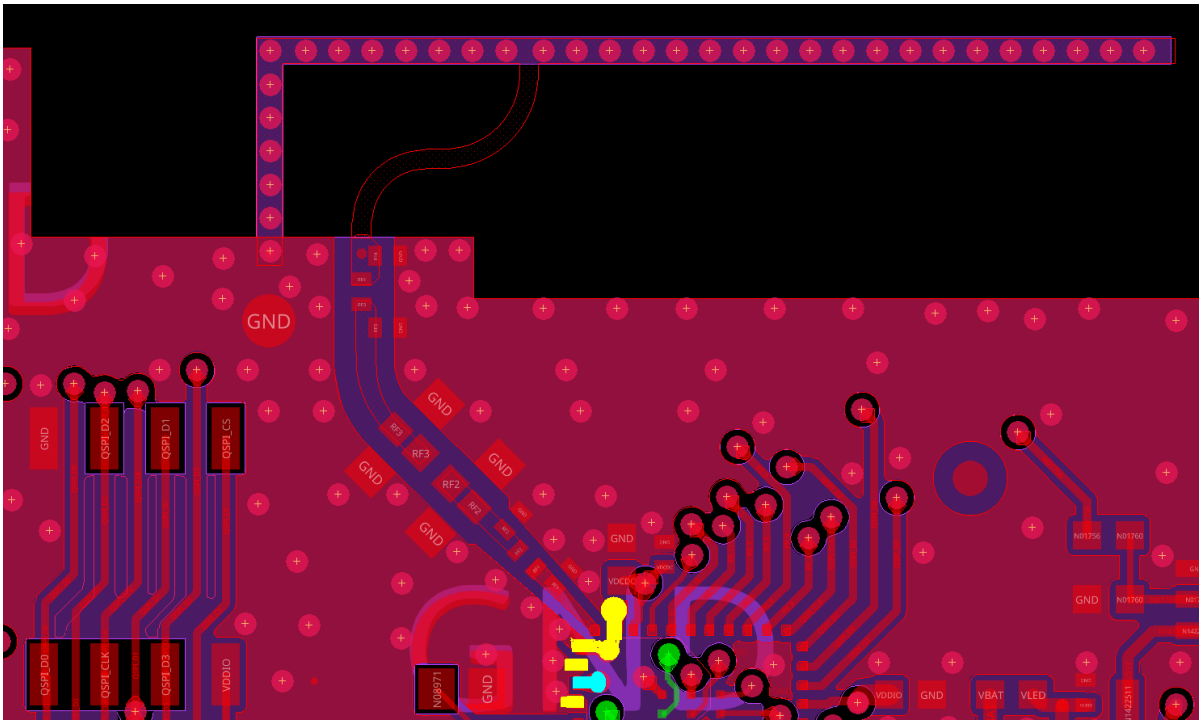

Figure 19. FCQFN52 RFIO routing and RFIOm grounding

Figure 20 shows the top layer copper (L1) only.

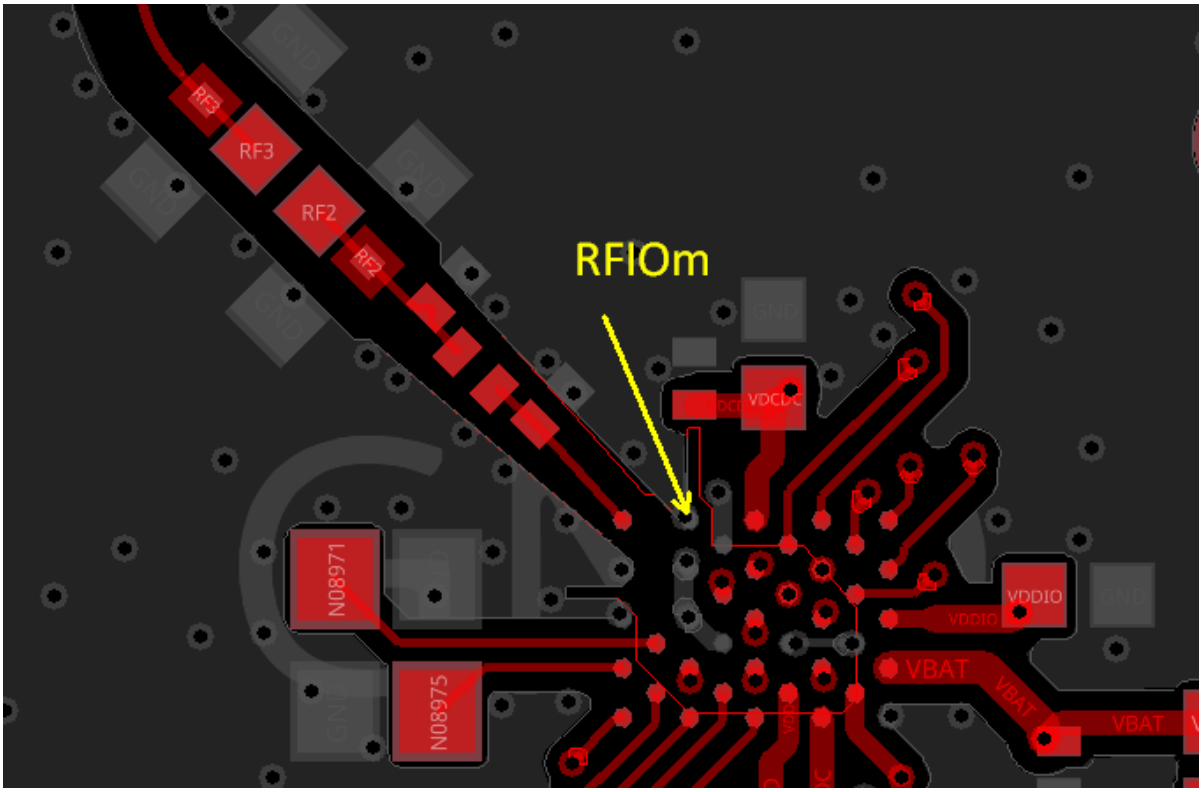

Figure 20. WLCSP39 RFIO routing and RFIOm grounding

6.3.3 XTAL Specific Guidelines

- Place the 32 MHz XTAL as close as possible to the IC to minimize additional capacitive load on the input pins and to reduce the chance of crosstalk and interference with other signals on the board.
- Do not route any lines under the XTAL32M area – risk of coupling and interference.

- Remove GND area under the XTAL "hot" pads to minimize the capacitive load to the XTAL32M oscillator. See Figure 21.
- If possible, try to create a ground shield around the crystals, and connect it to the XTAL32M GND pin (#4). The XTAL32M ground pads are also connected to the XTAL32M GND pin (#4). See Figure 21.

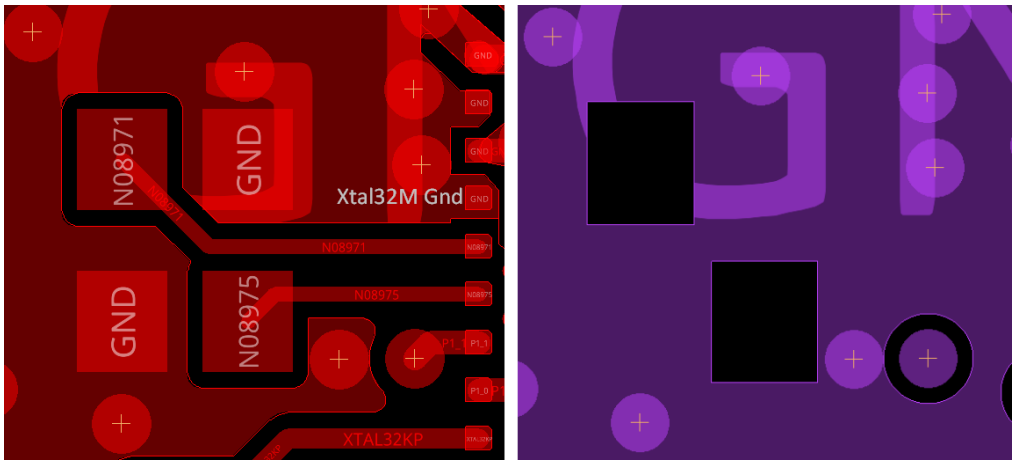

Figure 21. XTAL32M PCB design: top layer (L) and first inner layer (R)

6.3.4 QSPI Flash or QSPI RAM Specific Guidelines

- Place QSPI data Flash or RAM as close as possible to the chip.
- Add a decoupling capacitor next to the supply pin of the QSPI device.
- Route the traces with equal length if possible.
- Have solid ground under the traces to create controlled impedance traces. A good PCB design practice is to have controlled impedance of the routed traces, for example, 60 to 80 Ω.
- Ensure the safe distance between traces to avoid crosstalk.

Appendix A Reflow Soldering Profile

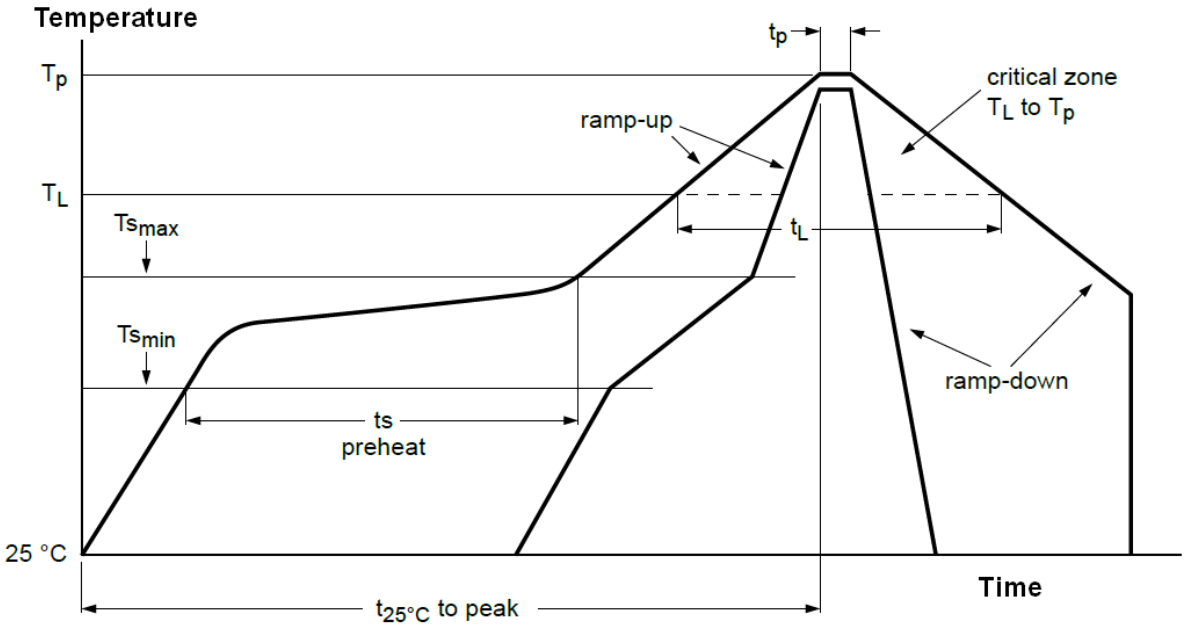

Figure 22. Soldering profile

Table 13. Soldering profile limiting values based on IPC/JEDEC J-STD-020E

Profile feature	SnPb eutectic assembly	Pb-free assembly
Average ramp-up rate (Tsmax to Tp)	3 °C/s maximum	3 °C/s maximum
Preheating		
Temperature minimum (Tsmin)	100 °C	150 °C
Temperature maximum (Tsmax)	150 °C	200 °C
Time (ts: Tsmin to Tsmax)	60 to 120 s	60 to 120 s
Time (tL) maintained above TL		
Liquidous Temperature (TL)	183 °C	217 °C
Time (tL)	60 to 150 s	60 to 150 s
Peak package body temperature (Tp)	235 °C (> 215 °C)	255 °C (> 235 °C)
Time within 5 °C of actual peak temperature (tp)	10 to 30 s	20 to 40 s
Ramp-down rate	6 °C/s maximum	6 °C/s maximum
Time 25 °C to peak temperature	6 min maximum	8 min maximum

7. Revision History

Revision	Date	Description
1.10	Jan 3, 2025	Added DA14594, VDDIO rail discharge function. Added note "Do not use the LDO_IO By-Pass mode." Ref. [2].
1.00	Jan 18, 2024	Initial version.

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Status	Definition
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