Application Note

DA9080 PCB Layout Recommendations

AN-PM-179

Abstract

This application note provides recommendations on how to place and route DA9080 device. It also gives guidance on the passive components needed for proper functioning of the system. This document is a guideline only; target applications may have different requirements.

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1 Terms and Definitions

IC	Channel
FCQFN	Flip chip quad flat-pack no-lead (package)
GND	Ground
IC	Integrated circuit
LDO	Low drop out
PCB	Printed circuit board

2 References

[1] DA9080_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3 Introduction

DA9080 is a five-channel advanced, configurable, system power management IC (PMIC) with four buck regulators and one LDO. Along with several other features, the DA9080 offers dynamic voltage control (DVC), robust protection features, and a dedicated I2C interface. These features coupled with the high-efficiency, fast transient response, and small footprint of the DA9080 lends itself to become the preferred power solution for a host of complex, high-performance applications. The DA9080 is offered in a FCQFN package. For more information, please see the DA9080 Datasheet [1].

The recommended components and connections for DA9080 is shown in Figure 1.

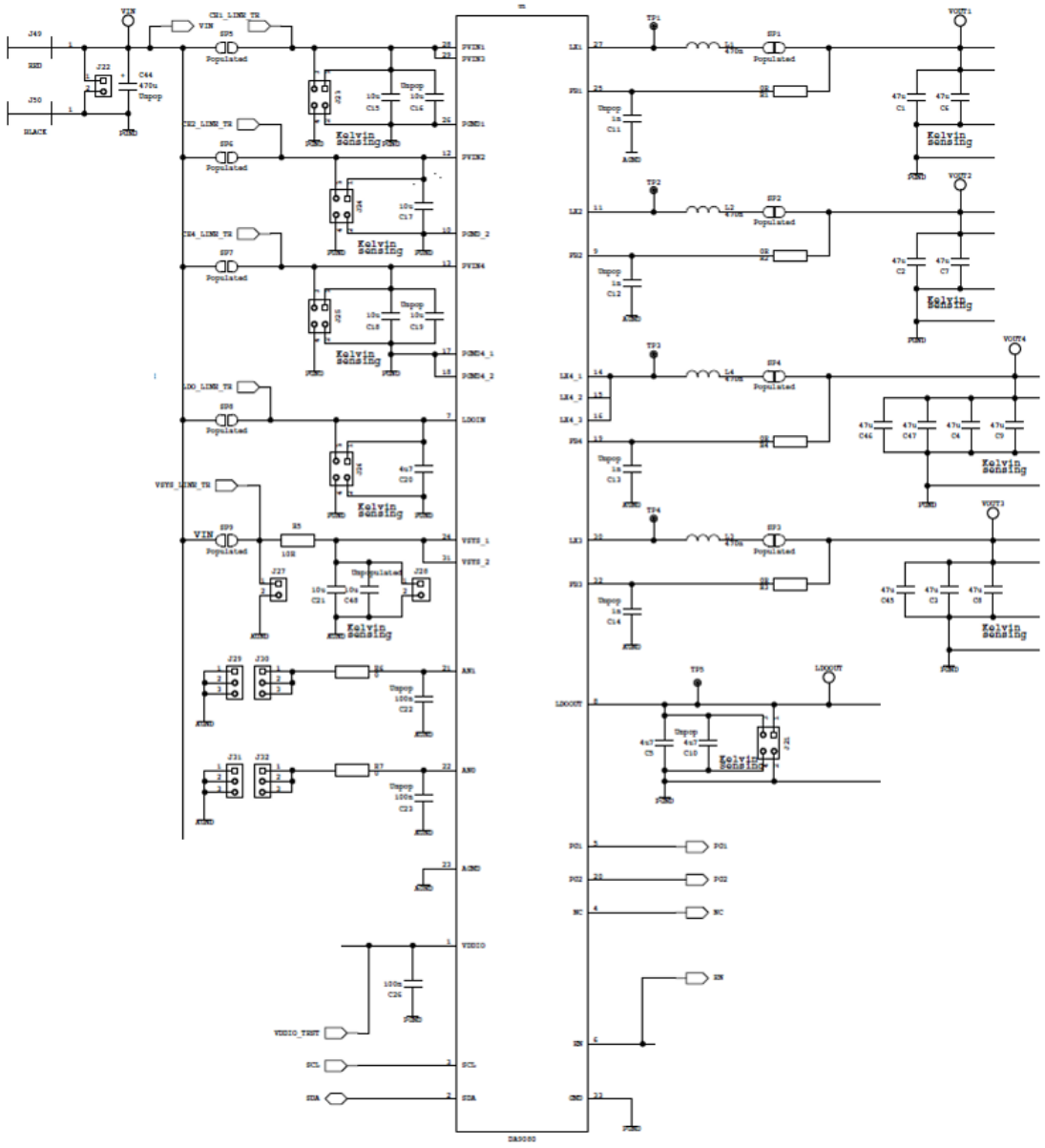

Figure 1: DA9080 Recommended Components and Connections

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Table 1: DA9080 Recommended Components

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
CVSYS	C21	10 µF	X5R or better	10 V or above	N/A
CPVIN1, CPVIN2, CPVIN3, CPVIN4	C15, C16(UNPOP), C17, C18	10 µF	X5R or better	10 V or above	N/A
CVOUT1, CVOUT2, CVOUT3, CVOUT4	C1~4, C6~9, C45~47	47 µF	X5R or better	6.3 V or above	N/A
CLDOIN	C20	4.7 µF	X5R or better	10 V or above	N/A
CLDOOUT	C5	4.7 µF	X5R or better	10 V or above	N/A
CVDDIO	C26	0.1 µF	X5R or better	10 V or above	N/A
LOUT1, LOUT2, LOUT3, LOUT4	L1~4	470 nH	N/A	N/A	5.6 A ISAT typical or above

4 Layout Recommendations

DA9080 comes in a 5.0 x 5.0 mm 32-pin FCQFN package with a 0.5 mm pitch.

Although the PCB layout recommendations described in this application note is with reference to the Renesas Electronics' DA9080 Evaluation Board, a six-layer PCB, the required number of routing layers and other PCB parameters are also determined by the other devices in the system.

4.1 DA9080 Package Information

4.1.1 Pinout

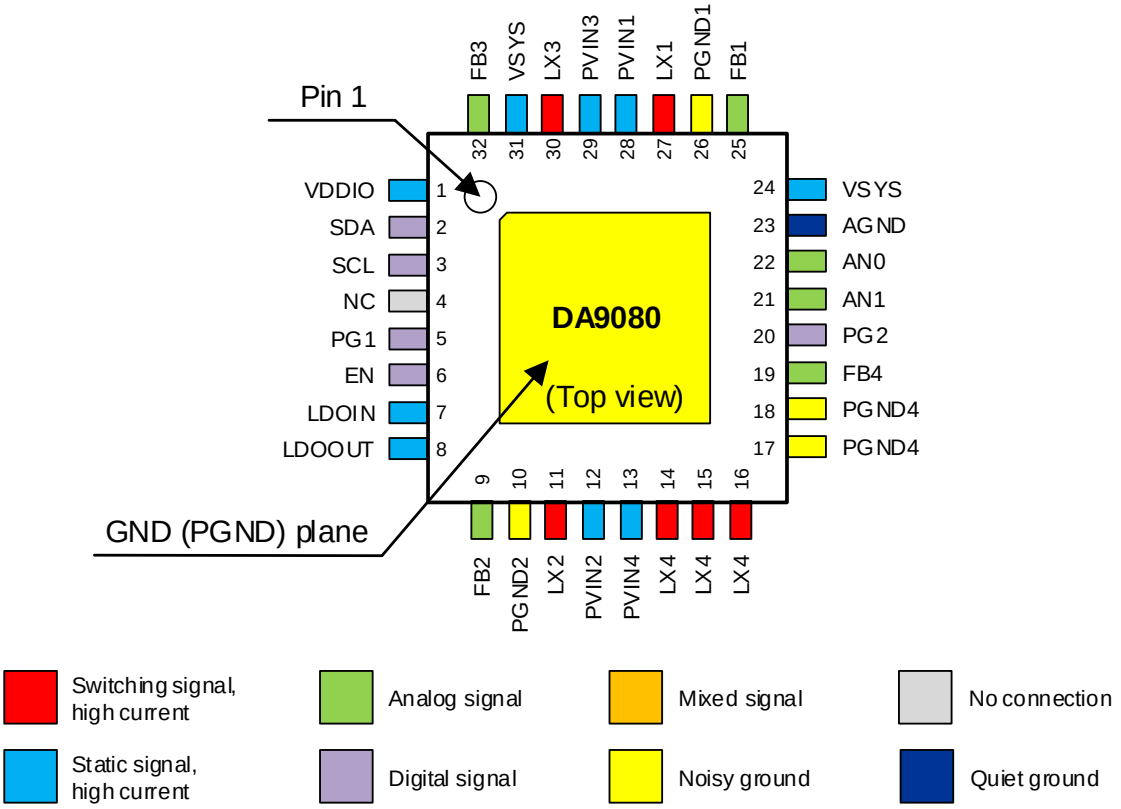

Figure 2: DA9080 FCQFN Pinout Diagram (Top View)

4.1.2 Package Information

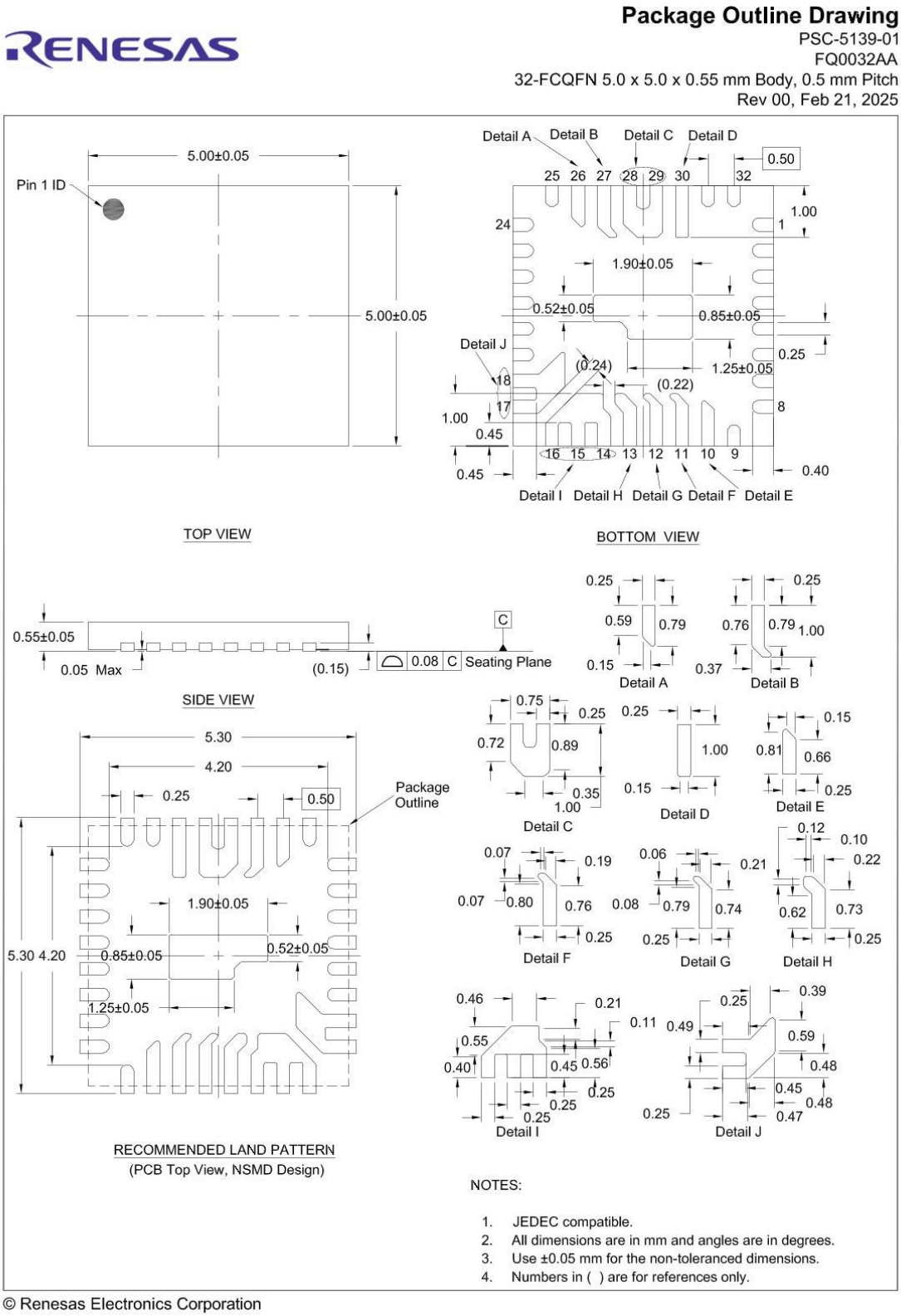

Figure 3: FCQFN5x5 Package Outline Diagram

4.2 Buck Converter and LDO

4.2.1 Input Decoupling

In a buck converter layout, the input capacitor location is critical. Locate the input capacitor as close as possible to the device's input and power GND pins to minimize the parasitic inductance.

In the DA9080 layout design, the input capacitor for each CH<x> should be placed as close as possible to the PVIN<x> and PGND<x> pins, and on the same layer as the DA9080 device.

If multiple layers are used, it is recommended to use as many as possible microvias (or through-hole vias) to minimize line resistance.

Figure 4 shows the input capacitor placement and routing recommendation.

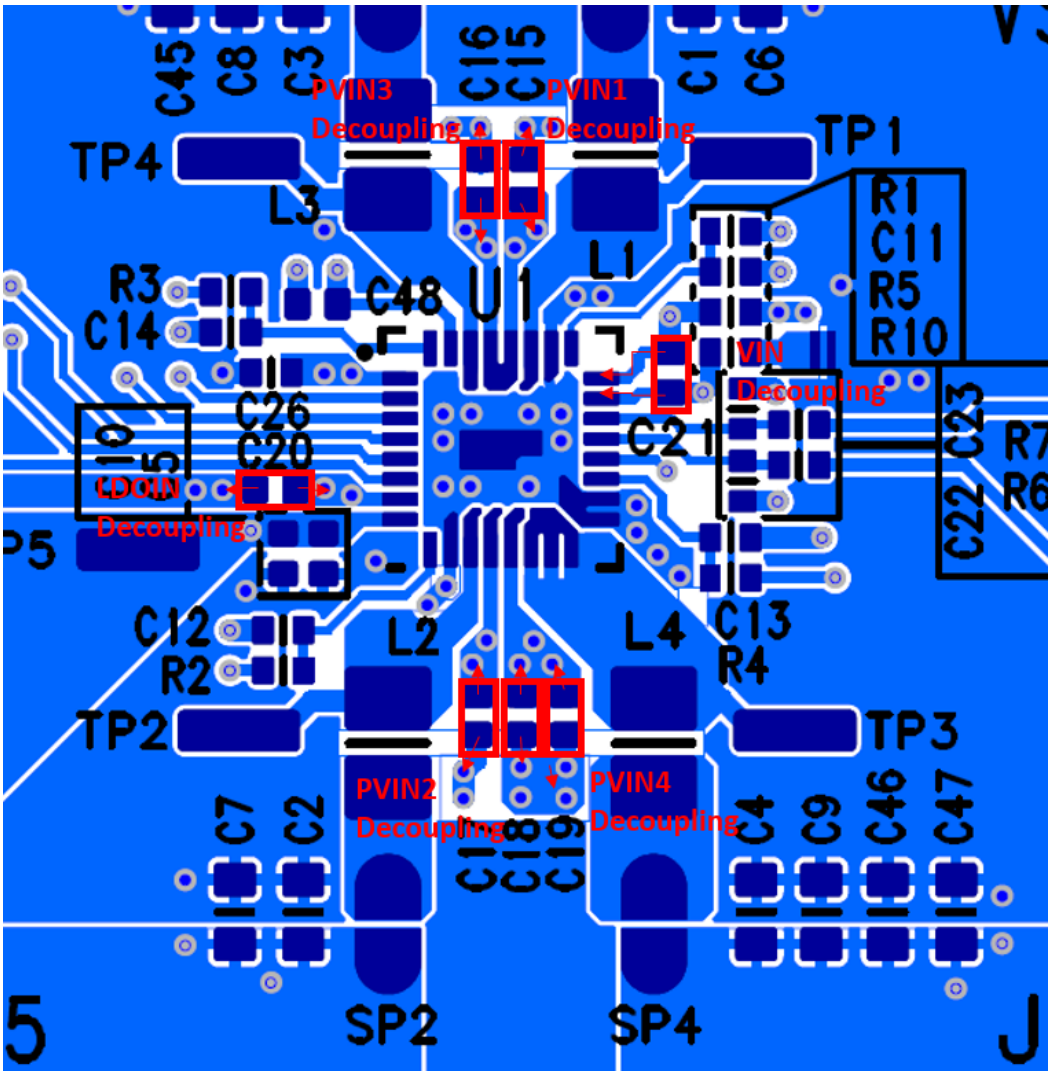

Figure 4: Recommended CH<x> Input Capacitors Placement and Routing

The LDO input capacitor should be placed as close as possible to the LDOIN and PGND pins.

Trace impedances to the LDO input connection should be minimized to reduce drop-out and effects on load regulation.

4.2.2 Ground Connections

Special care should be taken with ground connections because of the high current capability of DA9080 and because of the device's high-performance requirements.

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The power PGND terminals (PGND<x>) of the DA9080 are placed conveniently to allow the placement of the PVIN decoupling capacitors as close as possible to the device.

It is best practice to isolate quiet analog GND (AGND) from noisy power GND terminals (PGND<x>).

On the Renesas Electronics' DA9080 Evaluation Board, AGND is isolated from the power GND terminals (PGND<x>) at the top layer (component layer) and connected at a single point (C21). AGND and power GND (PGND<x>) are connected together with R10 (0R), which is located in a quiet area of the PCB.

Layer 2 can be used as a return power GND plane, where the device's power GND pins (for CH<x>) and output capacitor GND can be connected. It is recommended to minimize the line impedance of the power GND pins and output capacitor GND connections by using as many vias as possible. This will also improve the heat dissipation.

NOTE
It is always recommended to use copper plugged vias to achieve the minimum parasitic via impedance and best thermal performance.

Example of GND terminals connection is illustrated in Figure 5.

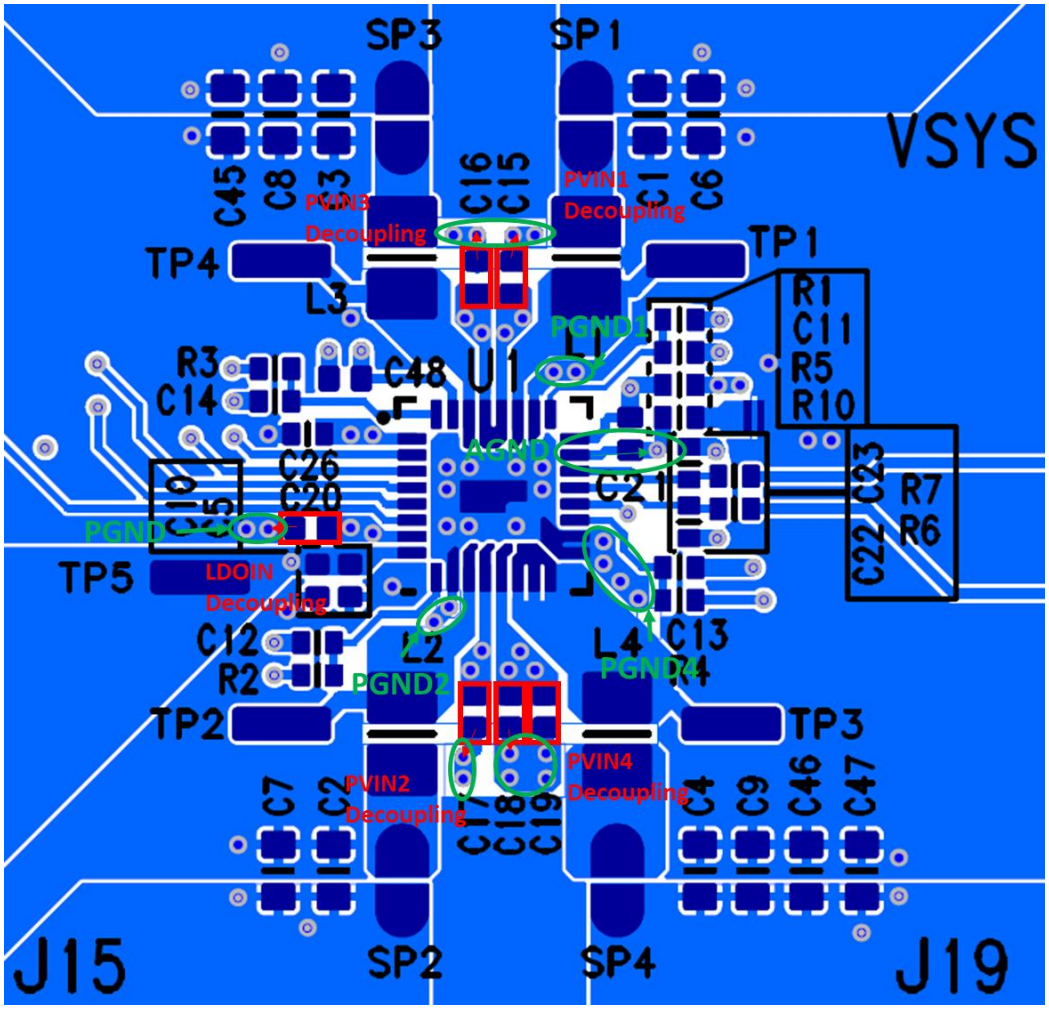

Figure 5: GND Terminals Connection

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To minimize ground-bounce effects from the bucks affecting the LDO or between bucks, it is recommended that GND 'cuts' are applied between each buck. Figure 6 illustrates the power ground with cuts (highlighted by red arrows) implemented on the Renesas Electronics' DA9080 Evaluation Board.?

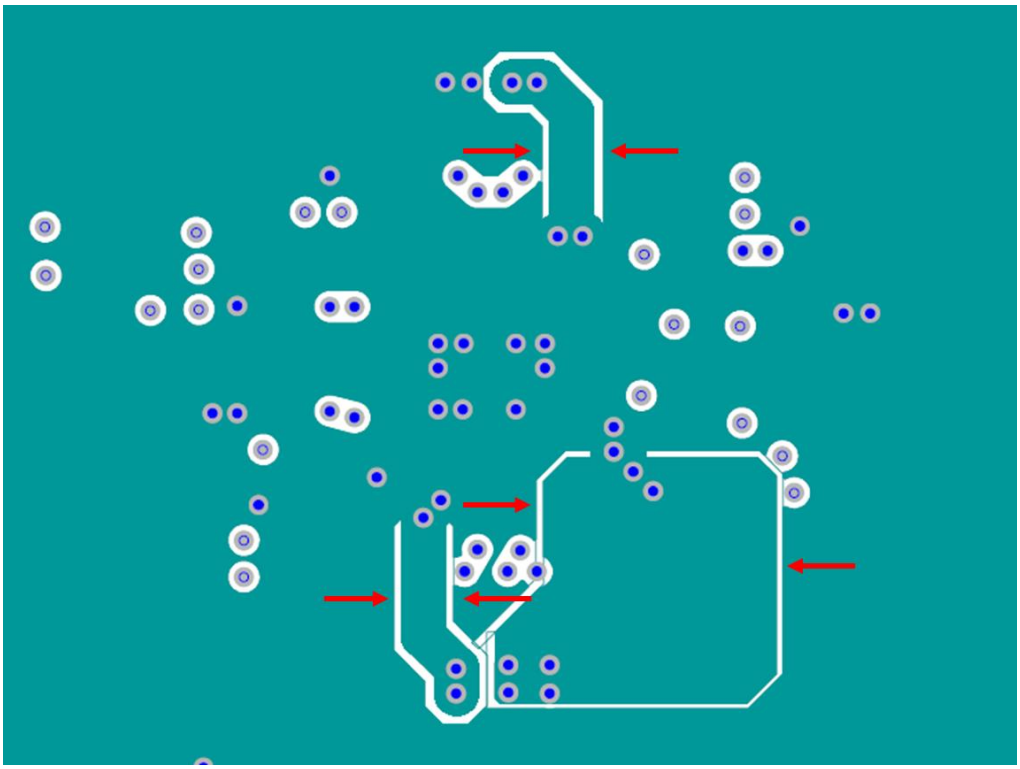

Figure 6: GND Cut on Layer 2

4.2.3 LX Routing

Switch node/LX node traces (traces between LX pins and output inductors) need to be kept as short as possible since this node generates switching noise, which can interfere with buck converters stability. Very high current will flow through these traces and so the minimum width of trace used for this LX node must be considered. Also, if used, ensure that there are enough vias to deliver the current.

The LX node patterns on the Renesas Electronics' DA9080 Evaluation Board are shown in Figure 7. The LX nodes are routed out on layer 1.

Layer 1:

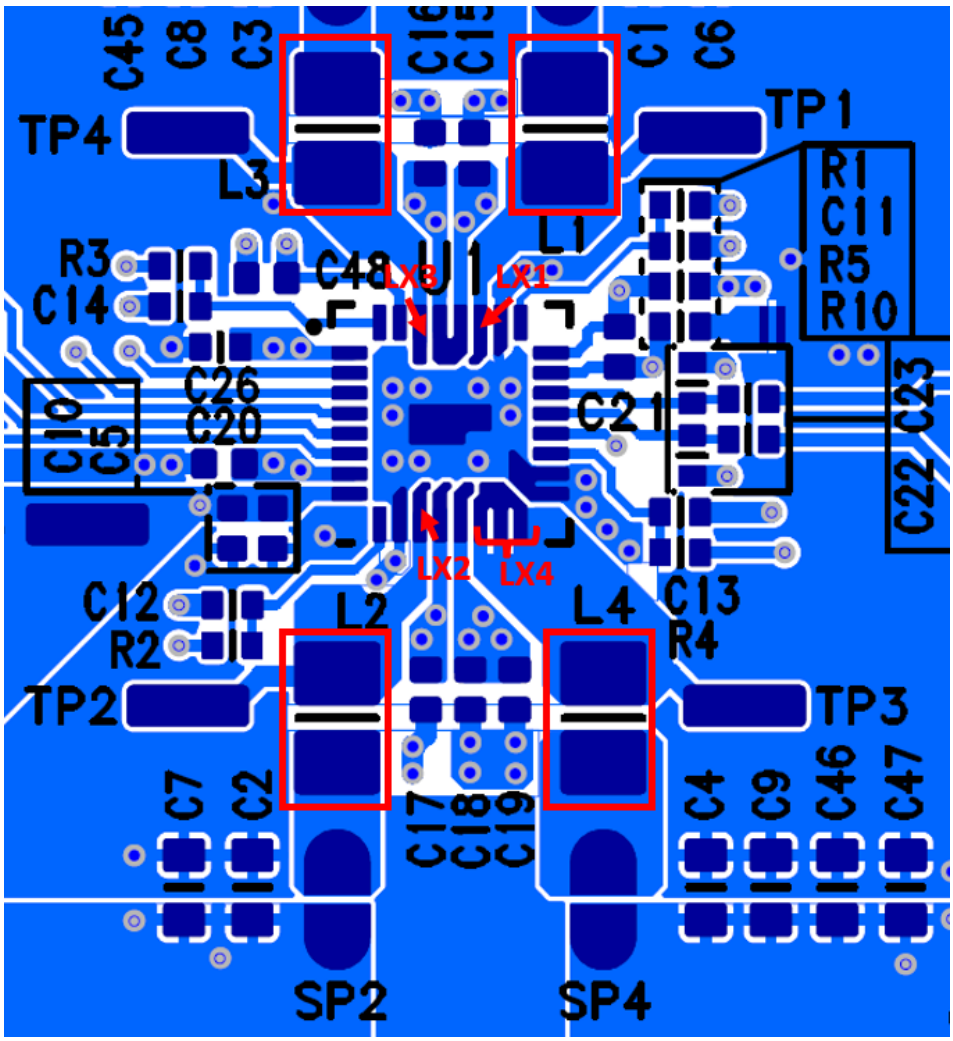

Figure 7: LX Node Pattern on DA9080 Evaluation Board

4.2.4 Buck and LDO

Output capacitors should be placed locally close to the output inductors to avoid any effects to the stability of the buck converters.

Minimizing the distance (which minimizes the line impedance) from the output inductors to the output capacitors is very important since it directly affects the efficiency and load transient response performance of the buck converter. Care must be taken with the size of the output traces to accommodate the high output current that DA9080 needs to support.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

The output capacitors for the LDO should be placed near the device. Trace impedances to the LDO output connection should be minimized to reduce drop-out and effects on load regulation.

4.2.5 Feedback Lines

Feedback lines must be routed far from any noise source (for example, output inductors, LX node, and so on). It is strongly recommended to place an UNPOP bypass capacitor (typically 1 nF) on the feedback. The bypass capacitor should be placed as close as possible to the IC. It is useful for filtering noise which may be injected to the feedback lines due to a layout limitation (for example, a long feedback pattern or noise from other devices in the system).

Also, ensure that the feedback lines are not overlapping any noisy node traces (for example, the LX node trace) without an insulation plane in between.

NOTE
The feedback lines must be routed directly from the load point in order to achieve the best voltage accuracy and stability.

Examples of output-voltage feedback-line routing, on the Renesas Electronics' DA9080 Evaluation Board, is shown in Figure 8.

Layer 6:

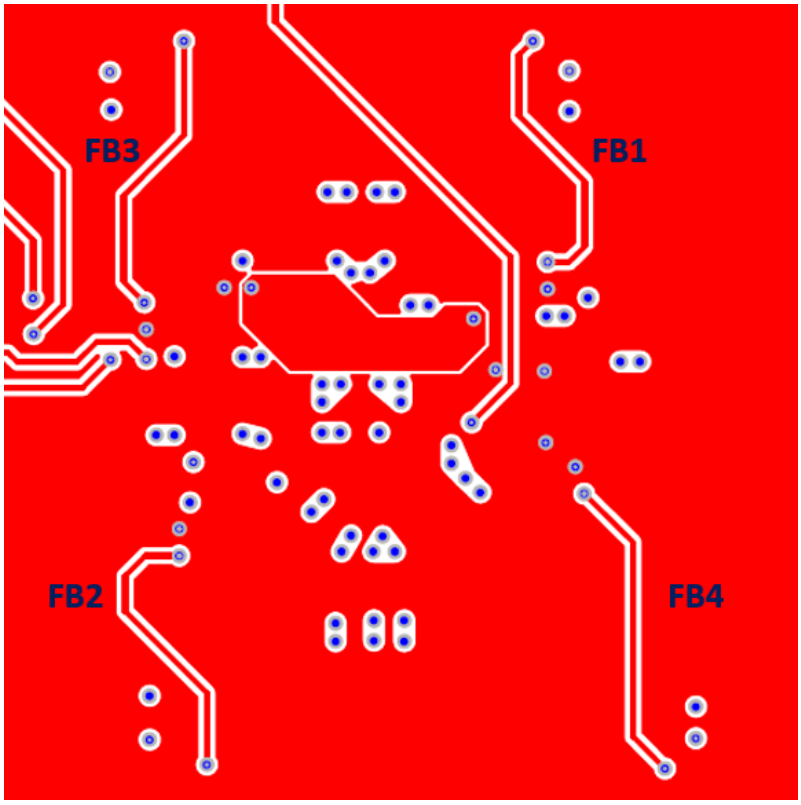

Figure 8: Output Voltage Feedback Line Routing on DA9080 Evaluation Board

4.3 Communication Interface (I^2C)

It is recommended to route the communication interface far from any noise source.

Care must also be taken regarding the noise produced by the interface signal in order to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but it is recommended to use the bottom or top layer.

Revision History

Revision	Date	Description
1	22-Nov-2023	Initial version.
2	04-Apr-2025	Watermark removed and Figure 3 updated.

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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